CIS450 Computer Architecture
Lab 3 quiz
Dr. Daniel Andresen

Notes: This quiz is closed book, closed notes, closed neighbor. Bring a blank sheet of paper to write down your answers. I will select several (but not all) of the questions below for you to answer in class.

1. **Briefly** define the following and discuss their major tradeoffs (advantages/costs). What problem are they addressing?
    a. RISC
    b. CISC
    c. Vector instructions (e.g., SSE/MMX)
    d. Condition codes
    e. Stack
    f. iRAM (the Berkeley project)
2. The IA32 architecture only has 8 registers. Argue for or against whether lots more (say, 64 or 128) would be a good thing.
3. What does the linker do?
4. What does `movl 8(%ebp), %edx` do?
5. What are the SetX instructions used for?
6. Why would goto/jmp be considered poor form for programmers, but be the standard for computer chip architects?
7. What effect would translating all loops to the "do-while" form have on a chip architecture?
8. Why do unconditional branches incur almost no overhead, but conditional branches might?
9. Explain two ways the performance of large "switch" statements is improved by compilers.
10. Summarize the AMD-64 vs. Itanium debate.