CIS 450 – Computer Organization and Architecture
Lab 5
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1. Which of the following programming techniques and structures are "good" for a cached environment? Which are "bad"? Explain your answers. (OSC10.4)
    a. Stack
    b. Hashed symbol table
    c. Sequential search
    d. Binary search
    e. Pure code
    f. Vector operations
    g. Indirection
2. Assume it takes 2 ns. to access an item in L0 cache. Memory access time is 100 ns. What is the maximum acceptable cache miss rate for an effective access time of no more than 104 ns.?
3. Consider a demand-paging system with the following time-measured utilizations.
    CPU utilization – 20%, Paging Disk – 97.7%, Other I/O devices – 5%
    For each of the following, say whether it will (or is likely to) improve CPU utilization. Explain your answers. (OSC 10.9)
    a. Install a faster CPU
    b. Install a bigger paging disk
    c. Increase the degree of multiprogramming
    d. Decrease the degree of multiprogramming
    e. Install more main memory
    f. Install a faster hard disk
    g. Add prepaging to the page-fetch algorithms
    h. Increase the page size
4. Consider the two dimensional array A:
    int a[][] = new int[100][100]
    where a[0][0] is stored at location 200, in a paged memory system with pages of size 200 and a cache with 4 lines of 8 bytes each. Assume an int takes two bytes of storage. A small process resides in page 0 (locations 0-199) for manipulating the A matrix; thus, every instruction fetch will be from page 0. For 101 page frames, how many data cache faults are generated by the following array-initialization loops, using LRU replacement, and assuming page frame 1 has the process in it.
    a. For (j = 0; j < 100; j++)
        for (i = 0; i < 100; i++)
            a[i][j] = 0;
    b. For (i = 0; i < 100; j++)
        for (j = 0; j < 100; i++)
            a[i][j] = 0;