
CIS 721 - Real-Time Systems

Lecture 23: UPPAAL Internals

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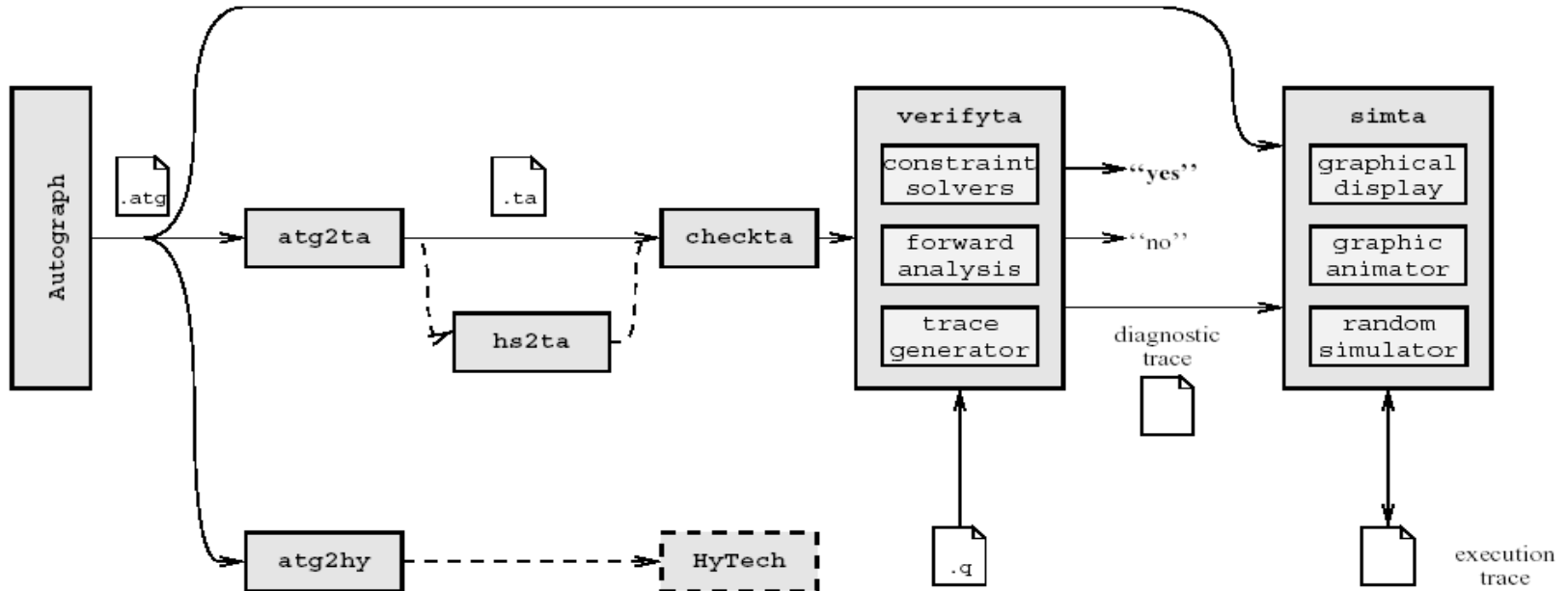
Outline

- Real-Time Verification and Validation Tools
 - **RT-SPIN – Real-Time extensions to SPIN**
 - **UPPAAL – Toolbox for validation and verification of real-time systems**
- Real-Time Communication

UPPAAL Components

- **UPPAAL** consists of three main parts:
 - a **description language**,
 - a **simulator**, and
 - a **model checker**.
 - The **description language** is a non-deterministic guarded command language with data types. It can be used to describe a system as a *network of timed automata* using either a graphical (*.atg, *.xml) or textual (*.xta) format.
 - The **simulator** enables examination of *possible* dynamic executions of a system during the early modeling stages.
 - The **model checker** exhaustively checks *all* possible states.
-

UPPAAL Tools (earlier version)



- **checkta** – syntax checker
- **simta** – simulator
- **verifyta** – model checker

UPPAAL Specification Language

A[] p

E<> p

(AG p) – on all paths A, always G

(EF p) – on some path E, eventually F

A = on all paths, [] = always

E = on some path, <> = eventually

process location data guards clock guards

p ::= a.l | gd | gc | p and p | p or p | not p | p imply p | (p)

In UPPAAL

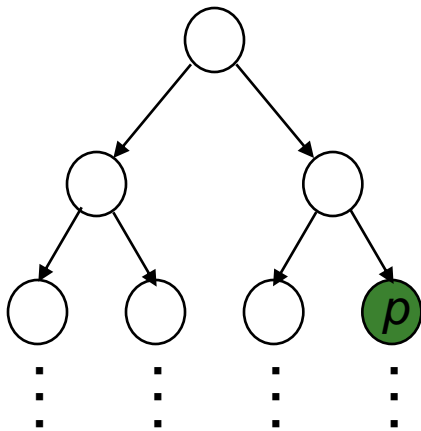
- **Invariantly:** The property $A[] p$ evaluates to true if and only if every reachable state satisfy p .
- **Possibly:** The property $E<> p$ evaluates to true for a timed transition system if and only if there is a sequence of alternating delay transitions and action transitions $s_0 \rightarrow s_1 \rightarrow \dots \rightarrow s_n$, where s_0 is the initial state and s_n satisfies p .
- **Potentially always (on some path always):** The property $E[] p$ evaluates to true for a timed transition system if and only if there is a sequence of alternating delay or action transitions $s_0 \rightarrow s_1 \rightarrow \dots s_i \rightarrow \dots$ for which p holds in all states s_i and which either:
 - is infinite, or
 - ends in a state (L_n, v_n) such that either
 - for all d : $(L_n, v_n + d)$ satisfies p and $Inv(L_n)$, or
 - there is no outgoing transition from (L_n, v_n)
- **Eventually (on all paths eventually):** The property $A<> p$ evaluates to true if (and only if) all possible transition sequences eventually reaches a state satisfying p . An *eventually* property $A<> p$ can be expressed as the *potentially* property $\text{not } E[] \text{ not } p$.

CTL, Derived Operators

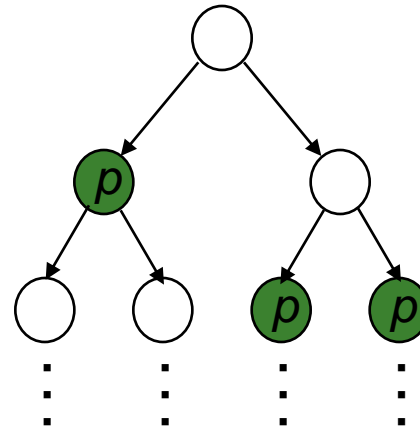
$$EF \phi \equiv E[\text{true} \mathbf{U} \phi] \quad \text{possible}$$

$$AF \phi \equiv A[\text{true} \mathbf{U} \phi]. \quad \text{inevitable}$$

$EF p$



$AF p$



CTL, Derived Operators

$$EG \phi \equiv \neg AF \neg \phi$$

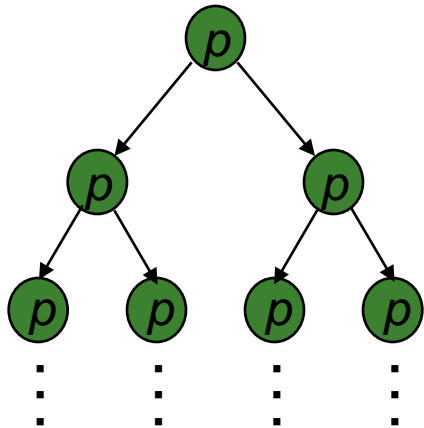
potentially always

$$AG \phi \equiv \neg EF \neg \phi$$

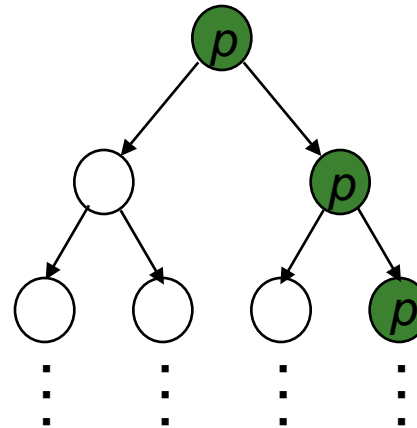
always

$$AX \phi \equiv \neg EX \neg \phi.$$

$AG p$

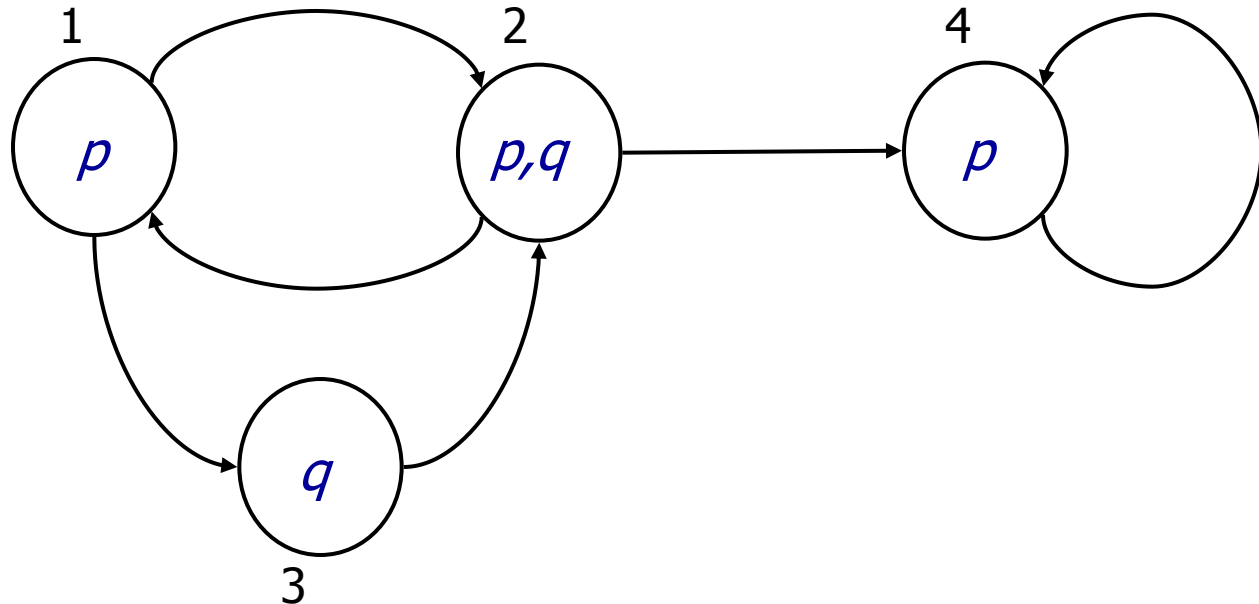


$EG p$



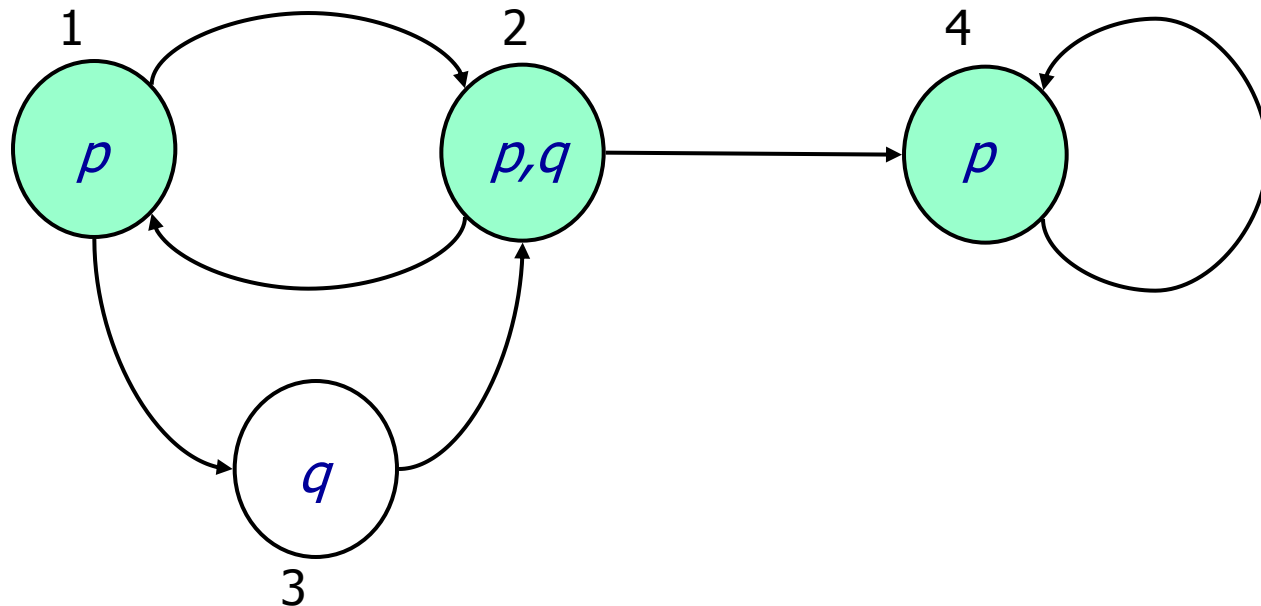
Example

$E[] p$



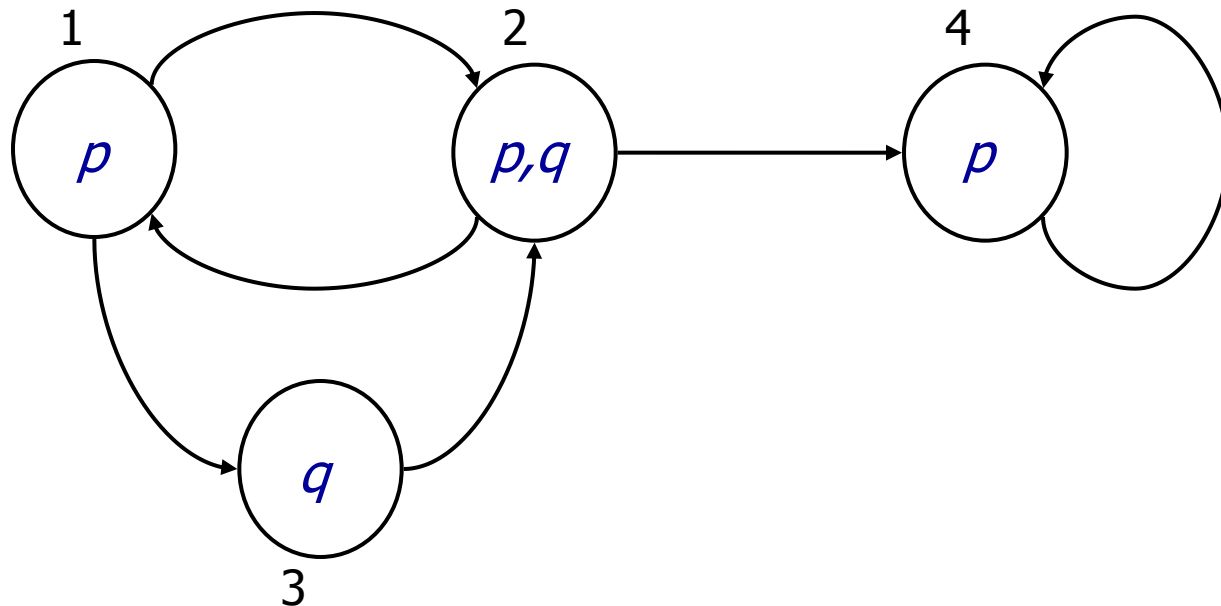
Example

$E[] p$



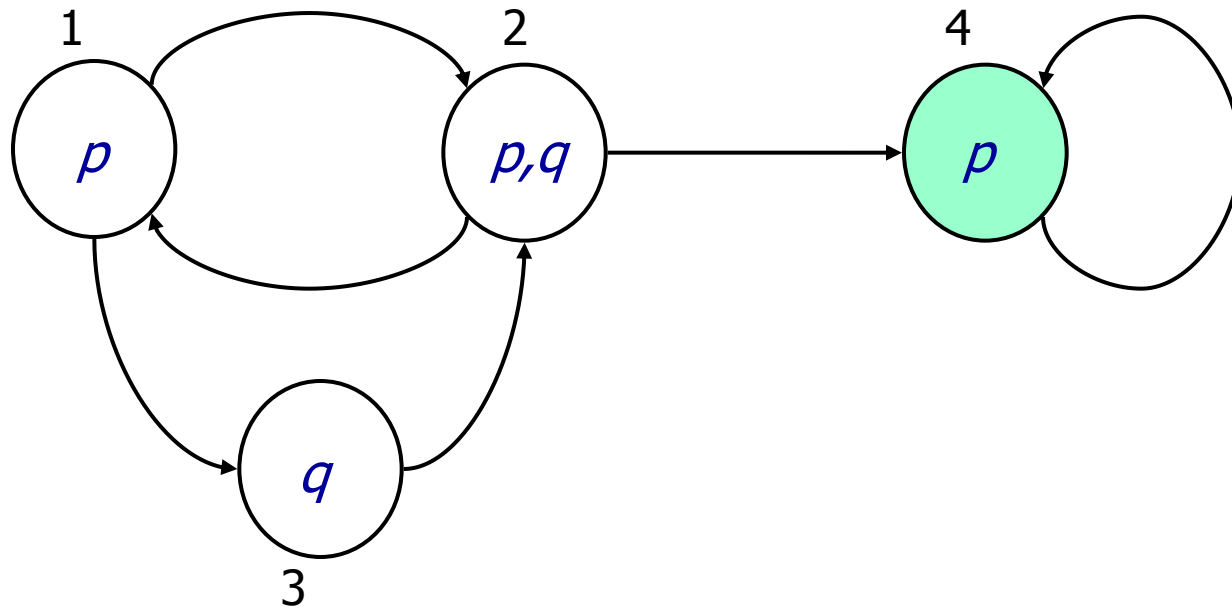
Example

A[] p



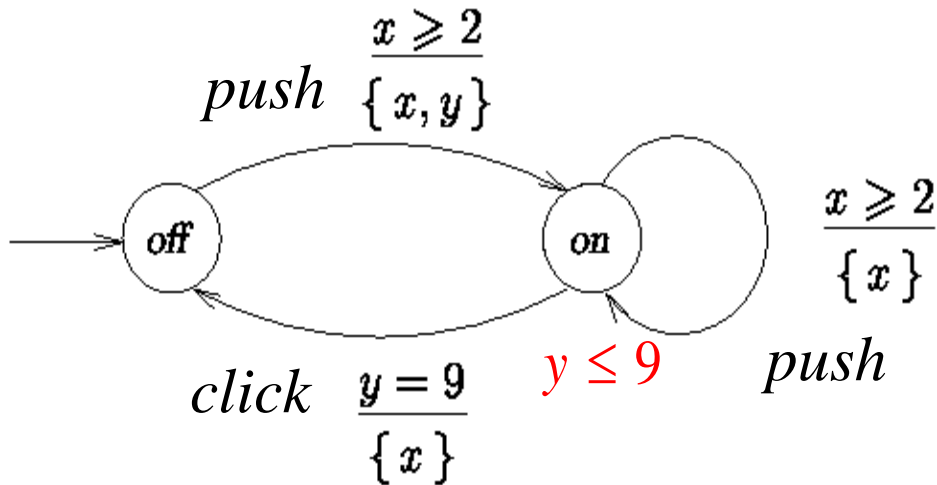
Example

A[] p



Timed CTL (TCTL)

Light Switch

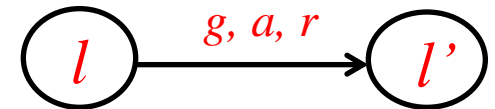


- Switch may be turned on whenever at least 2 time units has elapsed since last “turn off”
- Light automatically switches off after 9 time units.

Semantics

- clock valuations: $V(C) \quad v: C \rightarrow R_{\geq 0}$
- state: (l, v) where $l \in L$ and $v \in V(C)$
- Semantics of timed automata is a labeled transition system (S, \rightarrow) where

$$S = \{ (l, v) \mid v \in V(C) \text{ and } l \in L \}$$



- action transition

$$(l, v) \xrightarrow{a} (l', v') \text{ iff}$$

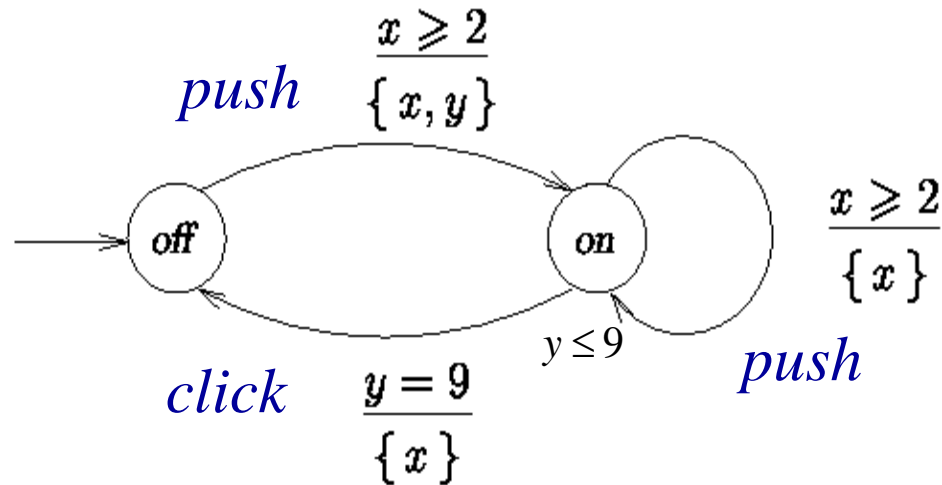
$$g(v) \text{ and } v' = v[r] \text{ and } \text{Inv}(l')(v')$$

- delay Transition

$$(l, v) \xrightarrow{d} (l, v + d) \text{ iff}$$

$$\text{Inv}(l)(v + d') \text{ whenever } d' \leq d \in R_{\geq 0}$$

Semantics: Example



$$(off, x = y = 0) \xrightarrow{3.5} (off, x = y = 3.5) \xrightarrow{push} \rightarrow$$

$$(on, x = y = 0) \xrightarrow{\pi} (on, x = y = \pi) \xrightarrow{push} \rightarrow$$

$$(on, x = 0, y = \pi) \xrightarrow{3} (on, x = 3, y = \pi + 3) \xrightarrow{9 - (\pi + 3)} \rightarrow$$

$$(on, x = 9 - (\pi + 3), y = 9) \xrightarrow{click} (off, x = 0, y = 9) \dots$$

Light Switch (cont.)

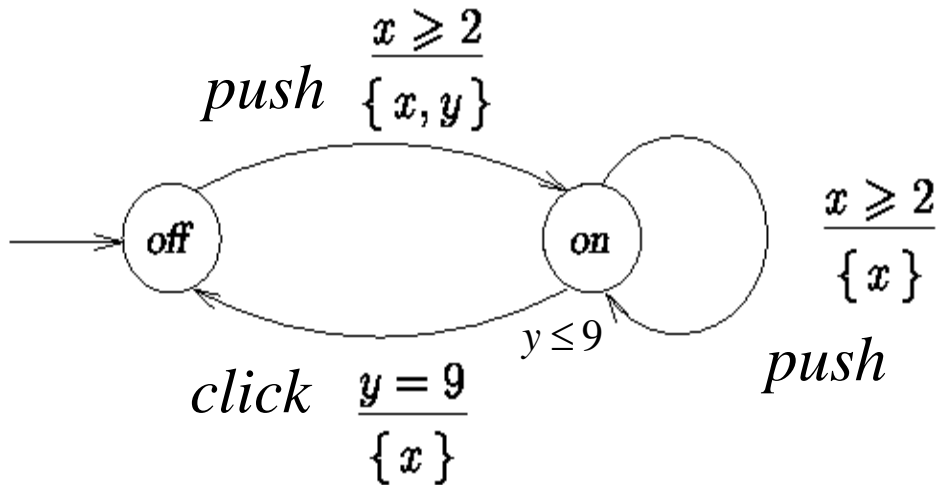
$A[] \quad (x \leq y)$

$AG(x \leq y)$

$P.on \rightarrow P.off$

$AG(on \Rightarrow AF\ off)$

$AG(on \Rightarrow AF_{\leq 9} off)$



$A[off \cup x \geq 2]$

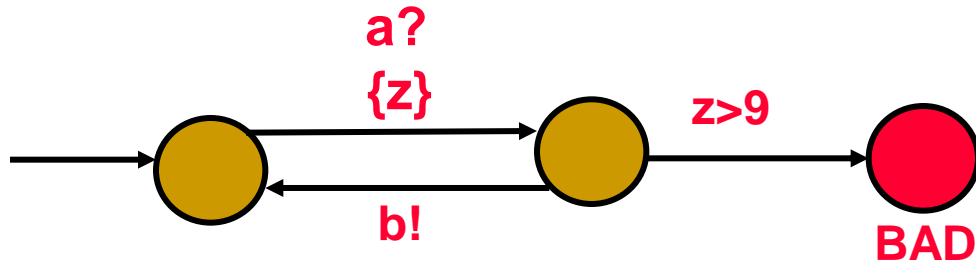
$A[off \cup x \geq 3]$

$E[off \cup x \geq 3]$

$A[x \leq 2 \cup on]$

$E[x \leq 2 \cup on]$

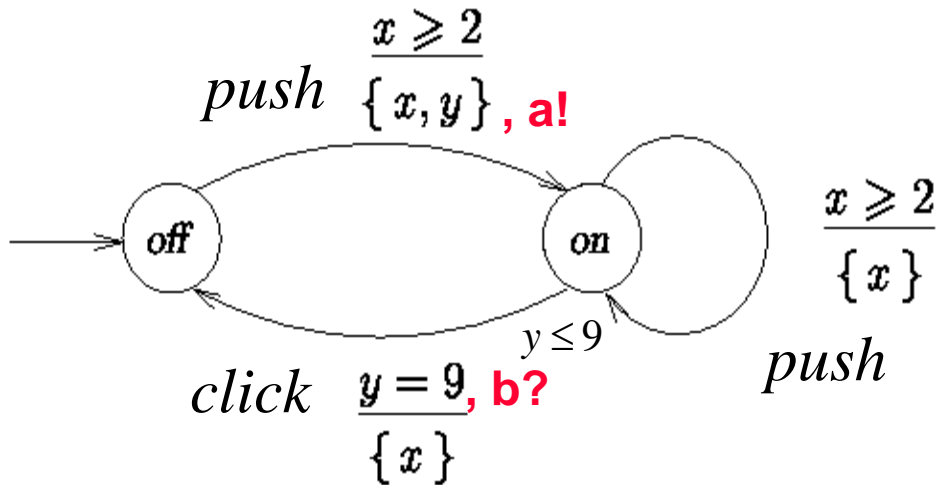
Light Switch (Add Observer)



$AG(x \leq y)$

$AG(on \Rightarrow AF\ off)$

$AG(on \Rightarrow AF_{\leq 9} off)$



$A[off \cup x \geq 2]$

$A[off \cup x \geq 3]$

$E[off \cup x \geq 3]$

$A[x \leq 2 \cup on]$

$E[x \leq 2 \cup on]$

Timeliness Properties

$$\text{AG} [\text{send}(m) \Rightarrow \text{AF}_{<5} \text{receive}(r_m)]$$

receive(m) always occurs within 5 time units after *send(m)*

$$\text{EG} [\text{send}(m) \Rightarrow \text{AF}_{=11} \text{receive}(r_m)]$$

receive(m) may occur exactly 11 time units after *send(m)*

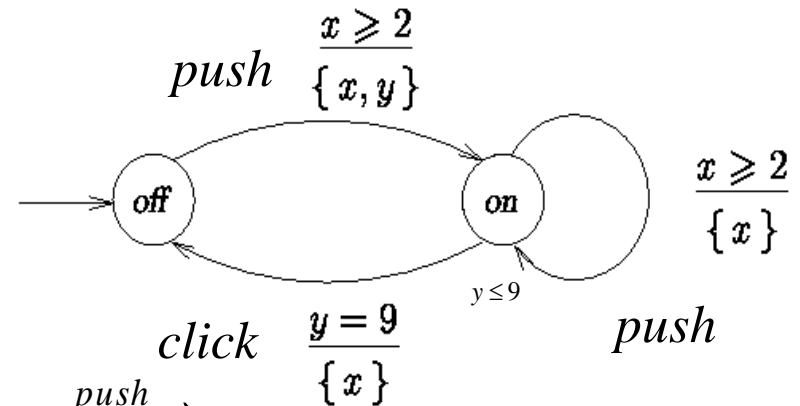
$$\text{AG} [\text{AF}_{=25} \text{putbox}]$$

putbox occurs periodically (exactly) every 25 time units
(note: other *putbox*'s may occur in between)

Paths

A *path* is an infinite sequence $s_0 a_0 s_1 a_1 s_2 a_2 \dots$ of states alternated by transition labels such that $s_i \xrightarrow{a_i} s_{i+1}$ for all $i \geq 0$.

Example Path:



$$(off, x = y = 0) \xrightarrow{3.5} (off, x = y = 3.5) \xrightarrow{push} \rightarrow$$

$$(on, x = y = 0) \xrightarrow{\pi} (on, x = y = \pi) \xrightarrow{push} \rightarrow$$

$$(on, x = 0, y = \pi) \xrightarrow{3} (on, x = 3, y = \pi + 3) \xrightarrow{9 - (\pi + 3)} \rightarrow$$

$$(on, x = 9 - (\pi + 3), y = 9) \xrightarrow{click} (off, x = 0, y = 9) \dots$$

Elapsed Time in Path

$$\Delta(\sigma, 0) = 0$$

$$\Delta(\sigma, i+1) = \Delta(\sigma, i) + \begin{cases} 0 & \text{if } a_i = * \\ a_i & \text{if } a_i \in \mathbb{R}^+. \end{cases}$$

Example:

$$\begin{aligned} \sigma = & (off, x = y = 0) \xrightarrow{3.5} (off, x = y = 3.5) \xrightarrow{push} \\ & (on, x = y = 0) \xrightarrow{\pi} (on, x = y = \pi) \xrightarrow{push} \\ & (on, x = 0, y = \pi) \xrightarrow{3} (on, x = 3, y = \pi + 3) \xrightarrow{9-(\pi+3)} \\ & (on, x = 9-(\pi+3), y = 9) \xrightarrow{click} (off, x = 0, y = 9) \dots \end{aligned}$$

$$\Delta(\sigma, 1) = 3.5, \Delta(\sigma, 6) = 3.5 + 9 = 12.5$$

TCTL Semantics

$s, w \models p$	iff $p \in \text{Label}(s)$
$s, w \models \alpha$	iff $v \cup w \models \alpha$
$s, w \models \neg \phi$	iff $\neg(s, w \models \phi)$
$s, w \models \phi \vee \psi$	iff $(s, w \models \phi) \vee (s, w \models \psi)$
$s, w \models z \text{ in } \phi$	iff $s, \text{reset } z \text{ in } w \models \phi$
$s, w \models E[\phi U \psi]$	iff $\exists \sigma \in P_{\mathcal{M}}^{\infty}(s). \exists (i, d) \in \text{Pos}(\sigma).$

$$(\sigma(i, d), w + \Delta(\sigma, i) \models \psi \wedge \\ (\forall (j, d') \ll (i, d). \sigma(j, d'), w + \Delta(\sigma, j) \models \phi \vee \psi))$$

$s, w \models A[\phi U \psi]$	iff $\forall \sigma \in P_{\mathcal{M}}^{\infty}(s). \exists (i, d) \in \text{Pos}(\sigma).$
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$$((\sigma(i, d), w + \Delta(\sigma, i)) \models \psi \wedge \\ (\forall (j, d') \ll (i, d). (\sigma(j, d'), w + \Delta(\sigma, j)) \models \phi \vee \psi)).$$

s - (location, clock valuation)

w - formula clock valuation

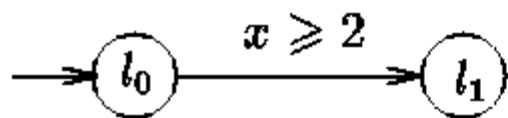
$P_{\mathcal{M}}^{\infty}(s)$ - set of paths from s

$\text{Pos}(\sigma)$ - positions in σ

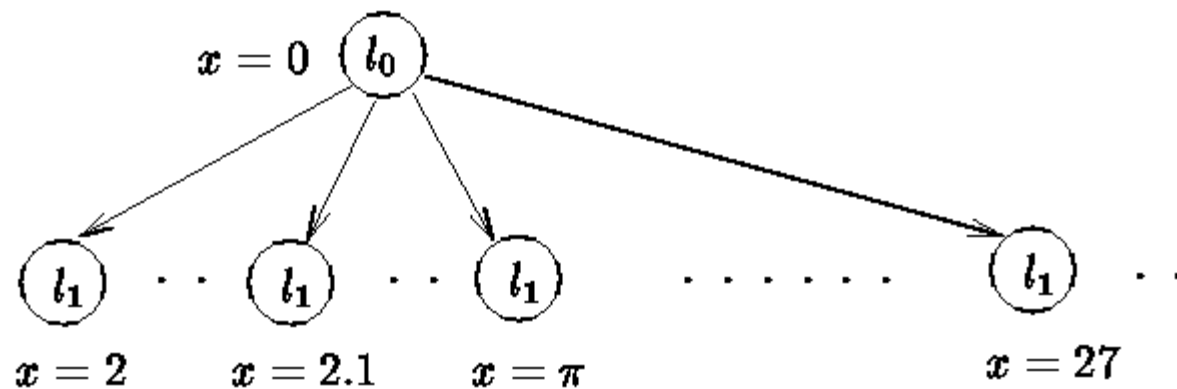
$\Delta(\sigma, i)$ - elapsed time

$$(i, d) \ll (j, d') \text{ iff } (i < j) \text{ or } ((i = j) \text{ and } (d < d'))$$

Infinite State Space?

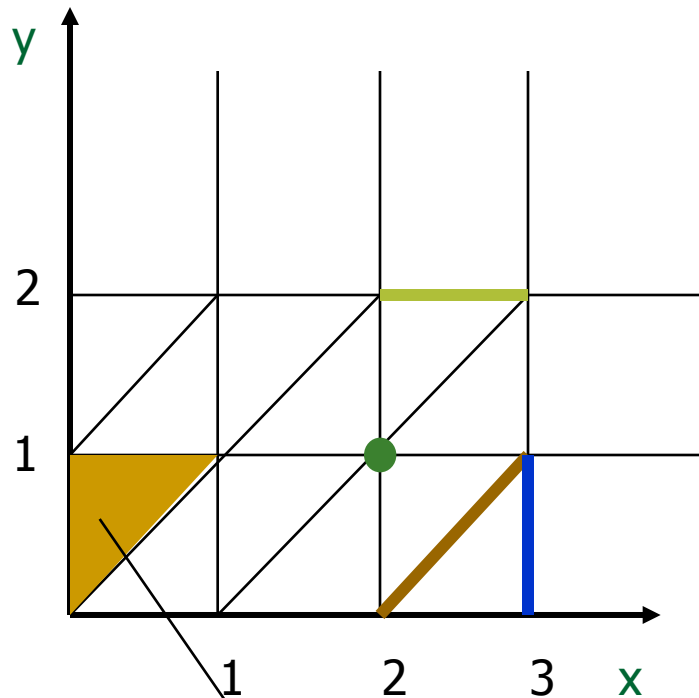


gives rise to the
infinite transition system:



Regions – two clocks: x, y

Finite partitioning of state space



Definition

$w \approx w'$ iff w and w' satisfy the exact same conditions of the form

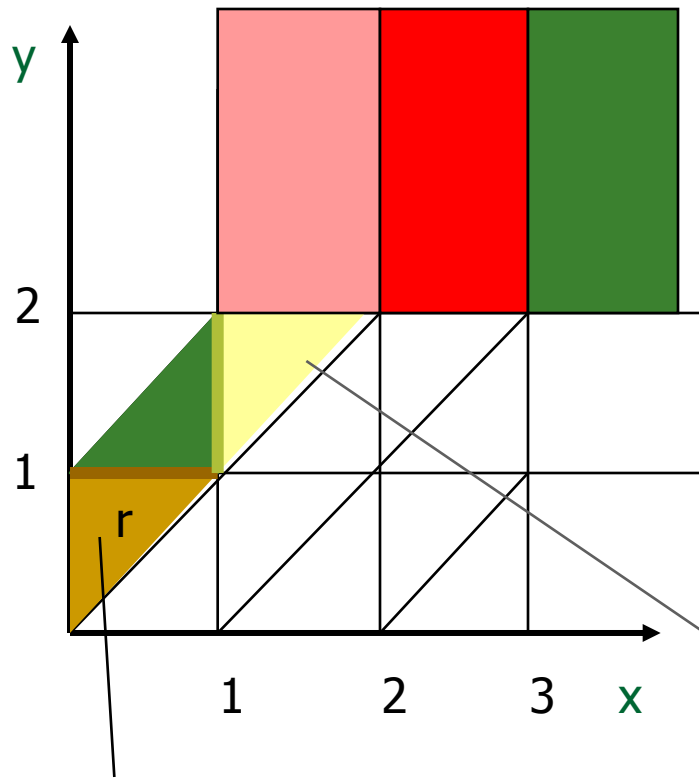
$$x_i \leq n \text{ and } x_i - x_j \leq n$$

where $n \leq \max$

An equivalence class (i.e. a *region*)
in fact there are only a *finite* number of regions!

Regions

Finite partitioning of state space



Definition

$w \approx w'$ iff w and w' satisfy the exact same conditions of the form

$$x_i \leq n \text{ and } x_i - x_j \leq n$$

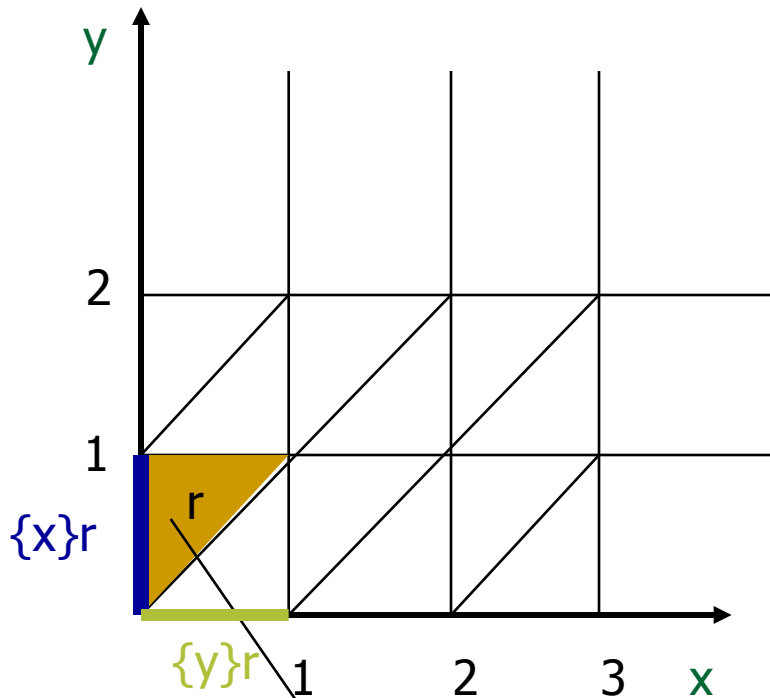
where $n \leq \max$

Successor regions, $\text{Succ}(r)$

An equivalence class (i.e. a *region*)

Regions

Finite partitioning of state space



Reset
regions

An equivalence class (i.e. a *region*) r

Definition

$w \approx w'$ iff w and w' satisfy
the exact same conditions of
the form

$$x_i \leq n \text{ and } x_i - x_j \leq n$$

where $n \leq \max$

THEOREM

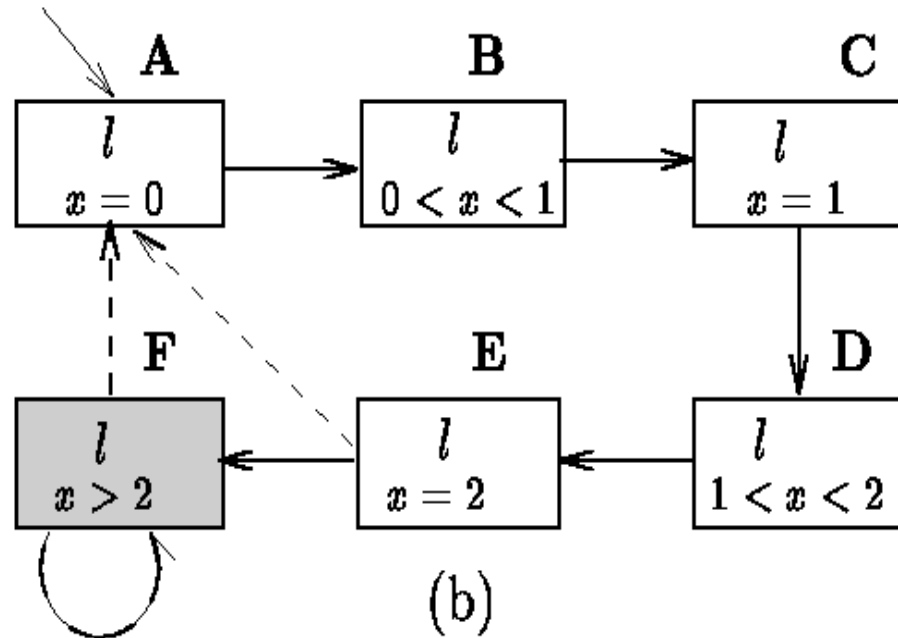
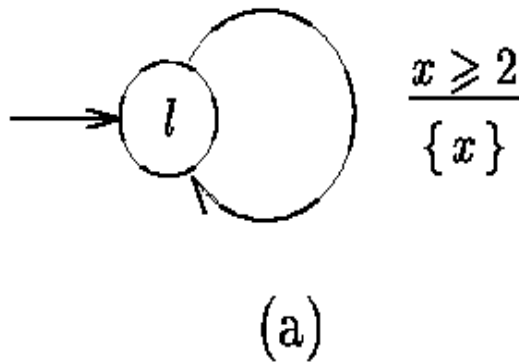
Whenever $uv \approx u'v'$ then

$$[(l, u), v] \text{ sat } \phi$$

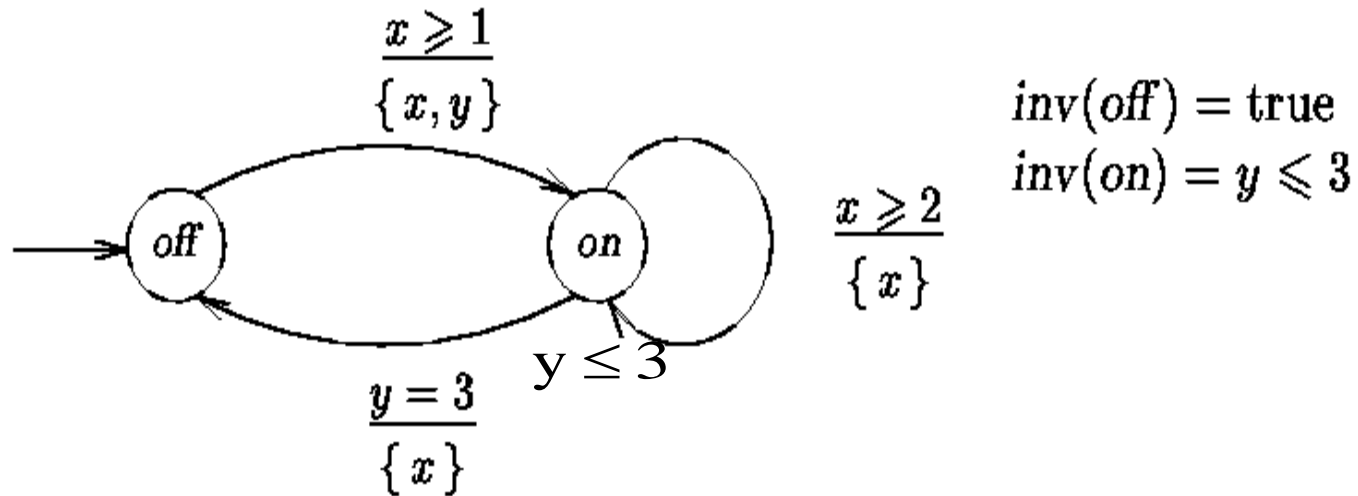
\Leftrightarrow

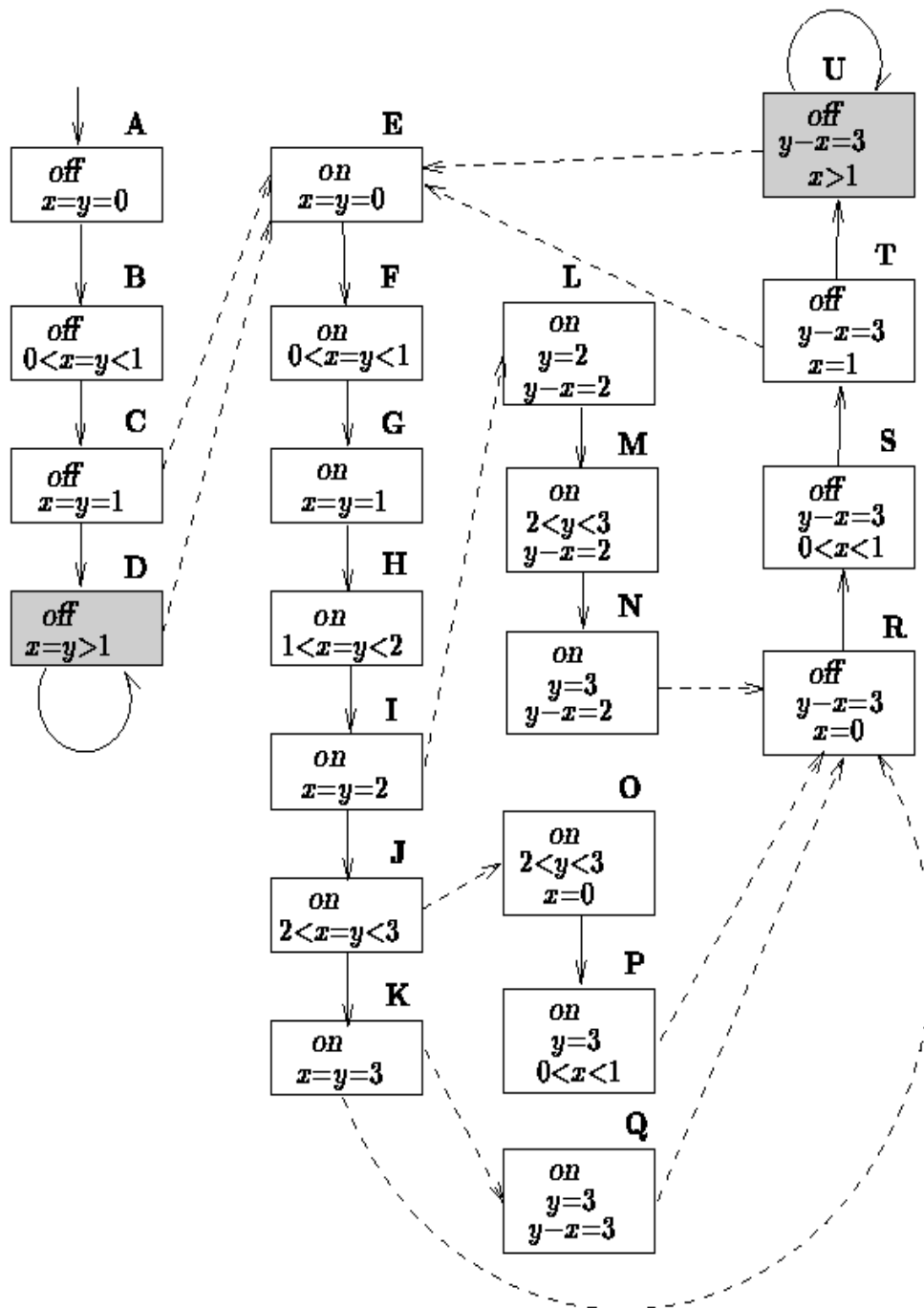
$$[(l, u'), v'] \text{ sat } \phi$$

Region graph of simple timed automata



Modified light switch





Reachable part
of region graph

Properties

$AG(x \leq y)$

$AG(on \Rightarrow AF_{off})$

$AG(on \Rightarrow AF_{\leq 3} off)$

Roughly speaking....

Model checking a timed automata
against a TCTL-formula amounts to
model checking its region graph
against a CTL-formula

Problem to be solved

The worst-case time complexity of model checking TCTL-formula ϕ over timed automaton \mathcal{A} , with the clock constraints of ϕ and \mathcal{A} in Ψ is:

$$\mathcal{O}(|\phi| \times (n! \times 2^n \times \prod_{x \in \Psi} c_x \times |L|^2)).$$

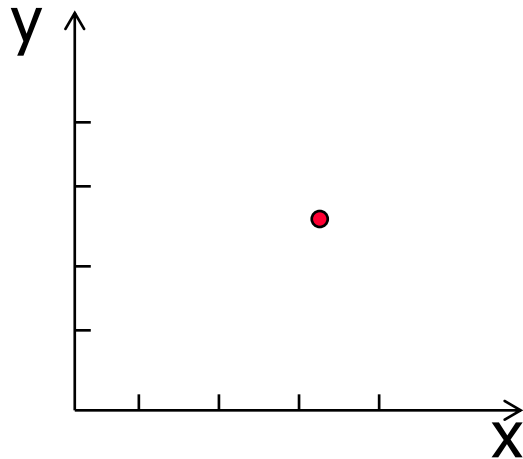
- 😊 (i) linear in the length of the formula ϕ
- 😐 (ii) exponential in the number of clocks in \mathcal{A} and ϕ
- 😞 (iii) exponential in the maximal constants with which clocks are compared in \mathcal{A} and ϕ .

Model Checking TCTL is PSPACE-hard

Zones: From Infinite to Finite

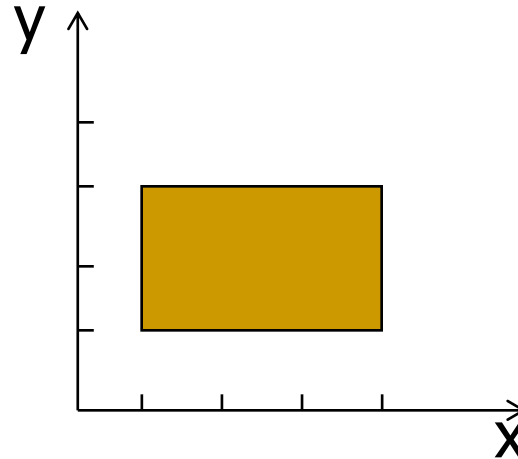
State

(n, $x=3.2$, $y=2.5$)

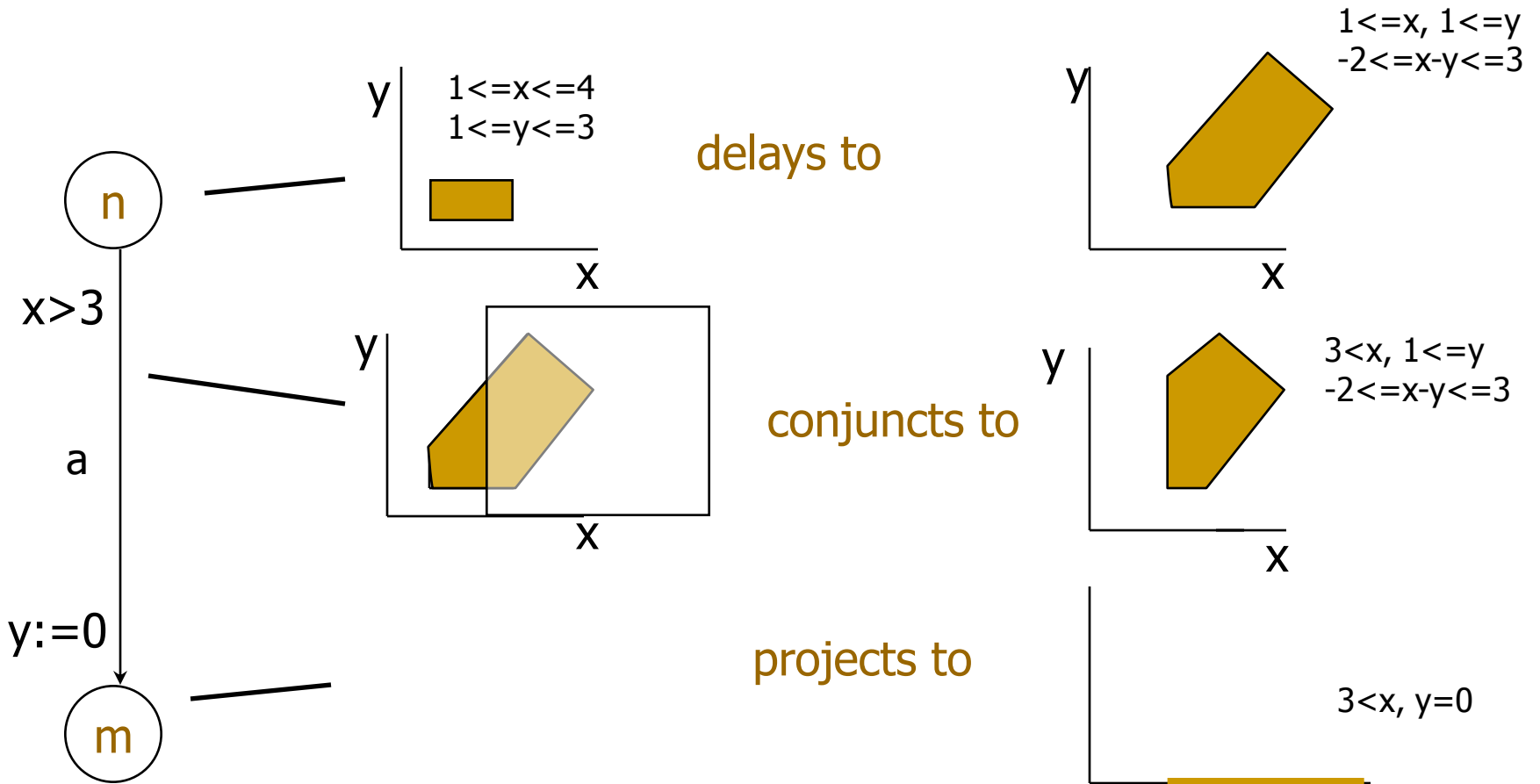


Symbolic state (set)

(n, $1 \leq x \leq 4$, $1 \leq y \leq 3$)



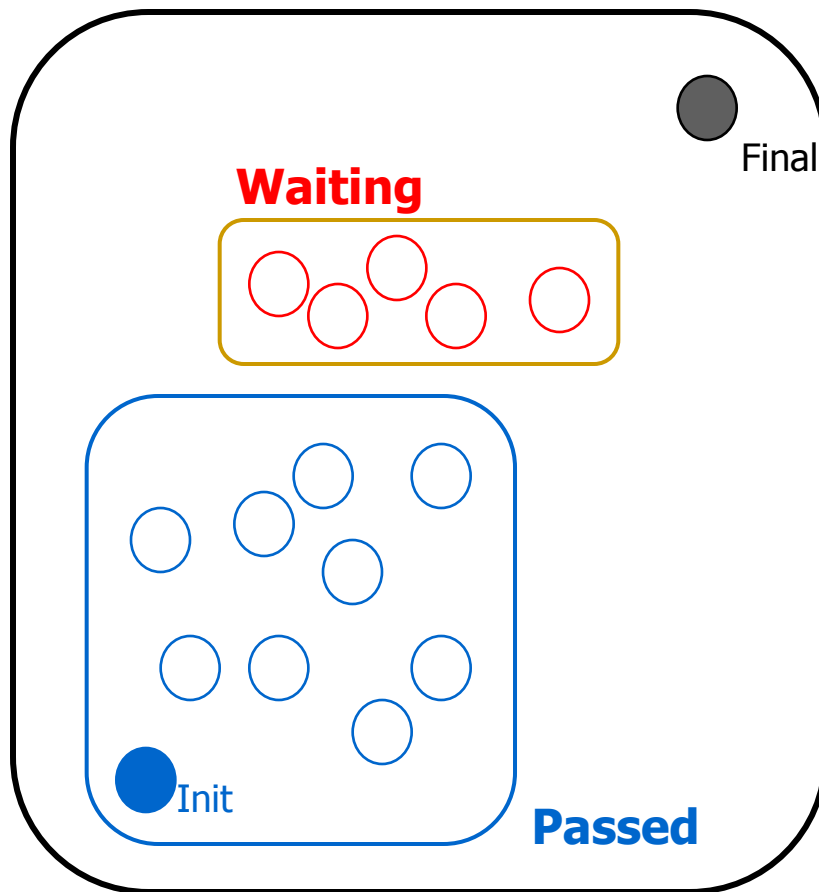
Symbolic Transitions



Thus $(n, 1 \leq x \leq 4, 1 \leq y \leq 3) = a \Rightarrow (m, 3 < x, y = 0)$

Forward Reachability

Init -> **Final** ?



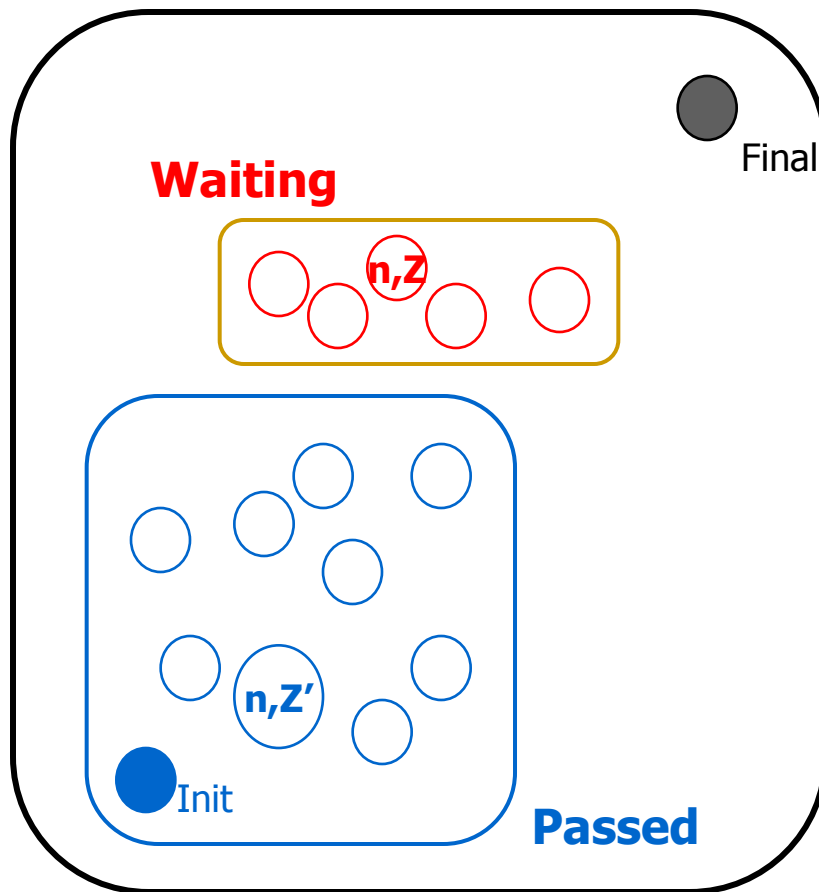
INITIAL **Passed** := \emptyset ;
Waiting := $\{(n_0, Z_0)\}$

REPEAT

UNTIL **Waiting** = \emptyset
or
Final is in **Waiting**

Forward Reachability

Init \rightarrow Final ?



INITIAL **Passed** $:= \emptyset$;
Waiting $:= \{(n_0, Z_0)\}$

REPEAT

- pick (n, Z) in **Waiting**
- **if** for some $Z' \supseteq Z$
 (n, Z') in **Passed** then **STOP**

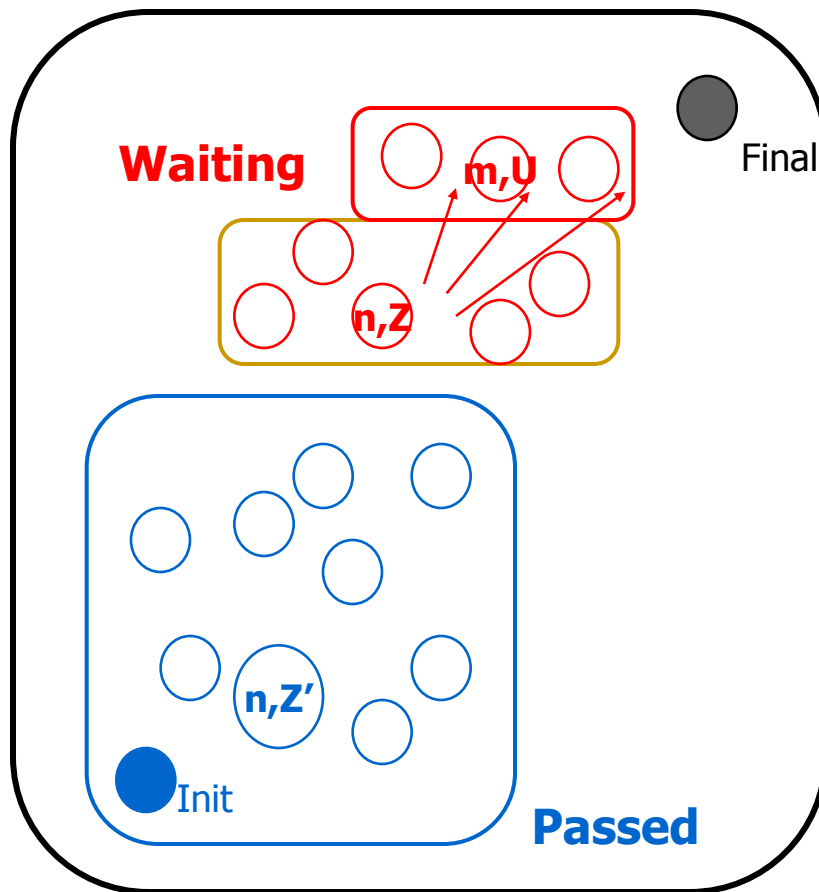
UNTIL **Waiting** $= \emptyset$

or

Final is in **Waiting**

Forward Reachability

Init \rightarrow Final ?



INITIAL **Passed** $:= \emptyset$;
Waiting $:= \{(n_0, Z_0)\}$

REPEAT

- pick (n, Z) in **Waiting**
- **if** for some $Z' \supseteq Z$
 (n, Z') in **Passed** **then STOP**
- **else** /explore/ add
 $\{ (m, U) : (n, Z) \Rightarrow (m, U) \}$
 to **Waiting**;

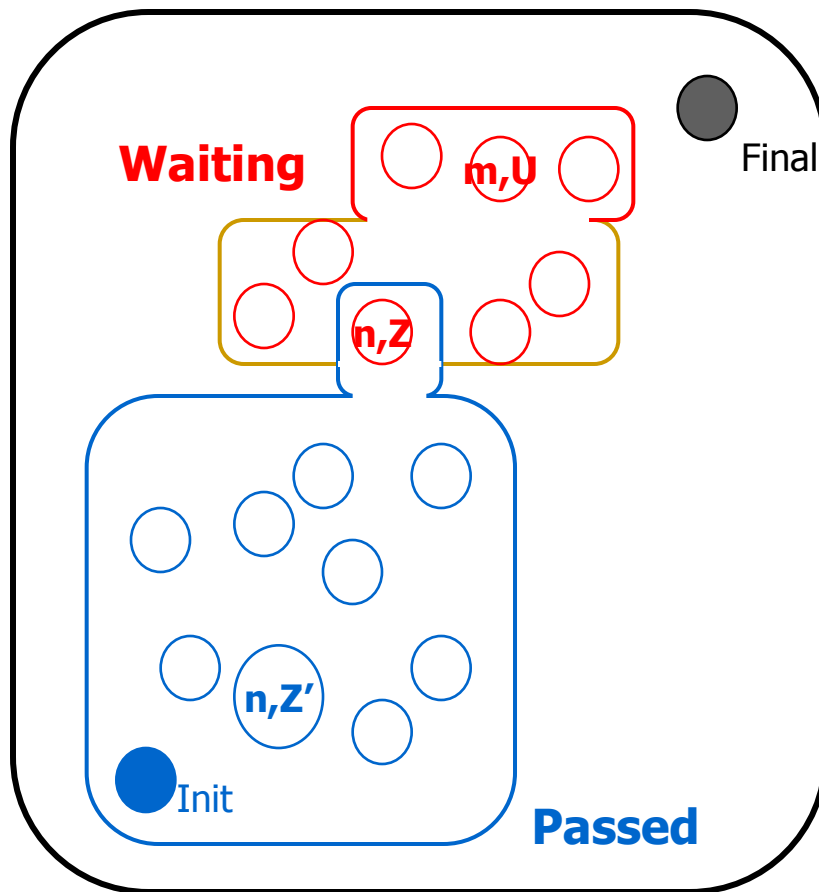
UNTIL **Waiting** $= \emptyset$

or

Final is in **Waiting**

Forward Reachability

Init \rightarrow Final ?



INITIAL **Passed** $:= \emptyset$;
Waiting $:= \{(n_0, Z_0)\}$

REPEAT

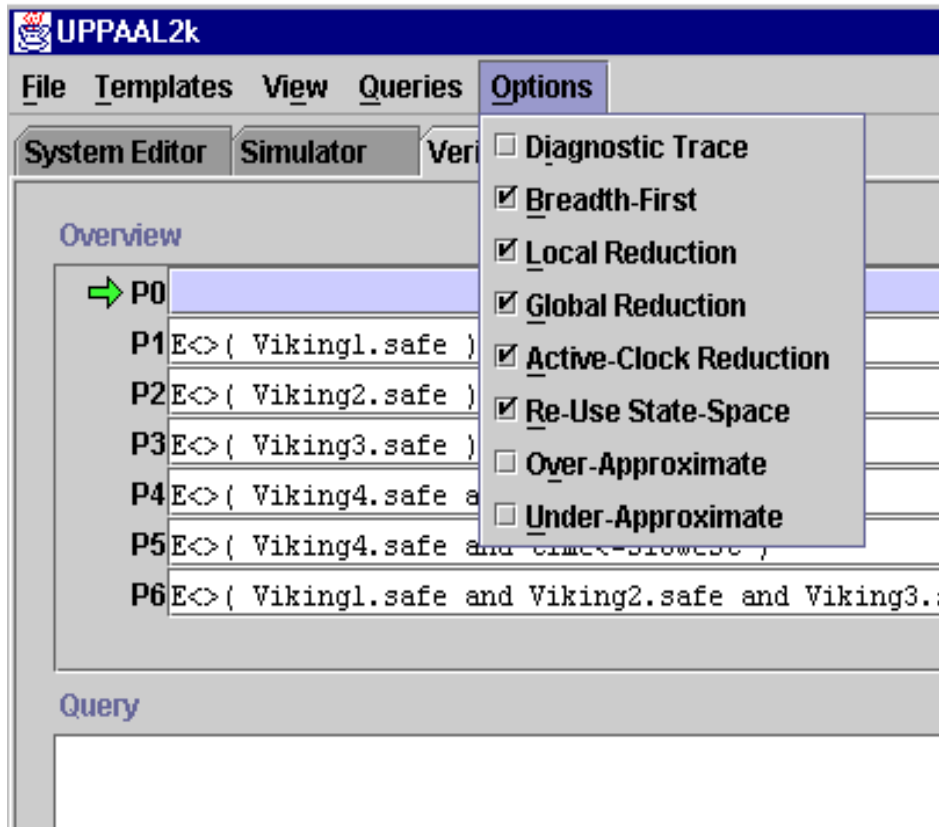
- pick (n,Z) in **Waiting**
- **if** for some $Z' \supseteq Z$
 (n,Z') in **Passed** then **STOP**
- **else** /explore/ add
 $\{ (m,U) : (n,Z) \Rightarrow (m,U) \}$
to **Waiting**;
Add (n,Z) to **Passed**

UNTIL **Waiting** $= \emptyset$

or

Final is in **Waiting**

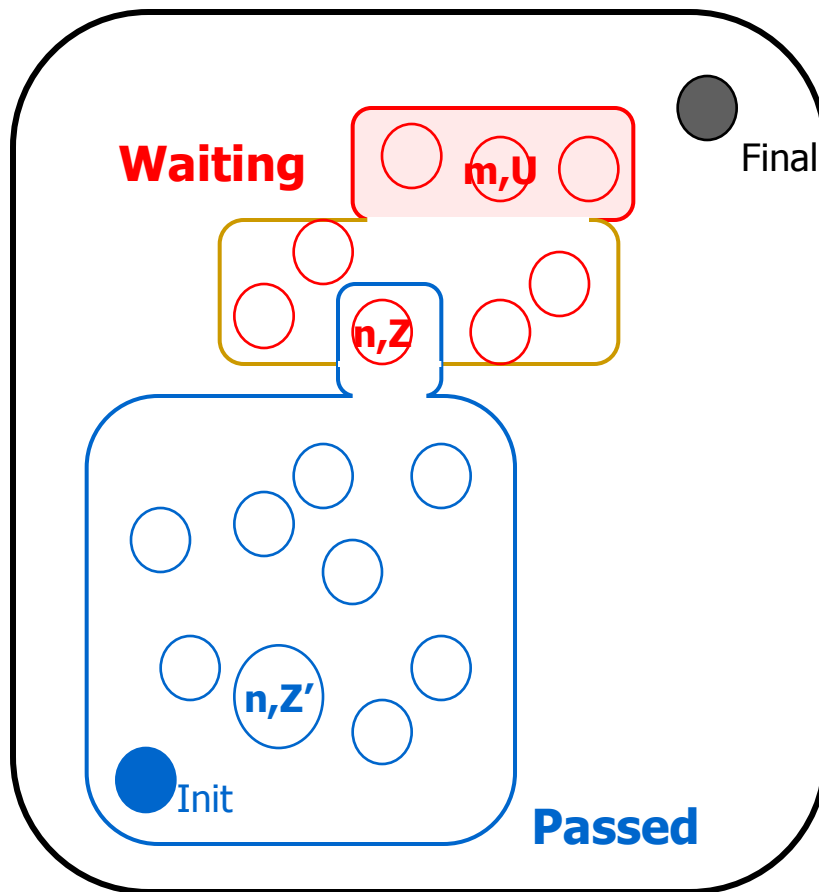
UPPAAL Verification Options



- Diagnostic Trace
- Breadth-First
 - Depth-First
- Local Reduction
- Global Reduction
- Active-Clock Reduction
- Re-Use State-Space
- Over-Approximation
- Under-Approximation

Forward Reachability

Init \rightarrow Final ?



INITIAL **Passed** $:= \emptyset$;
Waiting $:= \{(n_0, Z_0)\}$

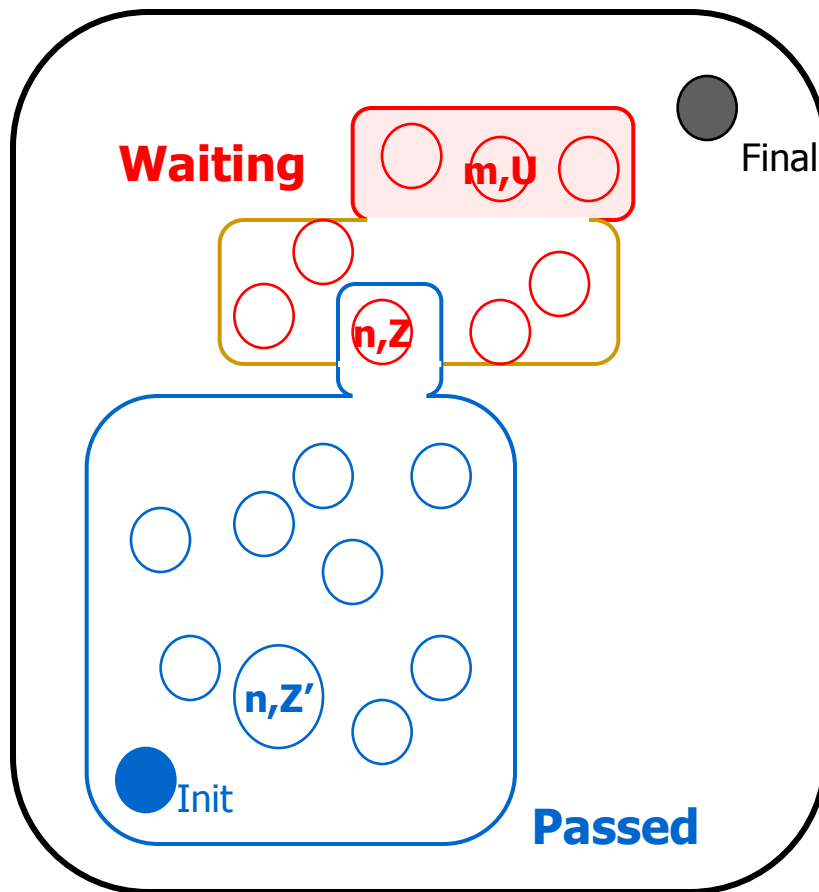
REPEAT

- pick (n, Z) in **Waiting** location zone
- **if** for some $Z' \supseteq Z$
 (n, Z') in **Passed** **then STOP**
- **else** /explore/ add
 $\{ (m, U) : (n, Z) \Rightarrow (m, U) \}$
to **Waiting**;
Add (n, Z) to **Passed**

UNTIL **Waiting** $= \emptyset$
or
Final is in **Waiting**

Order of Exploration

Depth-First vs Breadth-First



Depth-First

Waiting stored on *stack*

Breadth-First

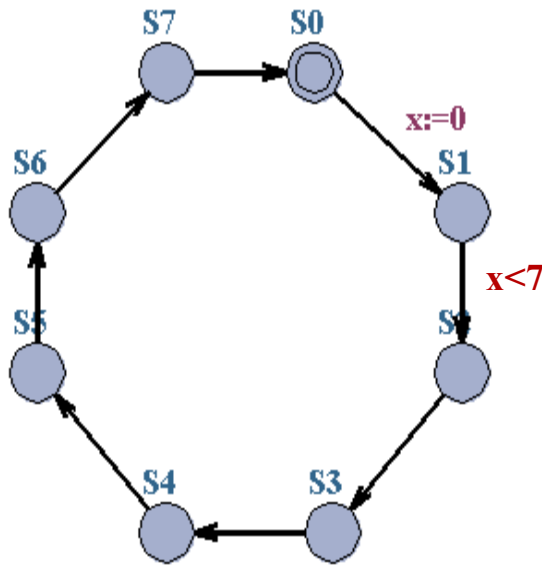
Waiting stored in *queue*

In most cases **BF** is preferred because it allows for generation of "shortest" traces.

DF is useful in situations when reachability may be concluded without generating the full state-space. Easy computation of traces.

Representation of Symbolic States

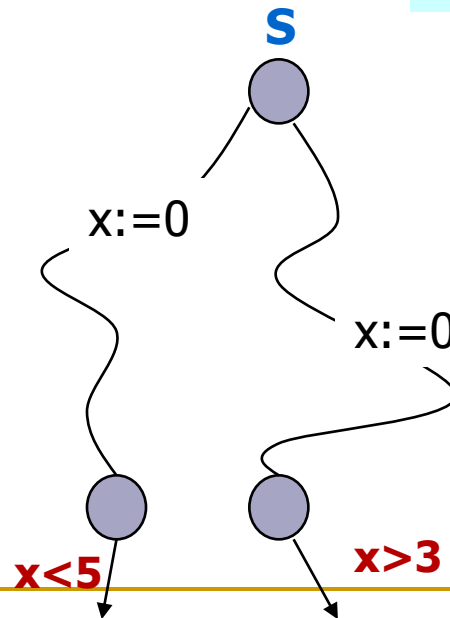
(In)Active Clock Reduction



x is only **active** in location **S1**

Definition

x is **inactive** at **S** if on all paths from **S**, x is always reset before being tested.

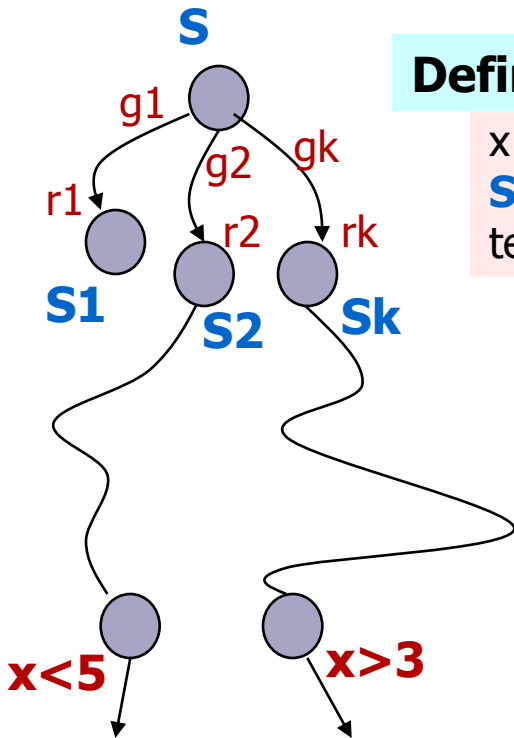


Representation of Symbolic States

Active Clock Reduction

Definition

x is **inactive** at S if on all paths from S , x is always reset before being tested.

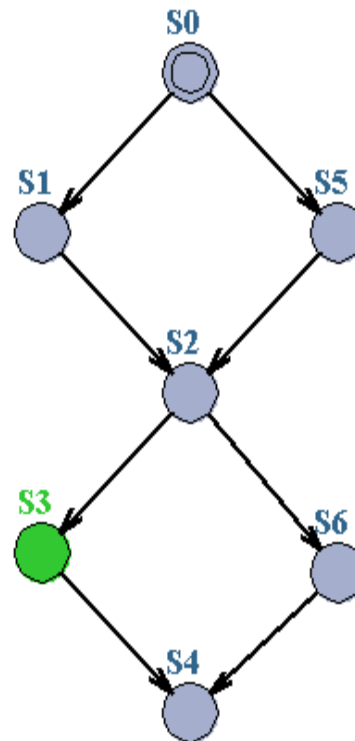


$$\begin{aligned} Act(S) = & \\ & \bigcup_i Clocks(g_i) \\ & \cup \\ & \bigcup_i (Act(S_i) - Clocks(r_i)) \end{aligned}$$

Idea: We only need to save constraints on active clocks.

When to Store Symbolic State

Global Reduction

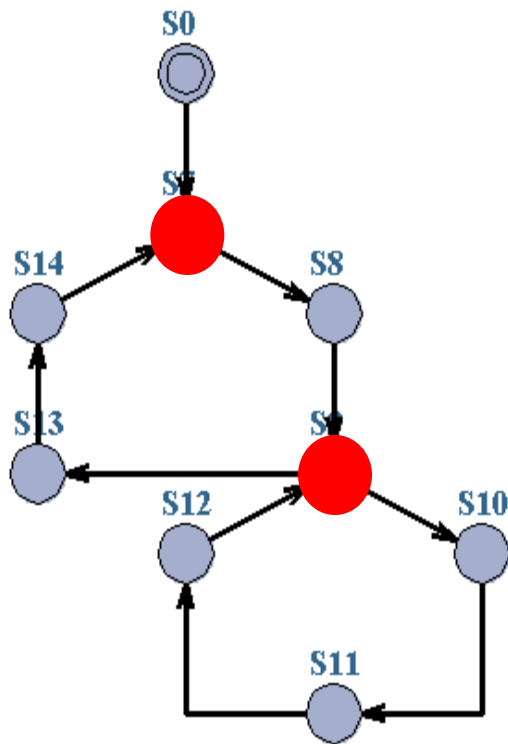


However, the **Passed** list is useful for efficiency.

If there are No Cycles: The **Passed** list is not needed for *termination*.

When to Store Symbolic State

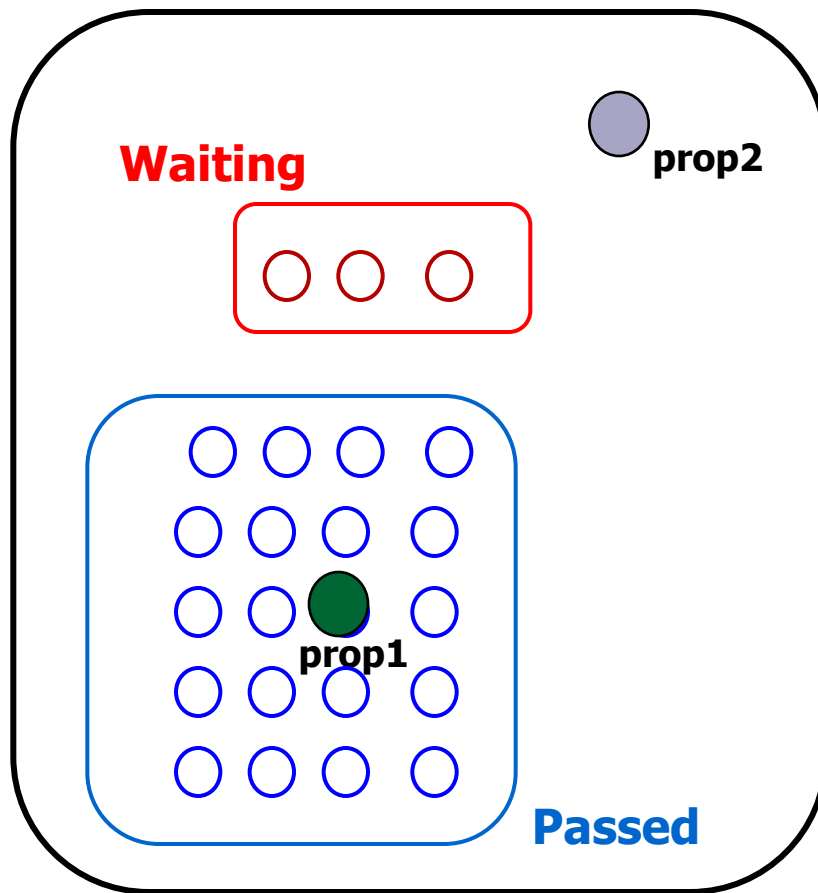
Global Reduction



Cycles:

Only symbolic states involving loop-entry points need to be saved on **Passed** list.

Reuse State Space



A[] prop1

A[] prop2

A[] prop3

A[] prop4

A[] prop5

.

.

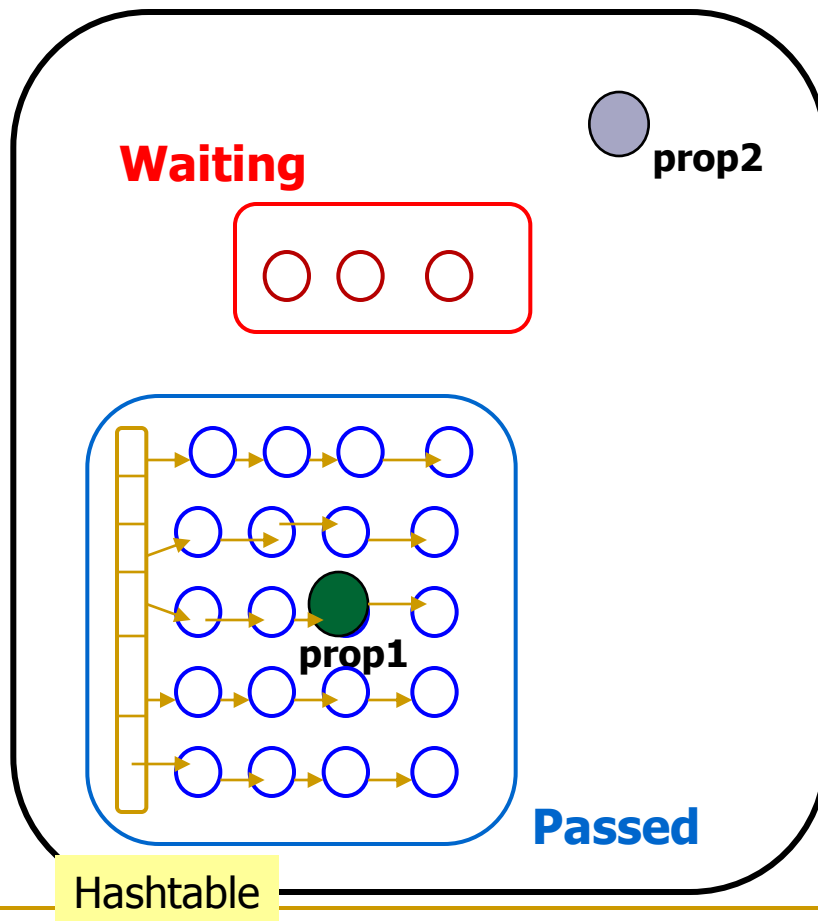
.

A[] propn

Search
in existing
Passed
list before
continuing
search.

Which order
to search?

Reuse State Space



A[] prop1

A[] prop2

A[] prop3

A[] prop4

A[] prop5

.

.

.

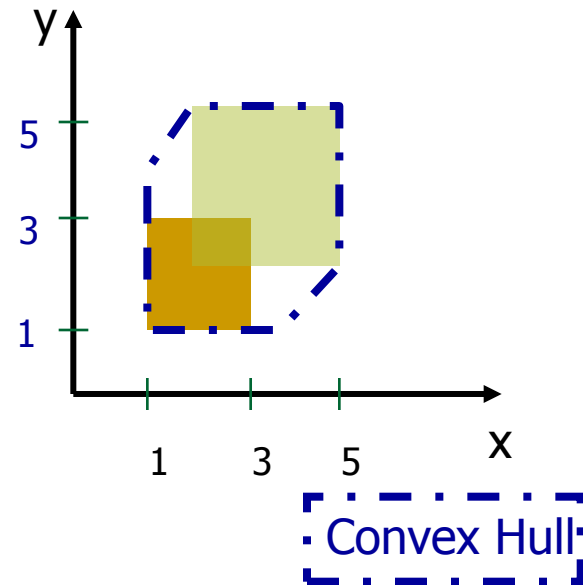
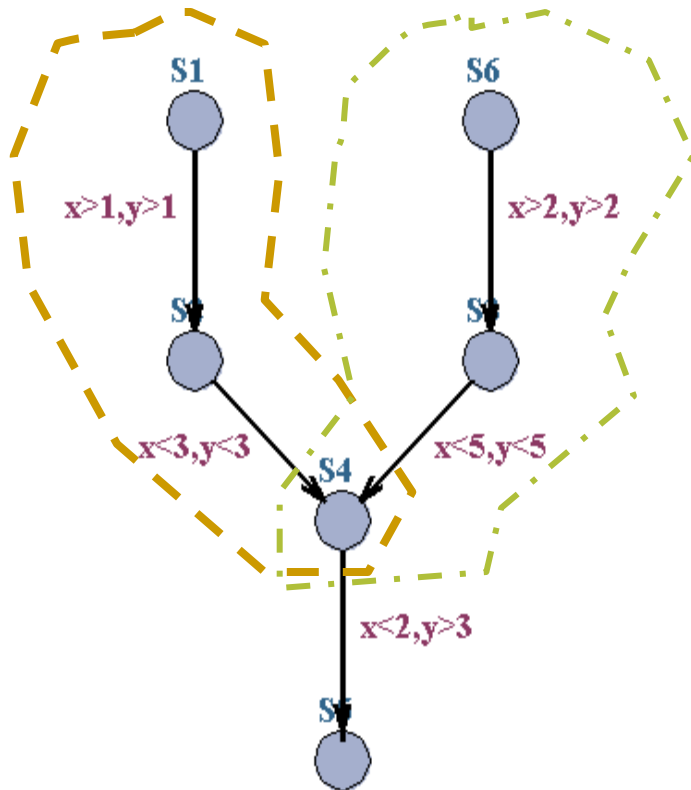
A[] propn

Search
in existing
Passed
list before
continuing
search.

Which order
to search?

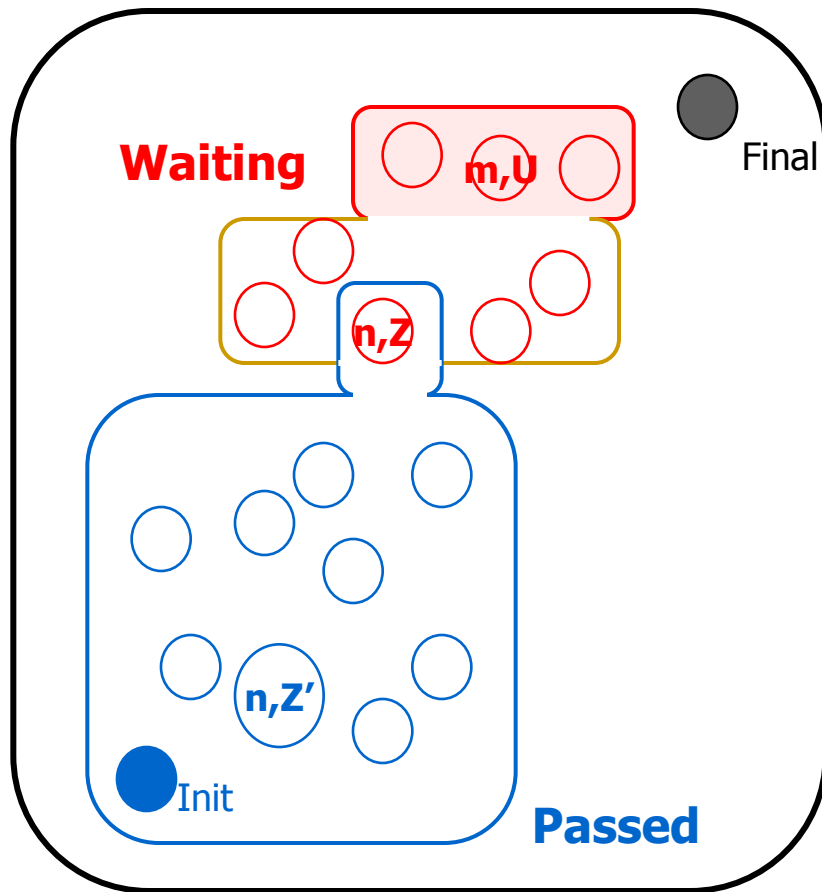
Over-Approximation

Convex Hull



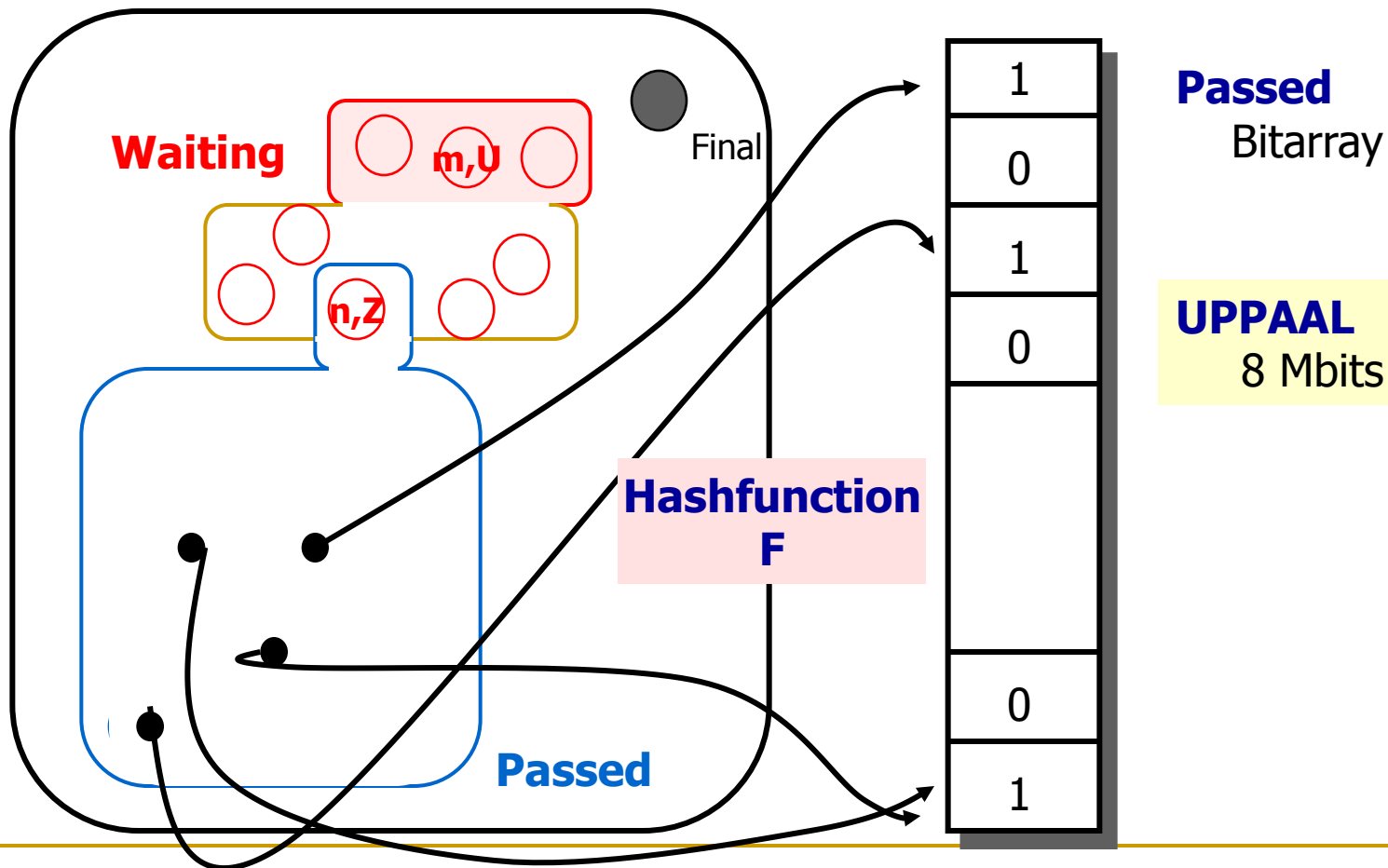
Under-Approximation

Bitstate Hashing



Under-Approximation

Bitstate Hashing



Bitstate Hashing

```
INITIAL Passed :=  $\emptyset$ ;  
         Waiting := {(n0,Z0)}  
  
REPEAT  
  - pick (n,Z) in Waiting  
  - if for some  $Z' \supseteq Z$   
    (n,Z') in Passed then STOP  
  - else /explore/ add  
    { (m,U) : (n,Z) => (m,U) }  
    to Waiting;  
    Add (n,Z) to Passed  
  
UNTIL Waiting =  $\emptyset$   
      or  
      Final is in Waiting
```

Passed(F(n,Z)) == 1

Passed(F(n,Z)) := 1

Options in UPPAAL 3.4.9

- **Search Order:** perform (symbolic) state-space exploration in breadth-first or depth-first order.
- **State Space Reduction:** determines if control-structure analysis should be performed to reduce the space requirements during verification. Possible values are *none*, *conservative* (control-structure reduction saving all non-committed states and all loop-entry points), and *aggressive* (control-structure reduction saving only loop-entry points). Note that there is normally a tradeoff between space requirement and speed.
- **State Space Representation:** determines how the state-space should be represented in the model checker. Possible values are *DBM* (Difference Bound Matrices), the *Compact Data Structure*, *Under Approximation* (by bit-state hashing), and *Over Approximation* (by convex-hull approximation).

Options in UPPAAL 3.4.9

- **Clock Reduction:** activates (in-)active clock reduction.
- **Reuse State-Space:** instructs, the verifier to (whenever possible) reuse the generated portion of the state-space when several properties of the same system are checked.
- **Diagnostic Trace:** generates a trace (if there is one) that shows how the checked property is (or is not) satisfied. The trace is automatically loaded into the simulator. The possible values are *none*, *some*, *shortest* (to generate an trace with minimum number of transitions), and *fastest* (to generate a trace with the shortest accumulated time delay).

Options in UPPAAL 3.4.9

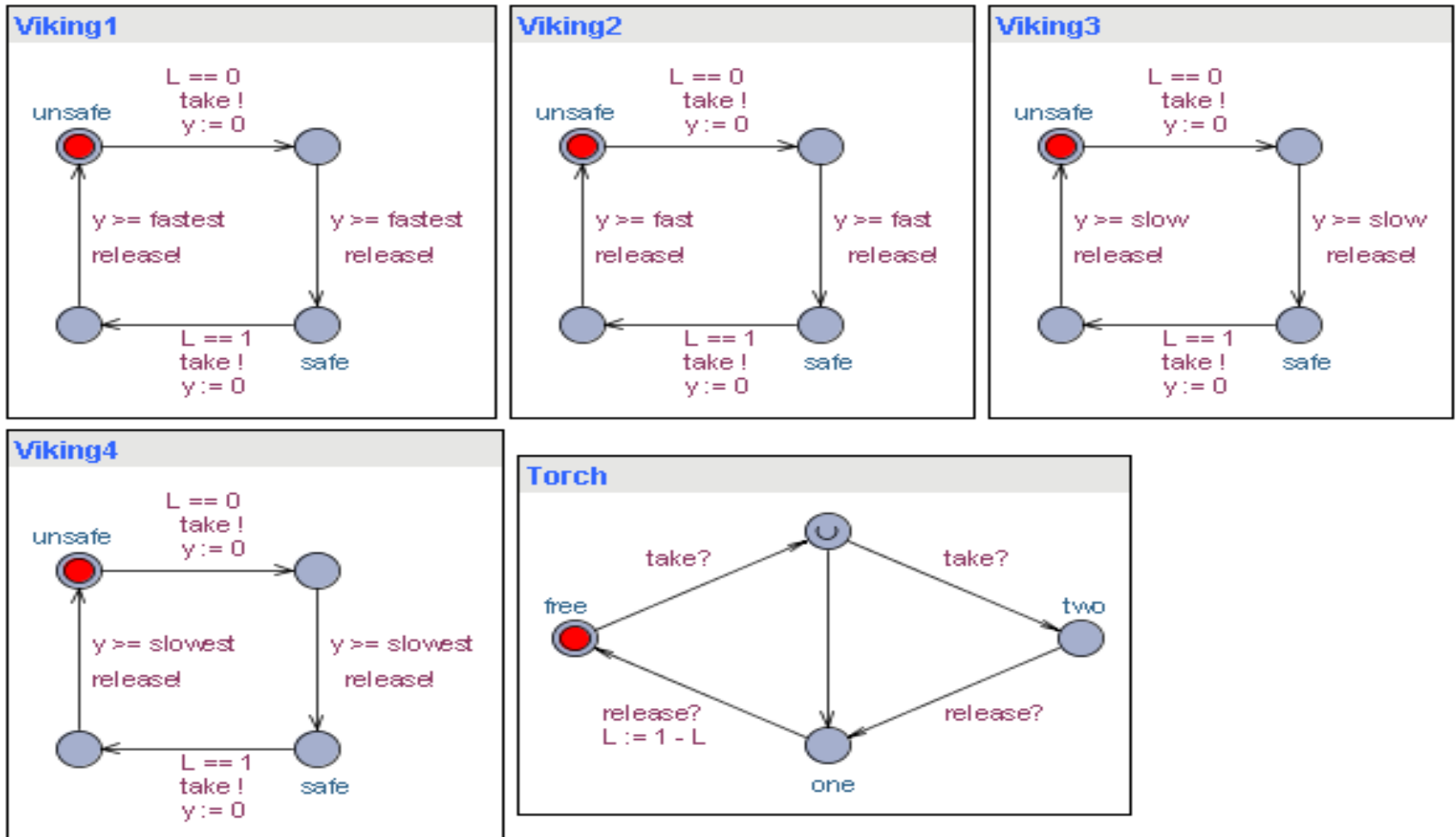
- **Note:** there are certain dependencies restricting how the various options can be combined. Activating one option may therefore deactivate other options. The Options menu is always updated to show the currently activated options.
 - **More Information:** control-structure reduction and compact data structure is described in the paper:
Efficient Verification of Real-Time Systems: Compact Data Structure and State-Space Reduction, Kim G. Larsen, Fredrik Larsson, Paul Pettersson and Wang Yi. In Proceedings of the 18th IEEE Real-Time Systems Symposium, pages 14-24. San Francisco, California, USA, 3-5 December 1997.
-

Example: Vikings' Problem

- Four vikings are about to cross a damaged bridge in the middle of the night.
 - The bridge can only carry two of the vikings at the time and to find the way over the bridge the vikings need to bring a torch.
 - The vikings need 5, 10, 20 and 25 minutes (one-way) respectively to cross the bridge.
 - Does a schedule exist which gets all four vikings over the bridge within 60 minutes? What is the minimum time required to get all four vikings over the bridge?
-

Example: Vikings' Problem Model

- Model the four vikings as four processes, and the torch as a single process (see bridge.xml).



Example: Vikings' Problem

- Four vikings are about to cross a damaged bridge in the middle of the night.
- The bridge can only carry two of the vikings at the time and to find the way over the bridge the vikings need to bring a torch.
- The vikings need 5, 10, 20 and 25 minutes (one-way) respectively to cross the bridge.
- **Question:** What is the minimum time required for all four vikings to safely cross the bridge?
- **Answer:** 60 minutes: use E<>(Viking1.safe and Viking2.safe and Viking3.safe and Viking4.safe) with the additional Option:
Diagnostic Trace: Fastest.

UPPAAL Example

- Wolf, goat, cabbage, farmer problem
 - The farmer needs to move the wolf, goat, and cabbage from one side of the river to the other side. The farmer can only carry one passenger.
 - If the wolf and goat are left alone, the wolf will eat the goat. If the goat and cabbage are left alone, the goat will eat the cabbage.
 - How can the farmer transport the passengers without allowing one to be eaten?

Drag out

Enabled Transitions

Farmer --> Boat

Next

Reset

Simulation Trace

unsafe, unsafe, unsafe, free, -)

Next

Replay

Save

Auto

Fast

Drag out

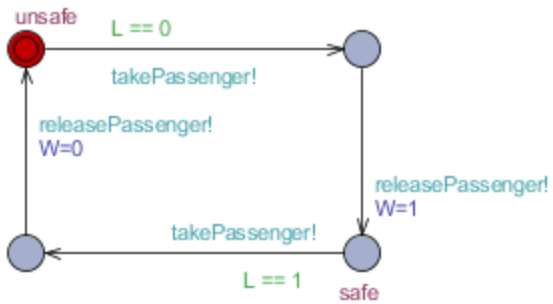
L = 0

W = 0

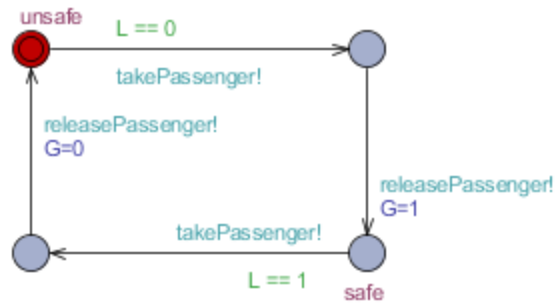
G = 0

C = 0

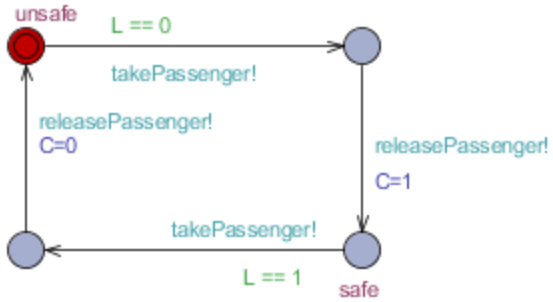
Wolf



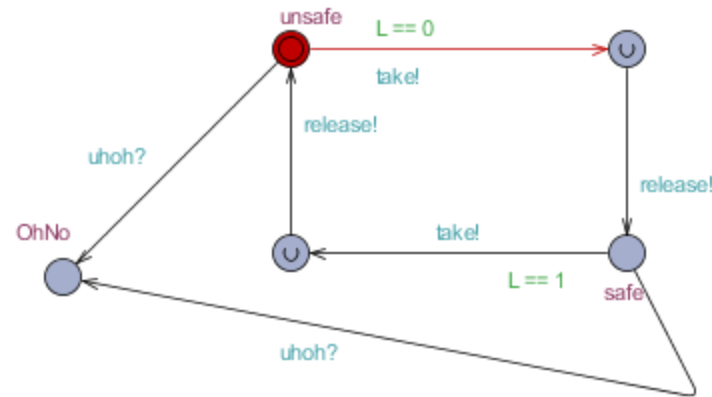
Goat



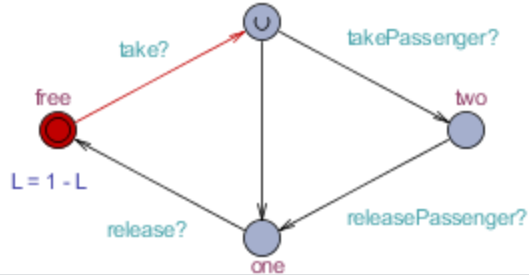
Cabbage



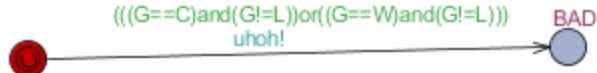
Farmer



Boat

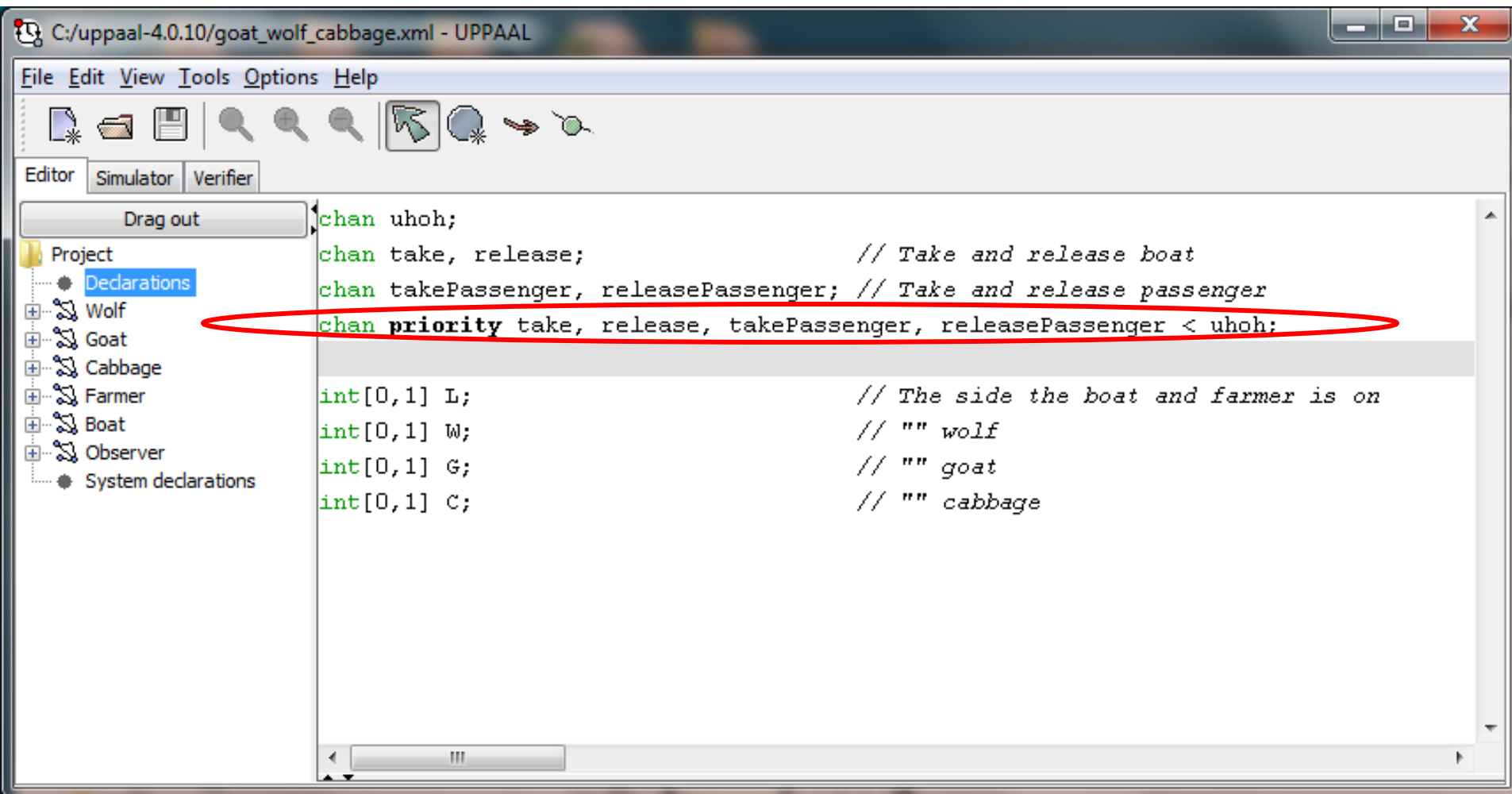


Observer

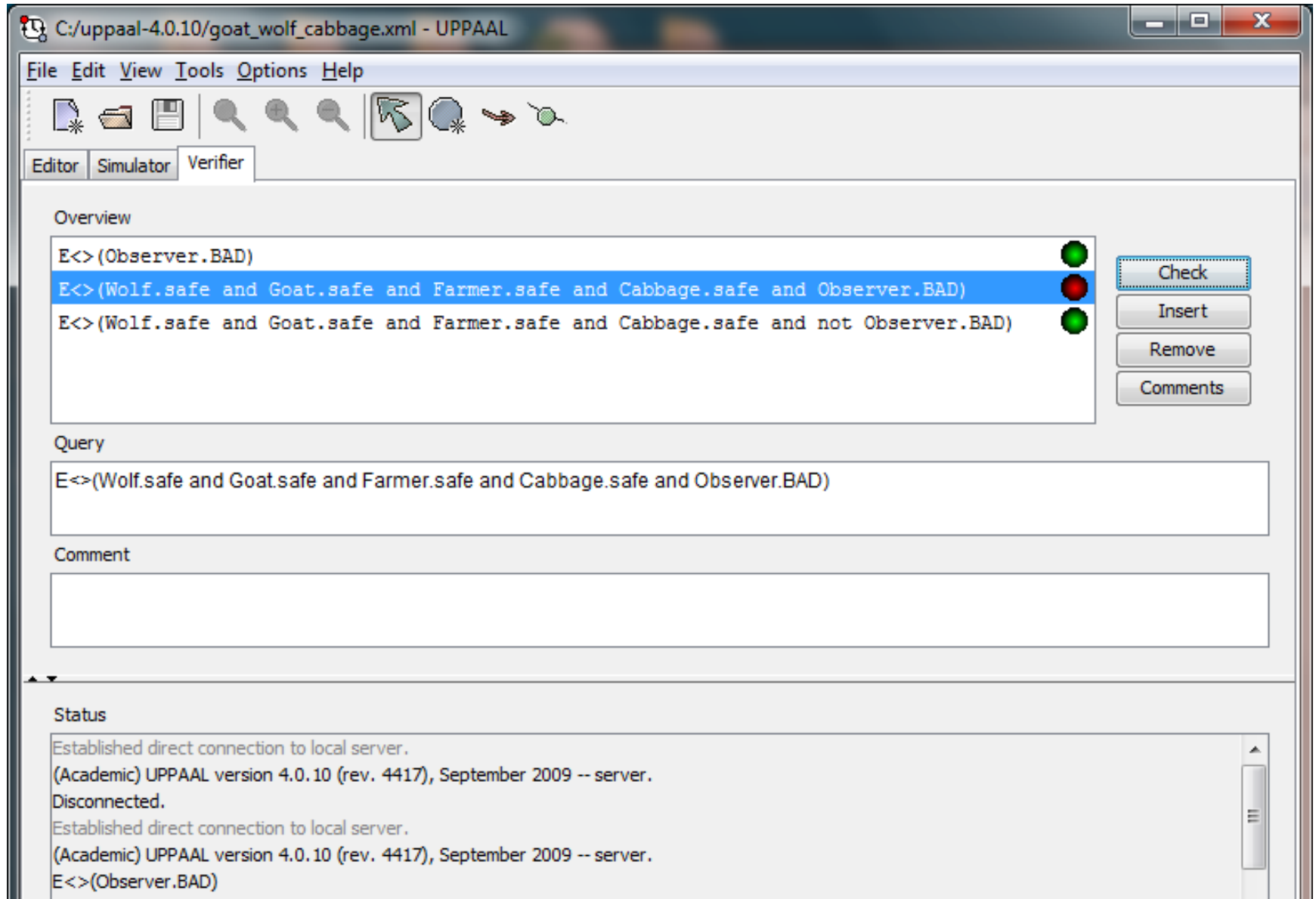


Wolf Goat Cabbage Farmer Boat Observer

UPPAAL Model



UPPAAL Model



Summary

- **Next Time: SPIN**