1. a) (RISC) Reduced Instruction Set Computing - reduces instruction set for quicker processing by using simple instructions but more of them

b) (CISC) Complex Instruction Set Computing - full instruction set, provides all needed capabilities. - complete task in as few lines of assembly as possible

c) (Vector Instructions) SSE provided help with floating point instruction types while MMX did integer. SSE providing integer instructions in a later release.

d) (Condition Codes) Requires less compare and test instructions when converting to assembly, but provides extra complexity to both the programmer and the compiler

e)(Stack) Data type that is easy to store large quantities of data in. LIFO - last in first out, can only access most recently entered data

f) (iRAM) Intelligent RAM - tried to find a better tradeoff between cost and performance by integrating DRAM on the chip and eliminating the need for a redundant static memory cache.

2. (argue against > 8 registers) Performance improvement would be comparable to a logarithmic function, so performance improvements would be minor in most situations,
while cost would increase drastically, as well as space required.

3. (what does linker do) The linker takes the code from the compiler, and replaces variables with specific memory addresses in order to create an executable.

4. (movl 8(%ebp), %edx) copies value of ebp + offset 8 into edx

5. (what is SetX instructions used for) Sets environment variables for the currently logged on user or the machine.

6. (why goto/jmp considered poor programming) Goto/jmp statements are dangerous to use in code because of how easily they can cause unexpected issues and the difficulty of
debugging such an issue.

7. (translating loops to do-while change chip architecture)

8. (unconditional branch incur no overhead but conditional do) An unconditional branch always executes if it is reached, while a conditional branch has to check a set of parameters before execution.

9. (2 ways switch statements is improved by compilers) If the switch has a dense range of case expressions, then the switch is turned into a jump table which is very quick and easy to execute.
If its impossible to use a jump-table then the compiler will reorder the comparisons in order to use a binary search.

10. (AMD-64 vs Itanium debate) AMD retained all backwards compatibility while providing specifications for 64 bit machines. Itanium is based on instruction-level
parallelism which made Itanium very inefficient with old x86 applications. Due to the lack of backwards compatibility, AMD made leaps in
the computing market while Itanium ended up with a very specific userbase (In 2009, HP had over 95% of the server market share).