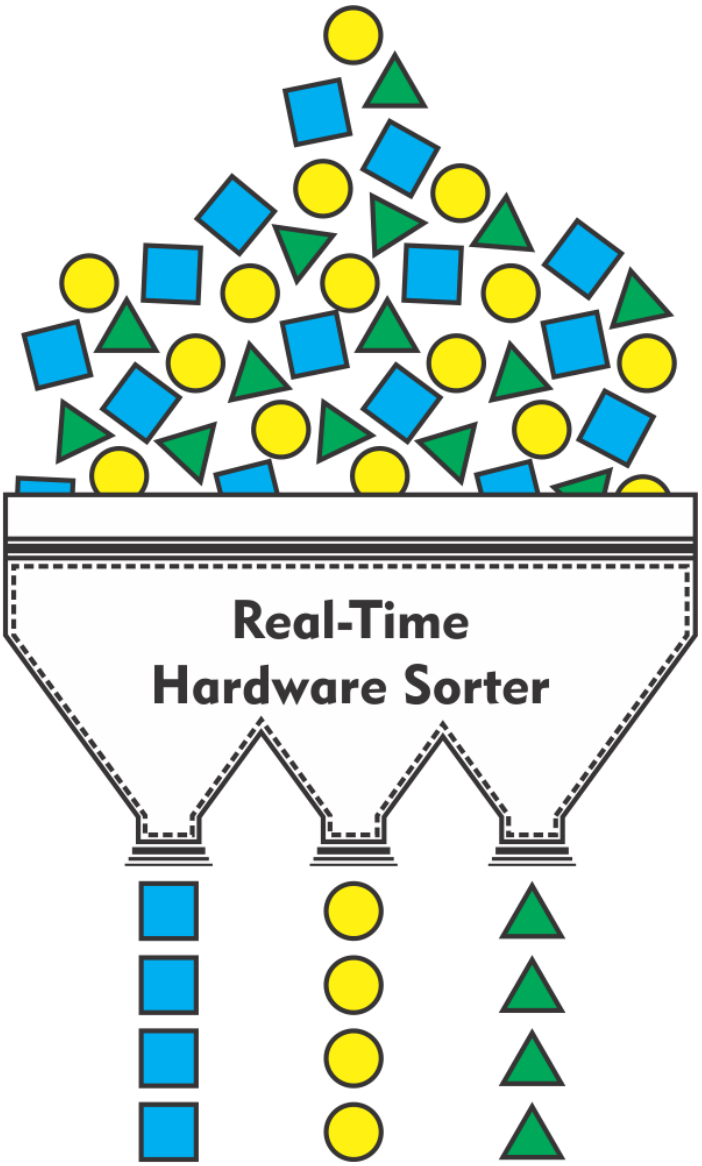
Iran University of Science and Technology

Hardware description of Real Time Hardware Sorter (RTHS)



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Introduction

Sorting is a fundamental computation task used in various computer science applications. In high-performance applications like big data processing, it is critical to sort input data quickly and with high efficiency. While many software algorithms have been proposed for this purpose, the increasing computational demands and the need to execute programs on many-core platforms like Network on Chip systems have necessitated the development of new parallel algorithms for sorting data on parallel platforms.

Conventional sorting networks are not suitable for this purpose. Therefore, new parallel algorithms based on networks, such as bitonic and odd-even sorting networks, have been proposed to take advantage of the features of high-performance platforms and increase performance. FPGA-based solutions have enabled the design of specific hardware for sorting, resulting in efficient hardware dedicated solely to the task of sorting data.

The biggest challenge in designing hardware sorters is to create a high-performance sorter that can handle the maximum number of records and sort them in minimal time. However, this is a significant challenge because increasing the number of input records in the sorter requires more hardware resources, which are limited due to the limited number of resources in the FPGA chip. Additionally, the sorting module is only one of several components in the system, so minimizing its size is essential.

Our proposed method is a novel hardware solution for data sorting using a multi-dimensional sorting algorithm. The project is divided into two main parts:

1. Designing the scalable Bitonic sorting network,
2. Designing and implementing the Real-Time Hardware Sorter (RTHS).

In this GitHub project, we have endeavored to simplify the RTHS design code to enhance its comprehensibility. Accordingly, we have described the hardware sorter that sorts 16 input records with a 16-bit data width.

The subsequent sections of this document will detail the bitonic sorting network and the RTHS design.

Bitonic sorting network Design

Our aim was to identify the similarities in the sorting network and program the relevant modules to enable scalability across different simulations, without the need to modify the code. Figure 1 illustrates the Bitonic sorting network for 8 input records.

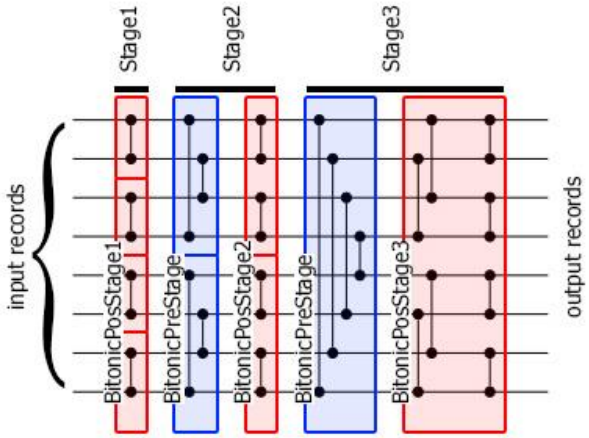

Figure 1 simple 8 input Bitonic sorting network.

We created a network consisting of five modules. The "BitonicPreStage" modules represent the iterative parts of the network that can be utilized in subsequent stages, while the "BitonicPosStageX" modules describe the remaining part of the network. In each stage, the corresponding modules need to be employed.

Scaling up this network to accommodate 16 input records involves duplicating the Figure 1 network in parallel and adding the new "BitonicPreStage" and "BitonicPosStage4" modules in series. By doing so, we can create a 16-input Bitonic network.

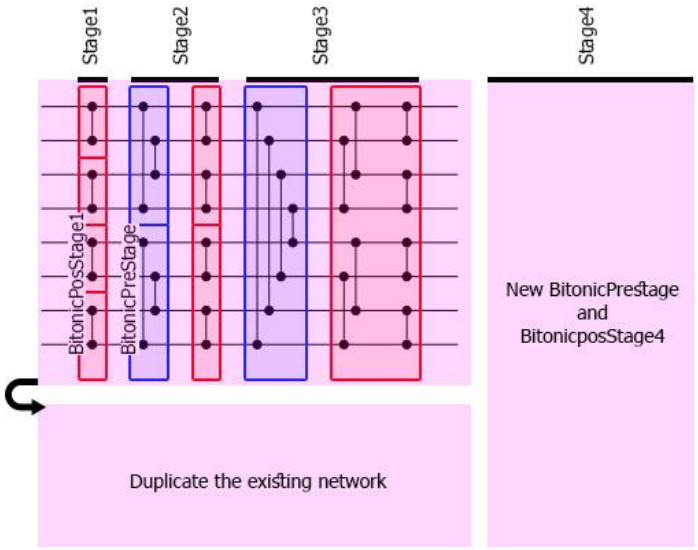

Figure 2 scalability.

Main RTHS design

The main module of the system employs the Bitonic sorting network as its fundamental building block. The sorting process begins with the input records being entered into the sorter in the form of a one-dimensional array, which is then transformed into a 2D matrix. Each Bitonic sorting network receives one column of the 2D matrix for partial sorting simultaneously. The column and row of the matrix are then swapped, and the 2D matrix is transformed to the other dimension (from I to J and vice versa). This process constitutes one phase of the sorting process.

After six phases, all the records of the 2D matrix have been sorted. The 2D matrix is then flattened by dimension order and sent to the output.

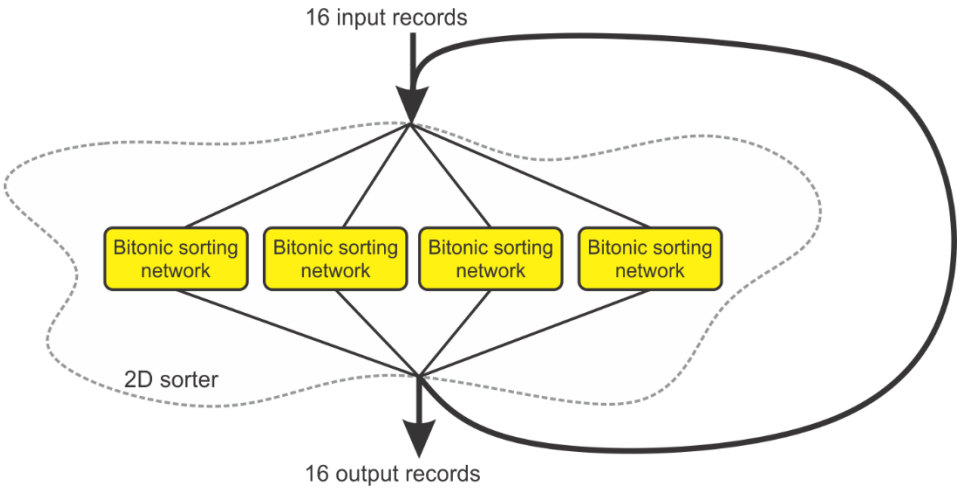

Figure 3 schematic of proposed sorter.

Figure 3 shows the schematic of the basic idea of the proposed 2D sorter for sorting 16 input records. For getting the more information about this architecture, you can see the following paper: "RTHS: A Low-Cost High-Performance Real-Time Hardware Sorter, Using a Multidimensional Sorting Algorithm", doi: 10.1109/TVLSI.2019.2912554.

As mentioned above, this design consisted of 4 modules as follows:

Num	Name of module	Description
1	Bitonic sorting networks	We used 4 bitonic sorting network to sort 16 input records.
2	2D switch	Also called it implicit switch. It has a task of turning the 2D matrix of records that is sorted in Bitonic sorting networks.
3	temporary registers	They located in the main module and have task of storing the input record in the first phase and output of the 2D switch in the others.
4	control unit	Set the Direction signals and Ready signal at the end of the process.