Sensor Signal Linearization Techniques: A Comparative Analysis

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***Abstract*—A comparative analysis of different linearization techniques for sensor signals is presented. Several solutions in the analog, digital and mixed-signal domains are considered. In each domain, a case study consisting on a realization on silicon developed by the authors is presented. The analysis can help designers to choose the linearization technique best suited for a given application.**

I. INTRODUCTION

Sensors usually exhibit nonlinear transfer characteristics, requiring linearization. Typical nonlinear characteristics are exponential (*e.g.* thermistors [1]), sinusoidal (*e.g.* GMR sensors [2]), or tangential (*e.g.* LMTs [3]). The choice of an adequate linearization method is critical for the overall performance of the system. Several techniques have been proposed to linearize sensor characteristics. They can be classified into three groups: analog, digital, and mixed-mode techniques. In the first case, analog signal processing by passive or active elements is employed to linearize the sensor output. The analog block achieving such linearization has a characteristic that approximates the inverse of that of the sensor. Thus, for instance, logarithmic amplifiers are widely employed for interfacing sensors featuring exponential characteristics like thermistors [1]. The second group of techniques consists in the digital linearization carried out after A/D conversion of the sensor output. A common technique in this group is the use of a ROM look-up table. The third group of techniques achieves linearization in the A/D conversion step, employing a nonlinear A/D converter that has a nonlinear characteristic such that the nonlinearity of the sensor output is removed; this way, A/D conversion and linearization are performed jointly using a single physical unit.

In this paper we present a comparative analysis of these linearization techniques. Case studies are extracted from industrial design projects developed by the authors in recent integrated sensor interfaces.

II. ANALOG LINEARIZATION TECHNIQUES

The use of analog circuits with passive and/or active components to linearize sensor characteristics is the oldest approach. They are widely used for thermistors. The first proposals often employ a Wheatstone bridge [1], where a thermistor is placed in one of the arms of the bridge. A very popular technique is using along with the thermistor a passive resistor and to excite it by a voltage source [4]. This way, current flowing through it can be made proportional to absolute temperature (PTAT). Alternatively, astable or monostable multivibrator bridges can be used [5]. Another related technique is the use of temperature-to-frequency converters based on a single astable multivibrator [6]. A fourth method, also very useful for other sensors with exponential characteristics, is the use of a logarithmic network or amplifier. Another alternative consists in a relaxation oscillator that operates comparing the outputs of a RC network and a resistive voltage divider circuit that contains the thermistor [7]. The result of the comparison triggers a timing network, which controls the charge or discharge of the RC circuit in a feedback loop.

Several nonlinear analog circuits like multipliers or dividers have been employed to linearize second-order and higher-order sensor models [8, 9]. Many other less common methods have been proposed based on nonlinear analog circuits, like the use of neural networks [10] or radial basis function networks [11].

A simple analog linearization approach readily found in commercial interfaces for bridge sensors is based on the variation of the bridge bias voltage or current according to the output signal using feedback loops [12]. For many silicon sensors, this kind of nonlinearity correction may reduce sensor nonlinearity by an order of magnitude.

A. Case Study: Analog PWL characteristics

A low-cost analog linearization method is described below. It is a representative example that illustrates many of the advantages and limitations of this kind of techniques. Like in other analog linearization techniques, the idea is to get an analog circuit whose input-output transfer characteristic is matched to the inverse of the sensor characteristic. This idealistic situation is difficult to achieve in practice. A more common approach is to implement a piecewise linear (PWL) approximation to the inverse of the sensor characteristic, leading to a much simpler implementation. An adequate choice of the number of segments, the slopes of such segments, and the corner voltages, allows achievement of a

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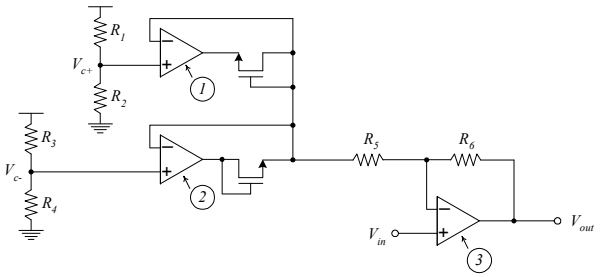
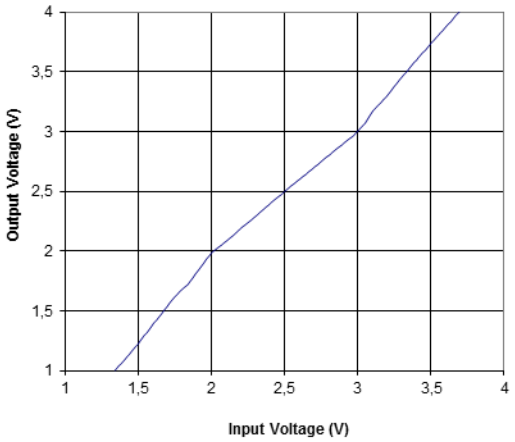


(a)



(b)

Figure 1. (a) Three-segment linearization (b) Measurement results

given accuracy. A tradeoff between accuracy and complexity exists as both factors increase with the number of segments.

Figure 1 shows the analog circuit and measurement results corresponding to a 3-segment PWL characteristic. It can be applied when the sensor characteristic is symmetrical and linear for low signal values, but nonlinear when signal values are higher. This situation is quite common in practice. In the middle range between corner voltages V_{c-} and V_{c+}, the analog linearization block is transparent. Outside this range, the slope of the outer segments is adjusted to minimize the RMS error in the linearized output. In the particular case of the PWL function shown, it is assumed that the sensor features a loss of sensitivity for extreme values, which is compensated by a slope greater than 1 in the outer segments. The circuit of Fig. 1 is based on super-diodes, each one consisting on a diode-connected MOS transistor in the negative feedback loop of an op-amp. When $V_{c-}<V_{in}<V_{c+}$, the voltage at the non-inverting input of op-amp #1 is higher than voltage at its inverting input, so the output of the op-amp tends to saturate in the positive direction. This turns off the diode-connected transistor at this output, opening the feedback loop. In a similar way, the output voltage of op-amp #2 tends to saturate in the negative direction as voltage at its non-inverting input terminal is lower than voltage at its inverting input terminal. This also turns off the diode-connected transistor at its output, and opens the feedback loop. Therefore, in the middle range of input voltages, super-diodes are not influencing the circuit, and op-amp #3 behaves like a simple voltage follower. When $V_{in}<V_{c-}$, op-amp #1 is still in open loop, but op-amp #2 is now in closed loop as its diode-connected transistor is on. In this case, this super-diode acts like a voltage follower and the common output node of the super-diodes is set to V_{c-}. In this case op-amp #3 acts like a non-inverting amplifier, and the input-output characteristic becomes:

$$V_{out} = -V_{c-}\left(\frac{R_6}{R_5}\right) + V_{in}\left(1+\frac{R_6}{R_5}\right) \quad (1)$$

achieving a slope set by R_5 and R_6. In a similar way, when $V_{in}>V_{c+}$, op-amp #2 is in open loop whereas op-amp #1 is in closed loop. The common output node of the super-diodes is set to V_{c+}, and the input-output characteristic becomes:

$$V_{out} = -V_{c+}\left(\frac{R_6}{R_5}\right) + V_{in}\left(1+\frac{R_6}{R_5}\right) \quad (2)$$

This approach can be generalized to implement PWL transfer functions of more segments, using for each corner in the PWL function a super-diode biased by the corner voltage.

Figure 1(b) shows the measured PWL characteristics of the circuit of Fig. 1(a) fabricated in a 2-µm CMOS process. The slopes and corner voltages of the segments are programmed in the integrated circuit via adjustment of external resistances, and their values are optimized by a software tool during calibration to minimize errors. Corner voltages are V_{c-}= 2 V and V_{c+}= 3 V. The total silicon area is approximately 0.4 mm^2.

III. DIGITAL LINEARIZATION TECHNIQUES

With the dominance of digital VLSI circuits and digital signal processing, linearization techniques in the digital domain are nowadays the most used ones, particularly when high performance is demanded. Such techniques achieve as much accuracy as required by the designer, at the expense of more circuit complexity and/or more processing time. Another typical benefit is programmability of the linearization circuit or algorithm, which eases the implementation of general-purpose sensor interfaces able to process signals from different kinds of sensors. These universal interfaces are becoming very common in industry due to their wider market.

The most common digital linearization is based on the storage of a "look-up table" (LUT) in a ROM memory that contains in each entry (row) a digital input value and its corresponding linearized digital output [3]. The table is typically acquired by direct measurement of the sensor. An advantage of this approach is that it is general, *i.e.*, it can linearize any kind of nonlinear sensor dependence, monotonic or not. However, when high accuracy is required, large LUTs are required, increasing silicon area. Alternatively fewer data points can be interpolated (*e.g.*, using piecewise linear, piecewise polynomial or spline interpolation) [13], but then intensive digital processing is necessary. This method is a tradeoff between processing time and silicon area, a common situation in digital linearization techniques. Other methods for reduction of the required memory size can also be adopted. For instance, if the sensor characteristic is symmetrical, only half of it needs to be stored. The reconstruction of the output then also involves the detection of the sign of the input, which is applied to the output. Another elegant solution can be used

when the input words correspond to a binary-ordered sequence. In this case it is not necessary to store such input words, as they are implicitly coded in the memory address. This allows savings of typically about half the memory size. Further savings can be obtained if the stored data do not correspond to the digital output word, but just to the difference between the output word and the corresponding input word. Such procedure corresponds to the storage of the difference between the nonlinear response and a straight line instead of the nonlinear response itself. The number of bits required for such difference depends on the kind of nonlinearity and the resolution required, but storage requirements are typically reduced in a 50-80% for weak nonlinearities. Every time an input word is received, the output word is obtained by adding the corresponding stored value to the input. The shortcoming of this method is that linearization implies a table search plus an addition, increasing slightly the processing time.

Another technique only requires the digital storage of the coefficients of a polynomial approximation to the nonlinear function [14]. For instance, assuming that a third-order polynomial is a good approximation for the nonlinear function in the range of interest, *i.e.*,

$$V_{out}(V_{in}) \cong a_0 V_{in} + a_1 V_{in}^2 + a_2 V_{in}^3 \qquad (3)$$

only coefficients a_0, a_1 and a_2 need to be stored. The values of these coefficients are obtained during calibration. When dedicated hardware is not used to perform the linearization, large processing time may be required. Again, it represents a trade-off between silicon area and processing time.

Another option is the implementation of the LUT by combinational logic. This solution does not require a physical memory, so it is convenient in low-cost integrated circuits, where the need for an internal ROM may increase the price. This approach is particularly effective when the table size is not very large, because in this case the silicon area occupied by the combinational logic tends to be much lower than the size required for a ROM memory. Again a trade-off between silicon area and processing time appears, as gate count in the combinational logic can be decreased if more logic gate stages are allowed, which increases delay. However, a combinational circuit cannot be reconfigured, so it cannot be rearranged to linearize other types of nonlinear functions. The differential approach mentioned above is also useful with this technique. In this case the input word is applied to the input of the combinational circuit, and its output corresponds to the difference between the input and the linearized output. As the number of output bits is reduced, the gate count of the combinational circuit is much lower. As before, the final output is obtained by adding this difference with the input. The following case study further investigates this technique.

A. *Case Study: Differential Combinational Processing*

A digital linearization technique was employed by the authors to linearize a GMR sensor bridge. It was based on the method described in the last paragraph. As the resolution required was relatively low (9 bits) and the silicon area had a notable impact on the final cost, a combinational circuit was employed for linearization instead of a ROM memory. The circuit provides the difference between the input and the desired output, so the final word is obtained by adding the input and output. The stored values correspond to the difference between the *arcsin(x)* function (in the required angular range) and a linear function (see Fig. 2), which is coded in 6 bits. As the resulting curve is symmetrical, only positive values are implemented. The combinational linearization circuit was designed using VHDL as part of the ASIC design flow. It was synthesized using Synopsys, optimizing the area occupied. The silicon area employed for the linearization circuit in a 0.8-µm CMOS technology is 0.2 mm^2. The fabricated chip was thus able to linearize sensors with sinusoidal dependence with the parameter measured.

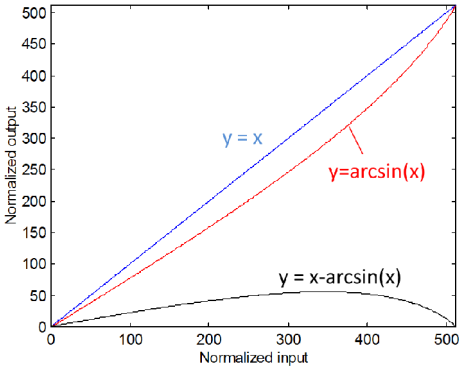


Figure 2. Linear and *arcsin(x)* function

IV. Mixed-Signal Linearization Techniques

It is also possible to perform linearization and A/D conversion in the same physical block, using a nonlinear ADC whose conversion characteristic is ideally matched to the inverse of the sensor characteristic. Such a nonlinear A/D conversion gets the best of each bit of resolution or, stated differently, requires the minimum number of bits for achieving a given resolution [2].

Several approaches for the implementation of a nonlinear A/D conversion exist. A well-known method is based on the ratiometric property of most A/D converters [15]. An external ratiometric reference voltage that is made dependent on the input voltage (typically by a simple resistive divider) is employed to achieve the required nonlinearity in the A/D conversion. The digital output voltage corresponds to the ratio of the input voltage to this input-dependent reference voltage. The resulting ADC can be regarded as an analog divider with digital output. Although this technique is simple, the correction of sensor nonlinearity is modest, much lower than that achieved by digital linearization techniques. The reason for the limited accuracy is that it is not possible to exactly implement the ideal A/D conversion characteristic, *i.e.*, the inverse of the sensor characteristic. An alternative approach that achieves better accuracy is the implementation of ADCs whose conversion characteristic is a PWL approximation to the inverse of the sensor characteristic [16]. The circuit can be equivalently seen as a PWL analog linearization circuit followed by a linear ADC. If the number and size of the PWL segments are properly chosen (*i.e.*, low RMS error with regard to the ideal A/D characteristic is achieved) high accuracy can be obtained by a relatively simple circuit. The following case study illustrates design issues of this kind of A/D converters.

A. Case Study: PWL ADC

The authors developed a PWL ADC to linearize the sinusoidal characteristic of a GMR sensor bridge used for contactless angle detection. The 16-segment PWL characteristic, approximating the *arccos(x)* function, can be seen in Fig. 3. The number of segments and position of the corner voltages was chosen to achieve a maximum fitting error with the ideal *arccos(x)* function of ±0.2%. The architecture chosen was a 4-bit flash stage employed in two conversion steps. In the first conversion step, a PWL ADC conversion takes place (using a resistor array in the Flash ADC with different resistance values to properly set the corner voltages of the PWL function), yielding the 4 most significant bits. Then a second linear ADC conversion step is performed using another resistor array with identical resistances, which provides the 4 less significant bits. Details of the operation of the circuit can be found in [2]. The circuit was implemented in a 2-µm CMOS process, achieving an overall error in the complete sensor interface of less than 1%. Area was 5 mm^2.

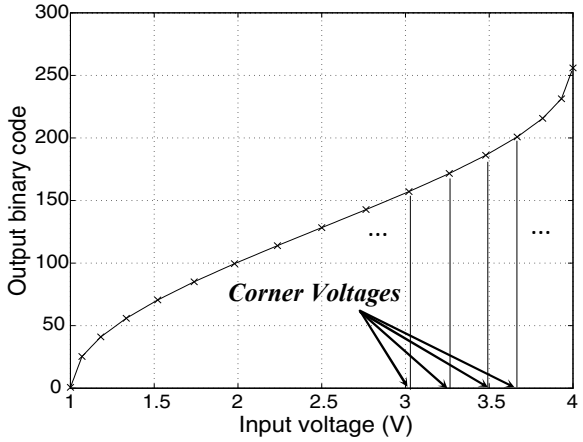


Figure 3. PWL ADC characteristics

V. Comparison and Conclusion

Three different groups of linearization techniques for sensor signals have been presented. Depending on the requirements of the application, one of these techniques may be superior to the others.

Analog linearization techniques are in general the simpler ones and can have a low cost in terms of silicon area and power consumption. Their main drawbacks are sensitivity to environmental conditions (mainly temperature), lack of flexibility when a different kind of sensor is employed, and that accuracy is high typically only in a small input range. Hence, they are usually the preferred choice in low-cost, low-performance applications where the linearized output is required in analog form.

Digital techniques offer more flexibility and accuracy. They can be implemented in general-purpose or dedicated hardware, which is programmed to achieve the required function. However, the potentially high accuracy obtained has a penalty in terms of silicon area and/or processing time. However, due to the advances in digital VLSI circuits, the processing overload of linearization is becoming manageable unless in particular applications were low power or low cost are key factors.

Mixed-signal techniques are particularly suited to applications where the sensor signal has to be converted to digital form and where the signal processing overhead of digital linearization in terms of silicon area, processing time, and power consumption, need to be minimized. This may be the case, for instance, in low-cost integrated sensor interfaces, where reasonable performance must be obtained at the minimum silicon cost.

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