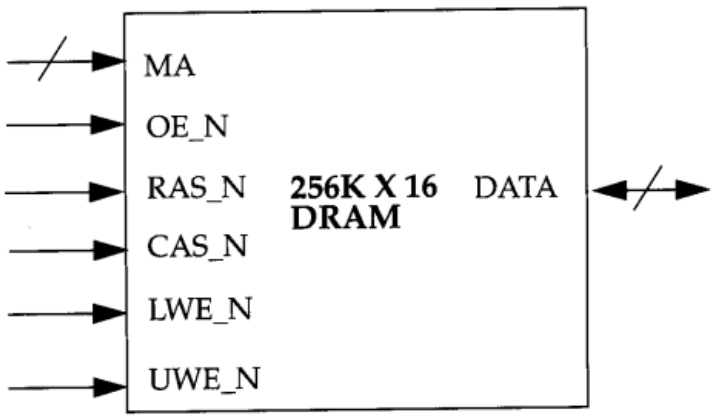
Behavioral DRAM Model

256K x 16 DRAM => 256K 16-bit memory locations

I/O ports:



All ports with a suffix “N” are low asserted.

MA – 10bit memory address

OE – output enable for reading data

RAS – row address strobe for asserting row address

CAS – column address

LWE – lower write enable to write lower 8 bits of data into memory

UWE – upper write enable

DATA – 16bit data as input or output. Write input if LWE_N or UWE_N is asserted; Read output if OE_N is asserted.