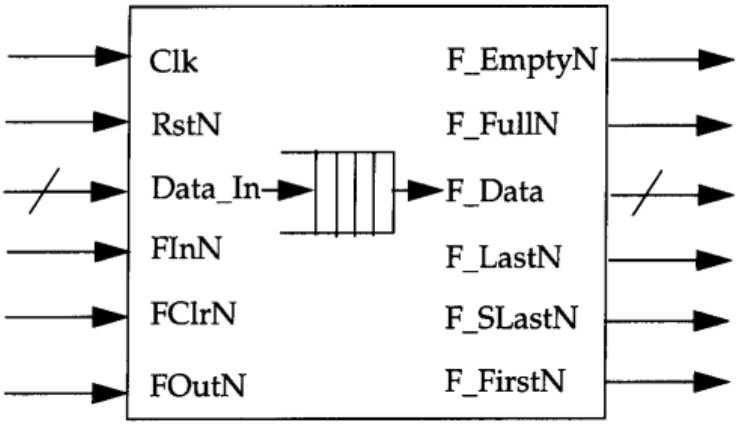
Book example – appendix F

Synthesizable model of a FIFO implementation



I/O ports

The FIFO depth and FIFO width in bits can be modified by simply changing the value of two parameters, ‘FWIDTH’ and ‘FDEPTH’. For this example, the FIFO depth is 4 and the FIFO width is 32 bits.

Input ports:

- Clock signal (Clk)
- Reset signal (RstN) – low asserted
- 32-bit data
- Write signal
- Clear signal
- Read signal

Output ports:

- 32-bit data
- Signal indicating FIFO is full
- Signal indicating FIFO is empty
- Signal indicating FIFO has space for one data value
- Signal indicating FIFO has space for two data values
- Signal indicating that there is only one data value in FIFO

The control circuitry for FIFO. If reset or clr signal is asserted, all the counters are set to 0. If write only the write counter is incremented else if read only read counter is incremented else if both, read and write counters are incremented.

Fcounter indicates the number of items in the FIFO. Write only indicates increments the fcounter, read only decremenets the counter and read&&write doesn't change the counter value.

```
always @(posedge Clk or negedge RstN)
begin
    if(!RstN) begin
        fcounter <= 0;
        rd_ptr <= 0;
        wr_ptr <= 0;
    end
    else begin
        if(~FClrN)begin
            fcounter <= 0;
            rd_ptr <= 0;
            wr_ptr <= 0;
        end
        else begin
            if(~WriteN)
                wr_ptr <= wr_ptr + 1;
            if(~ReadN)
                rd_ptr <= rd_ptr + 1;
            if(~WriteN && ~ReadN && F_FullN)
                fcounter <= fcounter + 1;
            else if(WriteN && ~ReadN && F_EmptyN)
                fcounter <= fcounter - 1;
        end
    end
end
```

All the FIFO status signals depends on the value of fcounter. If the fcounter is equal to afdepth, indicates FIFO is full. If the fcounter is equal to zero, indicates the FIFO is empty.

F_SLastN indicates that there is space for only two data words in the FIFO

Fifo_mem_blk.v – configurable memory block for fifo. The width of the mem block is configured via FWIDTH. All the data into fifo is done synchronous to block.