Project title:

Folded cascode amplifier with a large gain and bandwidth

Present by:

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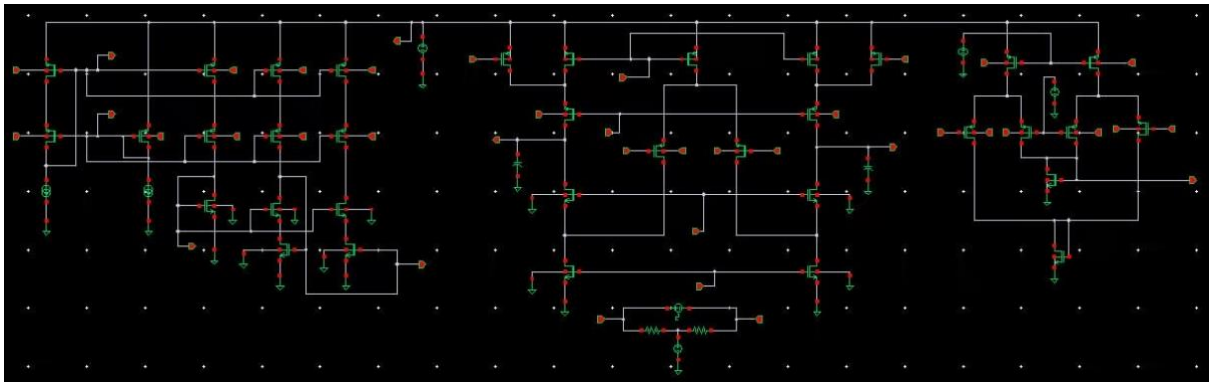
Table of Specifications:

Parameters	Folded Cascode	Positive Feedback
Voltage Gain (dB)	38	53
UGBW (GHz)	1.86861	1.83262
Phase Margin (Degree °)	78	76.5
Load Capacitance (Pico Farad)	0.5	0.5
Power (Milli Watt)	9.558	9.57546
Supply Voltage (V)	1.8	1.8
Input Common Mode Voltage (V)	0.8	0.8
Output Common Mode Voltage (V)	0.92	1.07
Input Noise (V**2/Hz) from (1Hz-2GHz)	26.0125E-8	1.109 E-6
Output Noise (V**2/Hz) from (1Hz-2GHz)	20.81E-6	499.4E-6
Slew Rate (V/µs)	928	1002
Input Referred Offset Voltage(µV) (ΔWin=1u)	16	2.73
CMRR (dB)	83.75	99
PSRR (dB)	245	214



Operation Principle of the Folded Cascode Amplifier

A folded cascode amplifier is a high-gain, wide-bandwidth analog circuit topology that combines the advantages of both common-source and common-gate configurations. The term “folded” refers to the way the signal path is bent, or folded, to allow for the use of both NMOS and PMOS transistors in a complementary manner. This structure enhances the output voltage swing while maintaining a high gain and good common-mode rejection ratio (CMRR).

In a typical fully differential folded cascode amplifier, the input differential pair converts the differential input voltage into a current signal. This current is then mirrored and “folded” into the cascode stage, which provides high output impedance and thus increases the voltage gain. The cascode transistors also help in isolating the input and output nodes, improving the frequency response and reducing the Miller effect.

The main advantages of the folded cascode topology include:

- **High gain** due to the large output resistance provided by the cascode stage.
- **Wide bandwidth** because of reduced parasitic capacitances at high-impedance nodes.
- **Improved output swing** since the signal path is folded, allowing for a higher headroom compared to the conventional cascode amplifier.

- **Excellent CMRR and PSRR**, making it suitable for precision analog applications such as operational amplifiers, ADC front-ends, and switched-capacitor circuits.
- **Good noise performance**, as the input pair can be designed for low noise independent of the output transistors' type.

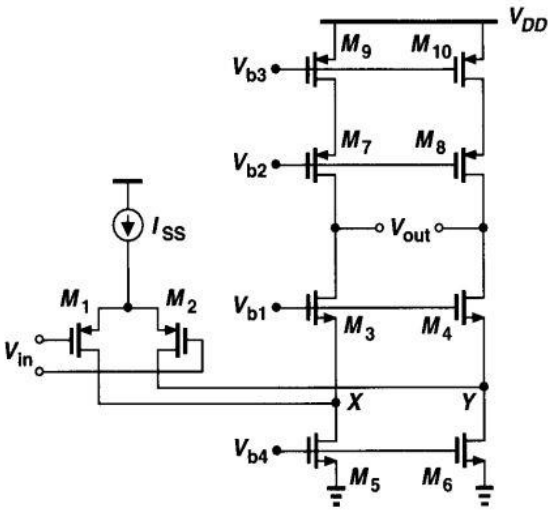


Fig 1: Folded Cascode Amplifier Topology

Circuit Description

The circuit shown below represents a fully differential folded cascode amplifier. In this configuration, transistors M1 and M2 serve as the input differential pair, responsible for converting the differential input voltage into a corresponding differential current. The transistor M0 acts as a current source, providing the bias current for the input stage and ensuring symmetrical operation between the two input branches. Transistors M9 and M10 conduct the total current of both the input and cascode branches (which include transistors M3–M8). Therefore, to handle the combined current without driving the devices out of saturation, M9 and M10 must be sized approximately twice as large as in a conventional single-branch configuration.

This amplifier exhibits three poles and one zero in its small-signal frequency response. The dominant pole appears at the output nodes (Vout+, Vout–). This occurs primarily because:

1. The output resistance at these nodes is significantly higher than at other nodes, which we will later calculate in detail.
2. The output capacitance is large due to both parasitic capacitances and the external load capacitor, which in this design is 0.5 pF**.** The large capacitance at the output node lowers the frequency of the dominant pole, setting the overall bandwidth of the amplifier.

The second pole is located at the lower cascode node, corresponding to transistors M7–M9. The large capacitance at this node results from the parasitic capacitances of transistors M7, M9, and M1. Since M9 is sized twice as large as usual, its parasitic capacitance contributes significantly to this node. Assuming that the first and second poles are widely separated, and the output node is effectively connected to ground beyond the first pole, the resistance seen from this lower cascode node can be approximated as 1/gm. Additionally, there exists a third pole at the upper cascode node (M3–M5) and a zero at the input node (M1). However, these occur at much higher frequencies and can be neglected in the midband analysis. Therefore, for the purpose of small-signal frequency analysis, only the first two poles are considered, as they are well separated and primarily determine the amplifier's stability and frequency response.

In summary, the folded cascode amplifier provides high voltage gain, wide bandwidth, and excellent differential operation. Its frequency response is dominated by the output pole, while the lower cascode pole influences the phase margin and stability. Proper transistor sizing and biasing are thus essential to achieve the desired trade-off between gain, speed, and stability.

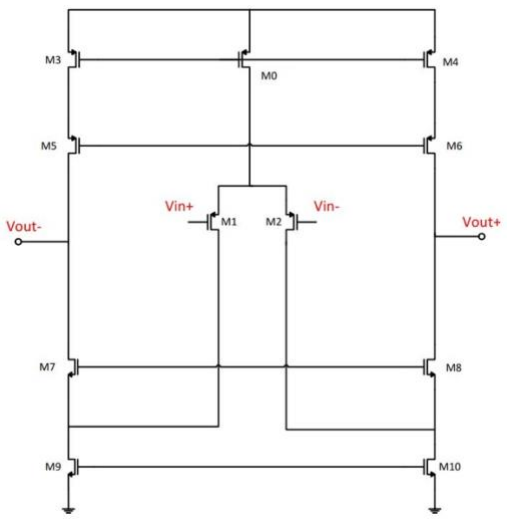


Fig2: Conventional Folded Cascode Circuit

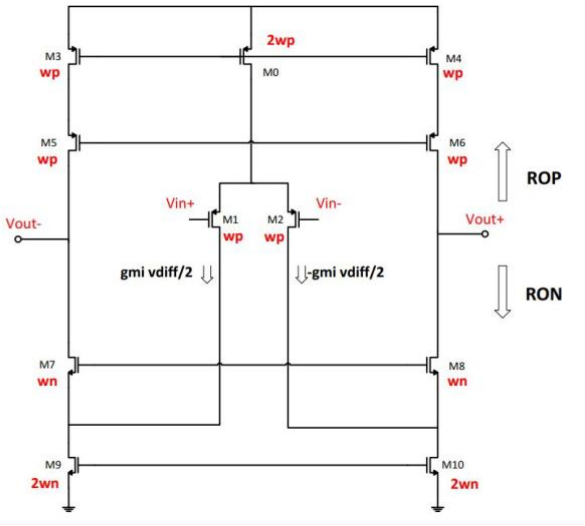


Fig3: Conventional Folded Cascode Circuit (small signal analysis)

Gain and Output Swing Calculation of the Folded Cascode Amplifier

The small-signal voltage gain of a single-stage fully differential amplifier can generally be expressed as: |AV|=Gmi*Rout
Where Gmi is the effective transconductance of the input differential pair, and Rout is the differential output resistance. The small-signal equivalent circuit of the folded cascode amplifier is shown below.

For the given transistor dimensions, the small-signal gain can be written as: Av = -Gmi*Rout

Since each input transistor contributes half of its transconductance in the differential configuration:

$$\text{Gmi} = \frac{\text{gmi}\,\frac{\text{vdiff}}{2}}{\text{vdiff}} = \frac{\text{gmi}}{2}$$

The overall output resistance is the parallel combination of the effective resistances seen from the output branches:

$$\text{Rout} = \text{ROP} \,||\, \text{RON} \qquad \text{where:} \quad \text{ROP} \approx \text{rdsp}\,(1+\text{gmp}\,\text{rdsp}) \qquad \text{RON} \approx \text{rdsn}\,(1+\text{gmn}\,[\,\text{rdsp} \,||\, \tfrac{\text{rdsn}}{2}\,])$$

Assuming that the carrier mobility and channel length modulation parameters are symmetric for NMOS and PMOS devices. that is If: $\text{wp} = \frac{\text{un}}{\text{up}}\,\text{wn}$, $\lambda n = \lambda p \implies \text{rdsn} = \text{rdsp}$, $\text{gmn} = \text{gmp} = \text{gmi}$

Under these conditions, the overall output resistance can be approximated as: $\implies \text{Rout} \approx \frac{1}{4}\,\text{gmi}\,\text{rds}^2$ and therefore, the voltage gain becomes: $\implies \text{AV} \approx \frac{1}{4}\,\text{gmi}^2\,\text{rds}^2$

This relationship shows that the folded cascode amplifier achieves a high intrinsic gain due to the squared dependence on the transistor output resistance rds, which results from the cascode configuration's current buffering effect.

Output Voltage Swing

The output voltage swing of the folded cascode amplifier is limited by the voltage headroom required to keep all transistors in saturation. The general expression for the output swing is: Swing=vdd-2Δvn-2Δvp

ssuming that the voltage drops across NMOS and PMOS transistors are approximately equal (Δvn = Δvp = Δv) the swing simplifies to: Swing=vdd-4Δv

For a 0.18 µm CMOS technology, with a supply voltage VDD=1.8 and assuming a typical overdrive voltage ΔV=0.2 V, the maximum achievable peak-to-peak differential output swing is approximately:

Vswing(max)=1.8−4(0.2) = 1.0V

Common-Mode Feedback (CMFB) Circuit

To achieve the maximum output swing from a fully differential amplifier while ensuring that all transistors remain in the saturation region, a common-mode feedback (CMFB) circuit is required. The primary function of the CMFB circuit is to stabilize the DC level of the output nodes by maintaining the common-mode voltage at a predefined value. This prevents any unwanted drift in the output DC voltage and ensures symmetrical signal swing around the desired operating point.

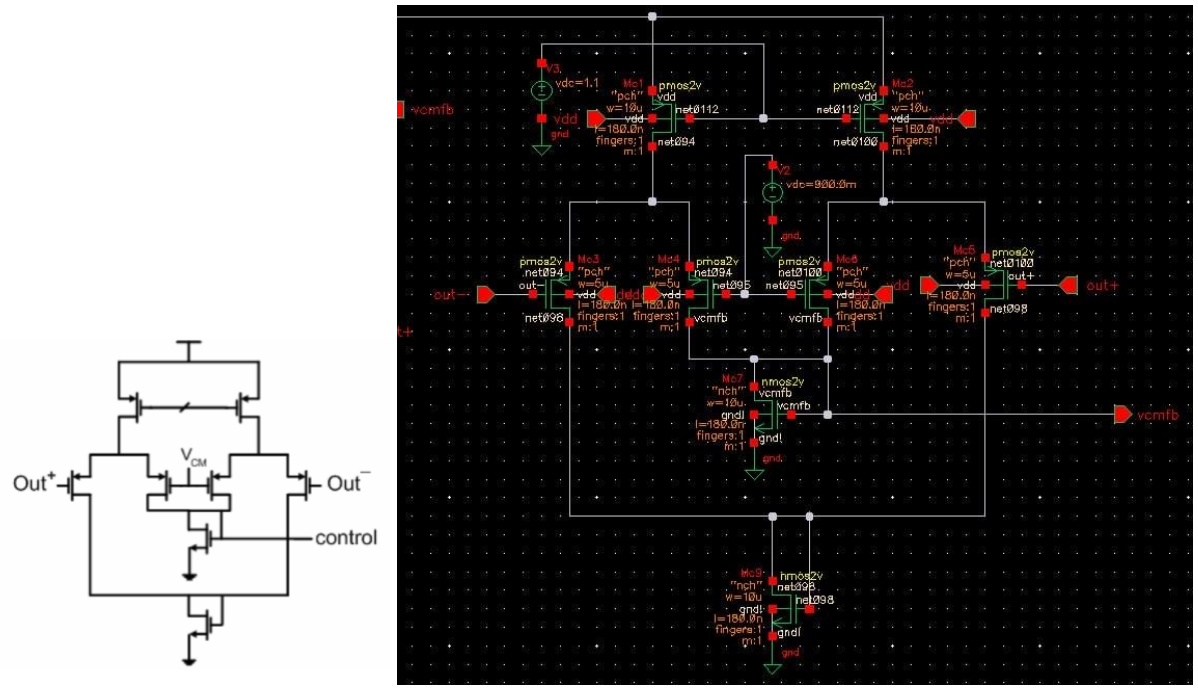


Fig4: Common Mode Feedback Circuit

The CMFB circuit used in this design is a continuous-time common-mode feedback structure. It senses the average voltage of the two differential outputs (Out+ and Out–) and compares it with a reference common-mode voltage (VCM). Based on the difference between the sensed and reference voltages, the CMFB generates an appropriate control voltage (Vctrl) to regulate the output DC level of the amplifier.
The operation principle can be described as follows:

- The differential outputs (Out+ and Out–) are first combined to extract their common-mode component.
- This common-mode voltage is compared with the desired reference voltage VCM (typically set to half of the supply voltage, VDD/2).
- If the actual output common-mode level rises above VCM, the CMFB circuit responds by increasing the control voltage, which in turn reduces the tail current or adjusts the bias of the cascode control transistors.
- Conversely, if the output common-mode level drops below VCM, the control voltage decreases, increasing the bias current and restoring the output to its nominal level.

In this design, the control voltage generated by the CMFB circuit is applied to the gates of the control transistors, which are placed in parallel with M5 and M6 of the main folded cascode amplifier. This configuration effectively adjusts the DC operating point of the differential outputs (Vout1 and Vout2) and stabilizes them near the desired VCM level. Assuming a supply voltage of 1.8 V and setting VCM ≈ VDD/2 = 0.9 V, the CMFB circuit ensures

that both output nodes remain centered around 0.9 V. As a result, the amplifier achieves maximum symmetrical output swing in both directions (positive and negative) without forcing any transistor into the triode region. The figure below illustrates the folded cascode amplifier integrated with its common-mode feedback (CMFB) circuit, which continuously monitors and regulates the output common-mode voltage to maintain stable DC operation and maximize the available dynamic range.

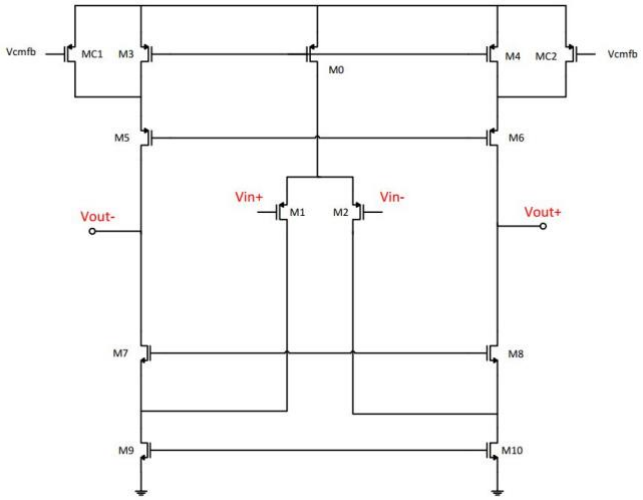


Fig5: Folded Cascode with CMFB Transistors

Positive Feedback Technique for Gain Enhancement.

The figure below illustrates a folded cascode amplifier that incorporates a positive feedback (PFB) technique to further increase the voltage gain. This method leverages controlled regenerative feedback to boost the effective output resistance, thereby enhancing the overall gain without significantly affecting bandwidth or power consumption.

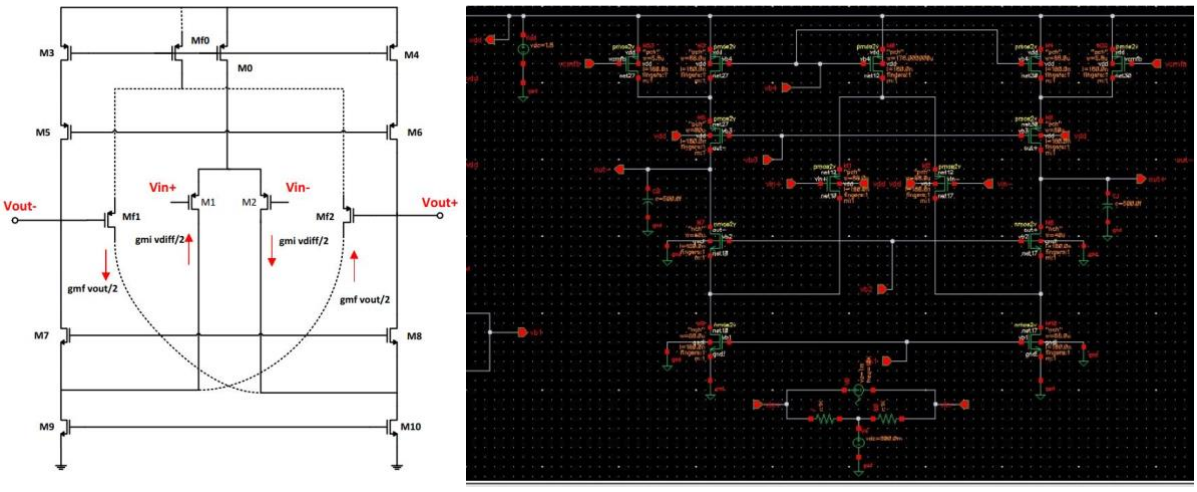


Fig6: Enhanced Gain Folded Cascode with Positive Feedback Method

The small-signal gain of the amplifier with positive feedback can be expressed as:

$$\frac{\text{Vout}}{2} = (\text{gmi}\,\frac{\text{Vdiff}}{2} + \text{gmf}\,\frac{\text{Vout}}{2})\,\text{Rout}$$

From which the voltage gain becomes: $$\frac{\text{Vout}}{\text{Vdiff}} = \frac{\text{gmi Rout}}{1-\text{gmf Rout}}$$

As evident from this expression, when the term gmf Rout approaches unity, the denominator tends to zero, leading to a theoretically infinite gain If $\text{gmf Rout} \approx 1 \implies \text{gain} \to \infty$

Therefore, by properly selecting circuit parameters, the gain can be significantly increased**.** However, care must be taken to ensure that the denominator does not become negative (i.e., gmf Rout > 1), as this would make the circuit unstable and potentially lead to oscillations. In small-signal operation, this configuration functions correctly and provides substantial gain improvement. However, under large-signal conditions, the feedback transistors (Mf1 and Mf2) may enter cutoff when the gate-source voltage difference drops below the threshold voltage (Vth0). In such a case, the positive feedback path is disrupted, causing a sudden reduction in gain and introducing distortion into the output signal. To overcome this limitation, an improved circuit structure is proposed. In this modified design, the voltage applied to the gates of the feedback transistors is attenuated, preventing them from turning off during large output swings and thus maintaining the amplifier's linearity and maximizing its output dynamic range. In the modified circuit, resistors are placed at the output nodes to act as voltage attenuators. These resistors reduce the gate voltage of the feedback transistors during large signal excursions, ensuring that they remain in the active region and continue providing positive feedback. As a result, the amplifier achieves higher output swing while maintaining enhanced gain and improved linearity.

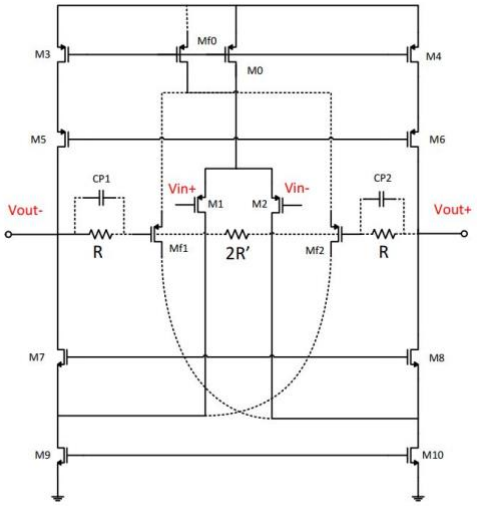


Fig7: Enhanced Gain Folded Cascode with Positive Feedback Method (Swing Compensated)

With the introduction of the attenuation network, the voltage gain is modified as follows: $\frac{\text{Vout}}{\text{Vdiff}} = \frac{\text{gmi Rout}}{1-k\text{gmf Rout}}$

Where k is the attenuation factor, defined as: $K = \frac{R'}{R+R'}$

This expression shows that by adjusting the ratio of the resistors R and R′, the designer can control the degree of positive feedback and thus fine-tune the amplifier's gain without compromising stability. The proposed structure effectively combines gain enhancement**,** stability, and large-signal robustness**,** making it a practical choice for high-performance analog circuit design.

Transistor Sizing and Bias Circuit Design

The transistor sizes are calculated based on their required current levels. The required current for each transistor is determined by the unity-gain bandwidth (UGBW) of the amplifier, which relates to the transconductance of the input transistors and the output load capacitance as follows: $\text{Wu} = \frac{\text{gmi}}{\text{CL}}$

Ingeneral, the transconductance can be approximated by: $\text{gm} = \frac{2\text{ID}}{\Delta\text{v}}$

However, for submicron technologies, a more accurate empirical relationship is used: $\text{gm} = \frac{1.2\ \text{ID}}{\Delta\text{v}}$

The main objective here is to analyze a conventional folded cascode amplifier and compare it with an improved version that uses a transconductance enhancement technique to increase the gain. Therefore, the design starts with an assumed bias current. By selecting a bias current of 1 mA for each transistor branch and an output load capacitance of 0.5 pF**,** the transistor dimensions can be determined using the standard current equations for NMOS and PMOS devices: $\text{ID}_{\text{nmos}} = \frac{1}{2}\,\text{un cox}\,\frac{wn}{l}\,\Delta\text{v}^2$ $\text{ID}_{\text{pmos}} = \frac{1}{2}\,\text{up cox}\,\frac{wn}{l}\,\Delta\text{v}^2$

Assuming ΔVnmos=150mV , ΔVnmos=150mV, and Cox=500μA/V2, while considering that the electron mobility is approximately 2.5 times greater than hole mobility (μn/μp≈2.5), the transistor widths are calculated as follows (with minimum channel length L=0.18μm):

$1mA = \frac{1}{2} 500 \frac{wn}{l} 0.15^2 \implies$ Wn=32u For PMOS transistors: $Wp=\frac{un}{up} wn \implies$ wp=80u

These values correspond to the transistor dimensions of the folded cascode amplifier for a 1 mA bias current. To establish the bias voltages for the transistors, a high-swing current mirror is used. This topology minimizes output swing limitations and allows the output voltage to reach its maximum range without pushing transistors out of saturation. It is important to note that the bias circuit does not influence the amplifier's small-signal behavior (such as gain, frequency response, or linearity). Therefore, its transistors are typically sized at 1/10th of those in the main amplifier to minimize power consumption. In this design, the high-swing current mirror is configured with **a** reference current (Iref) of 100 μA, and the PMOS and NMOS transistor sizes are set to one-tenth of the corresponding transistors in the folded cascode stage to properly generate the required bias voltages.

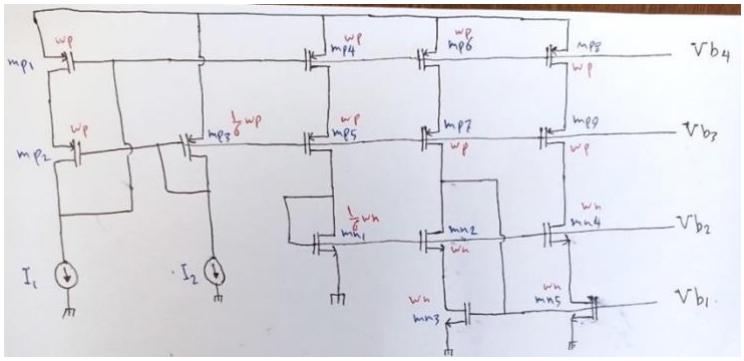
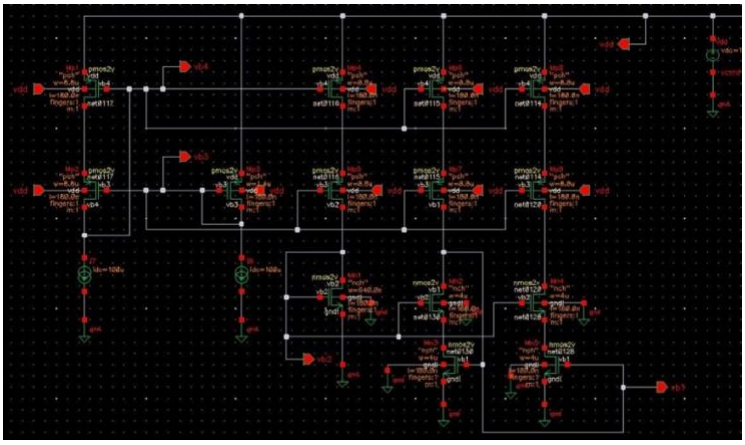


Fig8. Bias Circuit



Finally, it should be noted that theoretical calculations rarely match practical simulation or fabrication results exactly. This discrepancy arises because theoretical models assume ideal conditions and neglect secondary transistor effects such as channel-length modulation, body effect, velocity saturation, and hot-carrier effects. Therefore, in practice, transistor dimensions must often be fine-tuned through iterative simulations to achieve the desired performance.

Simulation Results

The frequency-domain simulation results confirm the correct operation of the folded cascode amplifier designed in the Cadence environment using 0.18 μm CMOS technology. As observed from the AC analysis, the conventional folded cascode amplifier achieves a voltage gain of approximately 77 V/V, which corresponds to 38 dB. The transient analysis results also verify this performance, confirming the amplifier's proper functionality in the time domain.

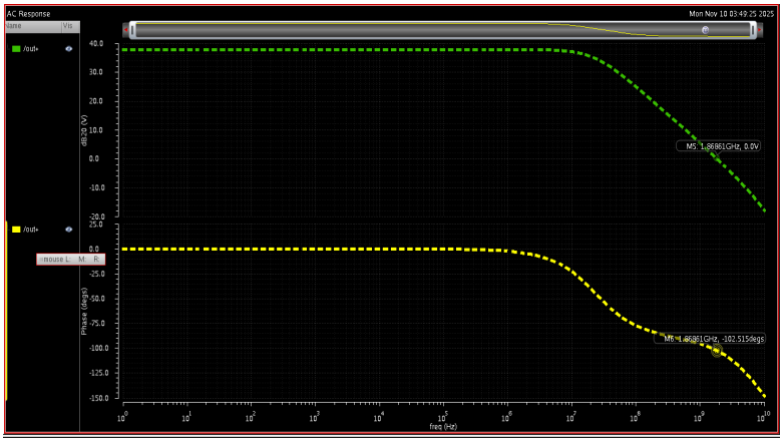


Fig9: AC Analysis for Conventional Folded Cascode (Frequency Domain)

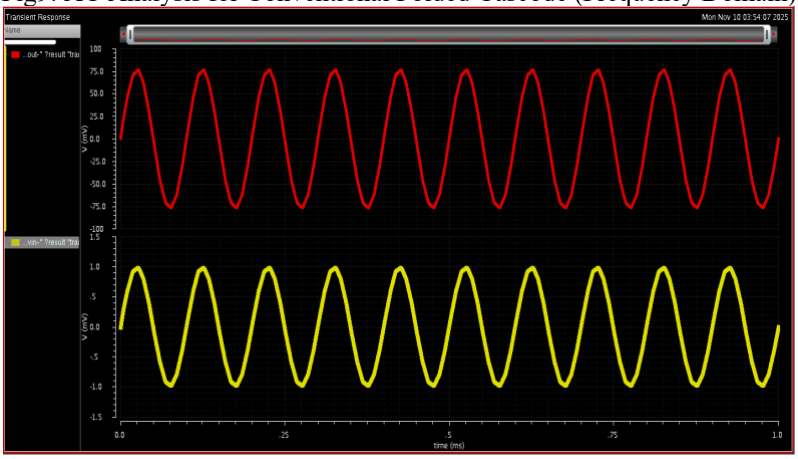


Fig10: Transient Analysis for Conventional Folded Cascode (Time Domain)

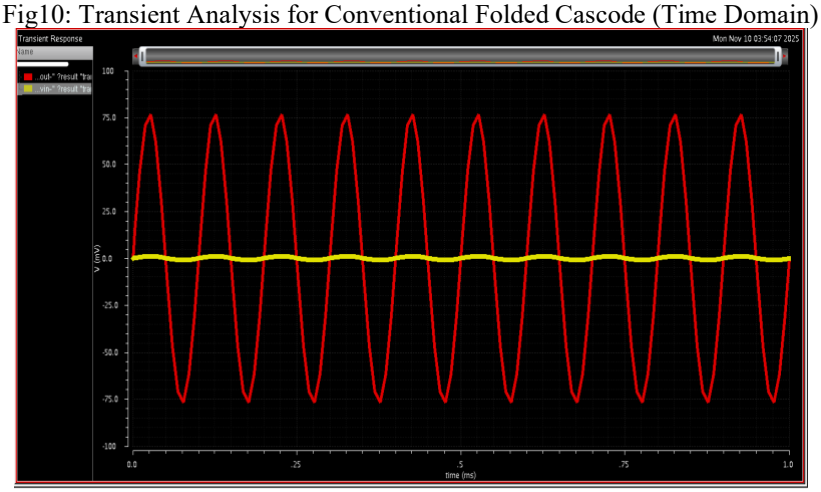


Fig11: Transient Analysis for Conventional Folded Cascode (Two Waves in one plot)

The unity-gain bandwidth (UGBW) of the amplifier is measured to be 1.86861 GHz, indicating a wide bandwidth suitable for high-speed analog applications. The phase margin (PM) is calculated using the standard relationship: PM=180°+Phase at UGBW

Since the phase at the unity-gain frequency is approximately –102°, the resulting phase margin is about 78°, which indicates excellent stability and phase response. Furthermore, the simulation results for the folded cascode amplifier with positive feedback enhancement clearly demonstrate a significant increase in voltage

gain, reaching approximately 53 dB. By further optimizing transistor dimensions and resistor values, even higher gain levels can be achieved while maintaining stability and linearity.

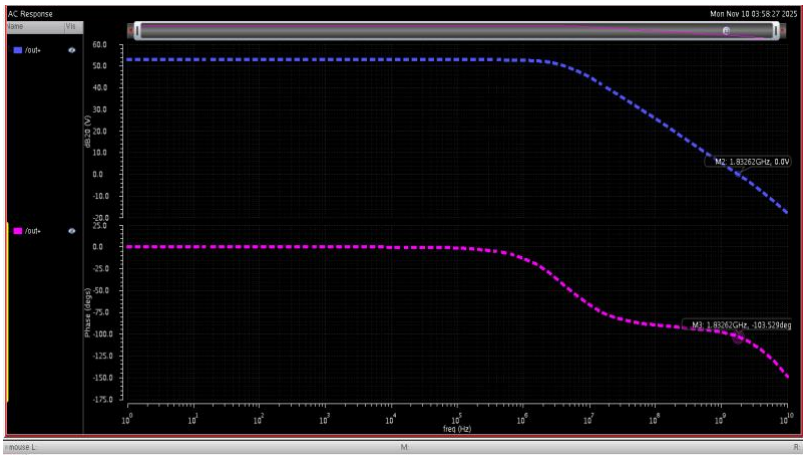


Figure 12-AC Analysis for Enhanced Folded Cascode with Positive Feedback (Frequency Domain)

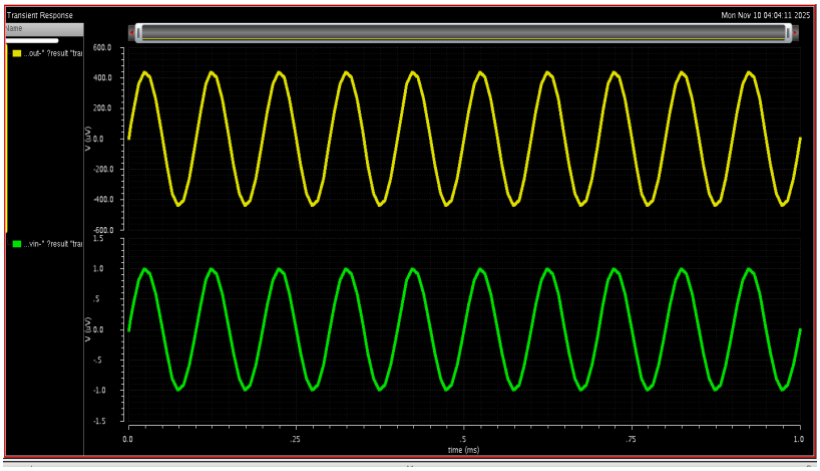


Fig13: Transient Analysis for Enhanced Folded Cascode with Positive Feedback (Time Domain)

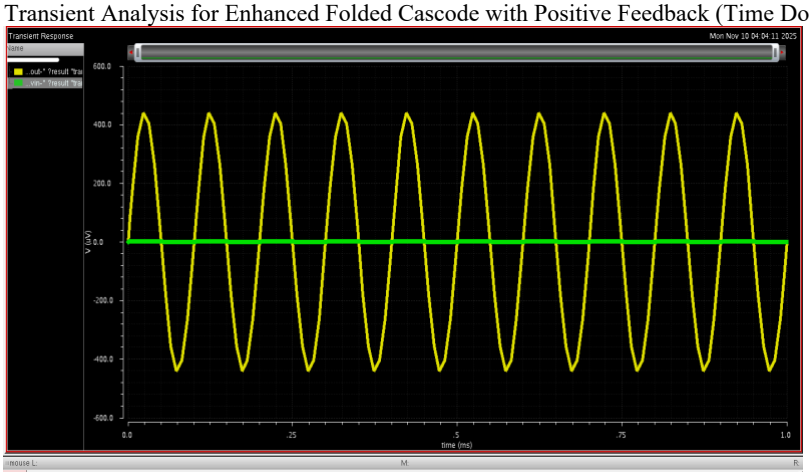


Fig14: Transient Analysis for Enhanced Folded Cascode with Positive Feedback (Two Waves in one plot)

All the key performance parameters of the conventional folded cascode amplifier and the folded cascode amplifier with positive feedback are summarized in the table below.

References:

Razavi, B. (2017). Design of analog CMOS integrated circuits. McGraw-Hill Education

Folded cascode amplifier | download scientific diagram. (n.d.). https://www.researchgate.net/figure/Folded-cascode-amplifier_fig1_319211241