Project title:

Folded cascode amplifier with a large gain and bandwidth

Present by:

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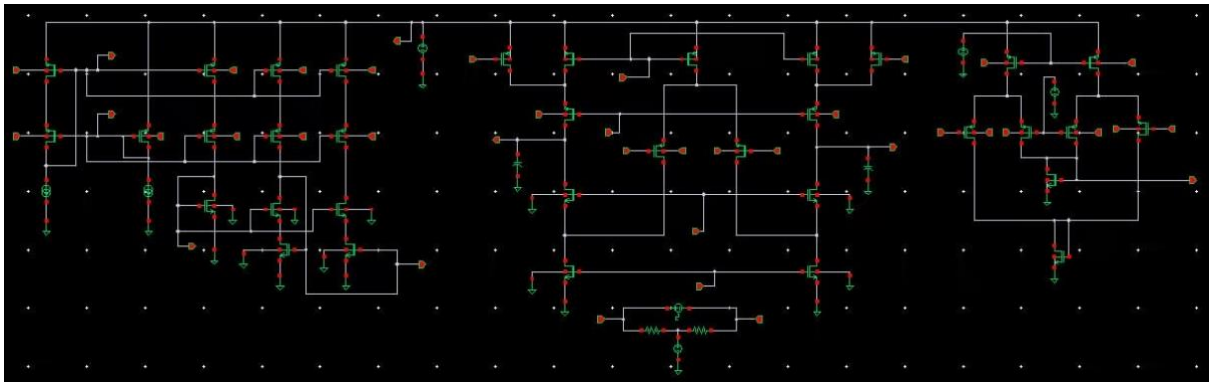
12/15/2025

Table 1: Specifications

Parameters	Folded Cascode	Positive Feedback
Voltage Gain (dB)	38	53
UGBW (GHz)	1.86861	1.83262
Phase Margin (Degree °)	78	76.5
Load Capacitance (Pico Farad)	0.5	0.5
Power (Milli Watt)	9.558	9.57546
Supply Voltage (V)	1.8	1.8
Input Common Mode Voltage (V)	0.8	0.8
Output Common Mode Voltage (V)	0.92	1.07
Input Noise (V**2/Hz) from (1Hz-2GHz)	26.0125E-8	1.109 E-6
Output Noise (V**2/Hz) from (1Hz-2GHz)	20.81E-6	499.4E-6
Slew Rate (V/µs)	928	1002
Input Referred Offset Voltage(µV) (ΔWin=1u)	16	2.73
CMRR (dB)	83.75	99
PSRR (dB)	245	214



Operation Principle of the Folded Cascode Amplifier

A folded cascode amplifier is a high-gain, wide-bandwidth analog circuit topology that combines the advantages of both common-source and common-gate configurations. The term “folded” refers to the way the signal path is bent, or folded, to allow for the use of both NMOS and PMOS transistors in a complementary manner. This structure enhances the output voltage swing while maintaining a high gain and good common-mode rejection ratio (CMRR).

In a typical fully differential folded cascode amplifier, the input differential pair converts the differential input voltage into a current signal. This current is then mirrored and “folded” into the cascode stage, which provides high output impedance and thus increases the voltage gain. The cascode transistors also help in isolating the input and output nodes, improving the frequency response and reducing the Miller effect.

The main advantages of the folded cascode topology include:

- **High gain** due to the large output resistance provided by the cascode stage.
- **Wide bandwidth** because of reduced parasitic capacitances at high-impedance nodes.
- **Improved output swing** since the signal path is folded, allowing for a higher headroom compared to the conventional cascode amplifier.
- **Excellent CMRR and PSRR**, making it suitable for precision analog applications such as operational amplifiers, ADC front-ends, and switched-capacitor circuits.

- **Good noise performance**, as the input pair can be designed for low noise independent of the output transistors' type.

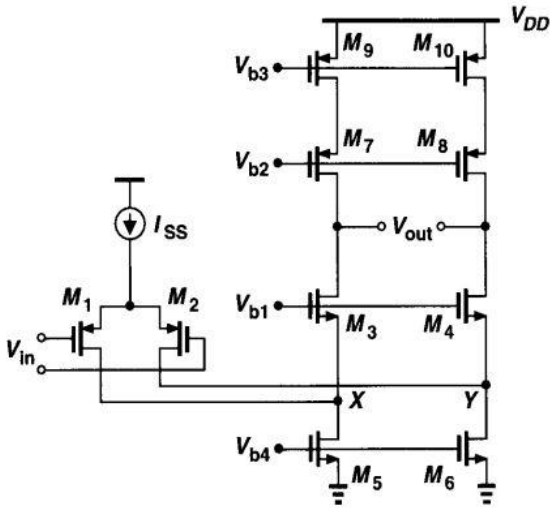


Fig 1: Folded Cascode Amplifier Topology

Circuit Description

The circuit shown below represents a fully differential folded cascode amplifier. In this configuration, transistors M1 and M2 serve as the input differential pair, responsible for converting the differential input voltage into a corresponding differential current. The transistor M0 acts as a current source, providing the bias current for the input stage and ensuring symmetrical operation between the two input branches. Transistors M9 and M10 conduct the total current of both the input and cascode branches (which include transistors M3–M8). Therefore, to handle the combined current without driving the devices out of saturation, M9 and M10 must be sized approximately twice as large as in a conventional single-branch configuration.

This amplifier exhibits three poles and one zero in its small-signal frequency response. The dominant pole appears at the output nodes (Vout+, Vout–). This occurs primarily because:

1. The output resistance at these nodes is significantly higher than at other nodes, which we will later calculate in detail.
2. The output capacitance is large due to both parasitic capacitances and the external load capacitor, which in this design is 0.5 pF**.** The large capacitance at the output node lowers the frequency of the dominant pole, setting the overall bandwidth of the amplifier.

The second pole is located at the lower cascode node, corresponding to transistors M7–M9. The large capacitance at this node results from the parasitic capacitances of transistors M7, M9, and M1. Since M9 is sized twice as large as usual, its parasitic capacitance contributes significantly to this node. Assuming that the first and second poles are widely separated, and the output node is effectively connected to ground beyond the first pole, the resistance seen from this lower cascode node can be approximated as 1/gm. Additionally, there exists a third pole at the upper cascode node (M3–M5) and a zero at the input node (M1). However, these occur at much higher frequencies and can be neglected in the midband analysis. Therefore, for the purpose of small-signal frequency analysis, only the first two poles are considered, as they are well separated and primarily determine the amplifier's stability and frequency response.

In summary, the folded cascode amplifier provides high voltage gain, wide bandwidth, and excellent differential operation. Its frequency response is dominated by the output pole, while the lower cascode pole influences the phase margin and stability. Proper transistor sizing and biasing are thus essential to achieve the desired trade-off between gain, speed, and stability.

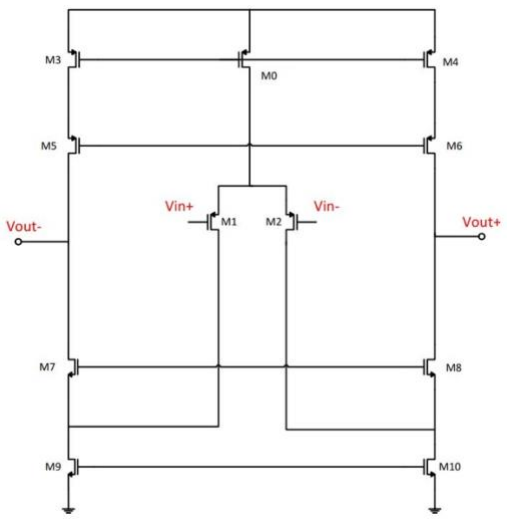


Fig2: Conventional Folded Cascode Circuit

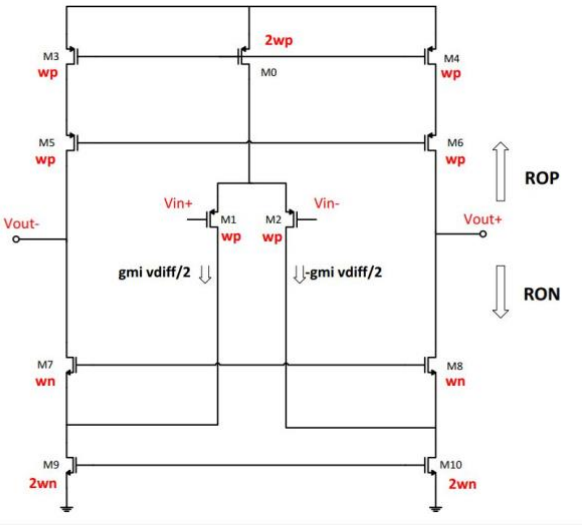


Fig3: Conventional Folded Cascode Circuit (small signal analysis)

Gain and Output Swing Calculation of the Folded Cascode Amplifier

The small-signal voltage gain of a single-stage fully differential amplifier can generally be expressed as: |AV|=Gmi*Rout Where Gmi is the effective transconductance of the input differential pair, and Rout is the differential output resistance. The small-signal equivalent circuit of the folded cascode amplifier is shown below.

For the given transistor dimensions, the small-signal gain can be written as: Av = -Gmi*Rout

Since each input transistor contributes half of its transconductance in the differential configuration:

$$\text{Gmi} = \frac{\text{gmi}\frac{\text{vdiff}}{2}}{\text{vdiff}} = \frac{\text{gmi}}{2}$$

The overall output resistance is the parallel combination of the effective resistances seen from the output branches:

$$\text{Rout} = \text{ROP} \,||\, \text{RON} \qquad \text{where:} \quad \text{ROP} \approx \text{rdsp}\,(\,1+\text{gmp rdsp}\,) \quad \text{RON} \approx \text{rdsn}\,(\,1+\text{gmn}\,[\,\text{rdsp} \,||\, \frac{\text{rdsn}}{2}\,]\,)$$

Assuming that the carrier mobility and channel length modulation parameters are symmetric for NMOS and PMOS devices. that is If: $\text{wp} = \frac{\text{un}}{\text{up}}\text{wn}$, $\lambda n = \lambda p \implies \text{rdsn} = \text{rdsp}$, $\text{gmn} = \text{gmp} = \text{gmi}$

Under these conditions, the overall output resistance can be approximated as: $\Longrightarrow \text{Rout} \approx \frac{1}{4}\ \text{gmi}\ \text{rds}^2$ and therefore, the voltage gain becomes: $\Longrightarrow \text{AV} \approx \frac{1}{4}\ \text{gmi}^2\ \text{rds}^2$

This relationship shows that the folded cascode amplifier achieves a high intrinsic gain due to the squared dependence on the transistor output resistance rds, which results from the cascode configuration's current buffering effect.

Output Voltage Swing

The output voltage swing of the folded cascode amplifier is limited by the voltage headroom required to keep all transistors in saturation. The general expression for the output swing is: Swing=vdd-2Δvn-2Δvp

assuming that the voltage drops across NMOS and PMOS transistors are approximately equal (Δvn = Δvp = Δv) the swing simplifies to: Swing=vdd-4Δv

For a 0.18 μm CMOS technology, with a supply voltage VDD=1.8 and assuming a typical overdrive voltage ΔV=0.2 V, the maximum achievable peak-to-peak differential output swing is approximately:

Vswing(max)=1.8−4(0.2) = 1.0V

Common-Mode Feedback (CMFB) Circuit To achieve the maximum output swing from a fully differential amplifier while ensuring that all transistors remain in the saturation region, a common-mode feedback (CMFB) circuit is required. The primary function of the CMFB circuit is to stabilize the DC level of the output nodes by maintaining the common-mode voltage at a predefined value. This prevents any unwanted drift in the output DC voltage and ensures symmetrical signal swing around the desired operating point.

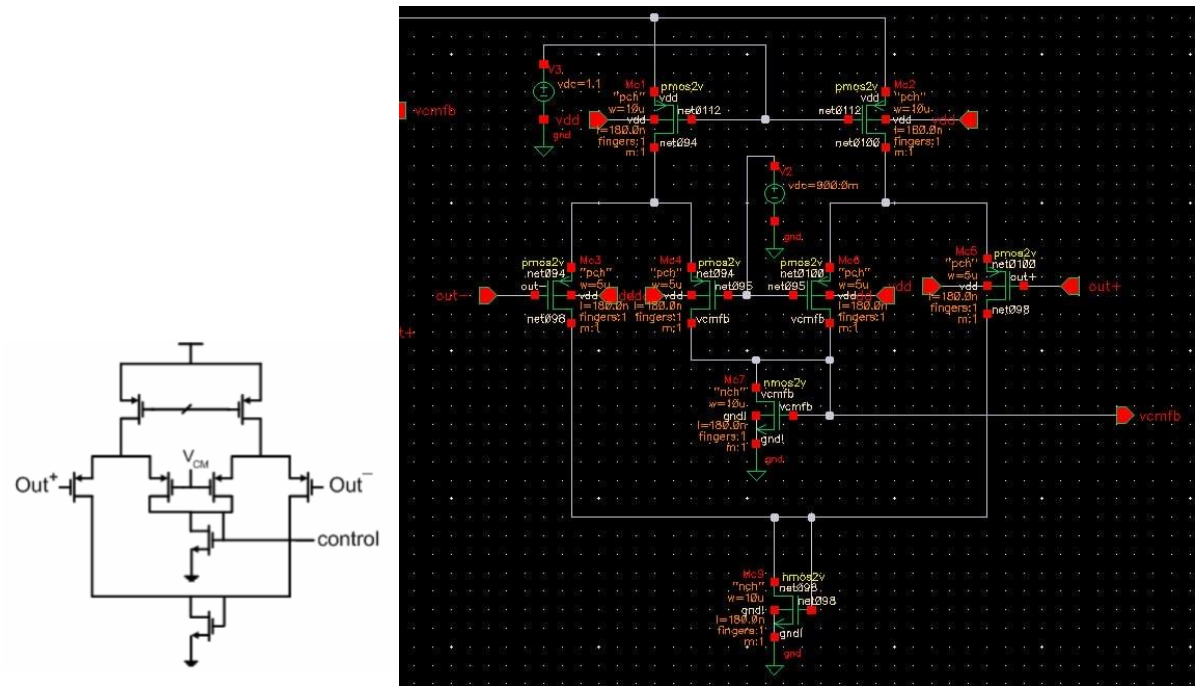


Fig4: Common Mode Feedback Circuit

The CMFB circuit used in this design is a continuous-time common-mode feedback structure. It senses the average voltage of the two differential outputs (Out+ and Out–) and compares it with a reference common-mode voltage (VCM). Based on the difference between the sensed and reference voltages, the CMFB generates an appropriate control voltage (Vctrl) to regulate the output DC level of the amplifier. The operation principle can be described as follows:

- The differential outputs (Out+ and Out–) are first combined to extract their common-mode component.
- This common-mode voltage is compared with the desired reference voltage VCM (typically set to half of the supply voltage, VDD/2).
- If the actual output common-mode level rises above VCM, the CMFB circuit responds by increasing the control voltage, which in turn reduces the tail current or adjusts the bias of the cascode control transistors.
- Conversely, if the output common-mode level drops below VCM, the control voltage decreases, increasing the bias current and restoring the output to its nominal level.

In this design, the control voltage generated by the CMFB circuit is applied to the gates of the control transistors, which are placed in parallel with M5 and M6 of the main folded cascode amplifier. This configuration effectively adjusts the DC operating point of the differential outputs (Vout1 and Vout2) and stabilizes them near the desired VCM level. Assuming a supply voltage of 1.8 V and setting VCM ≈ VDD/2 = 0.9 V, the CMFB circuit ensures that both output nodes remain centered around 0.9 V. As a result, the amplifier achieves maximum symmetrical output swing in both directions (positive and negative) without forcing any transistor into the triode region. The figure below illustrates the folded cascode amplifier integrated with its common-mode feedback (CMFB) circuit, which continuously monitors and regulates the output common-mode voltage to maintain stable DC operation and maximize the available dynamic range.

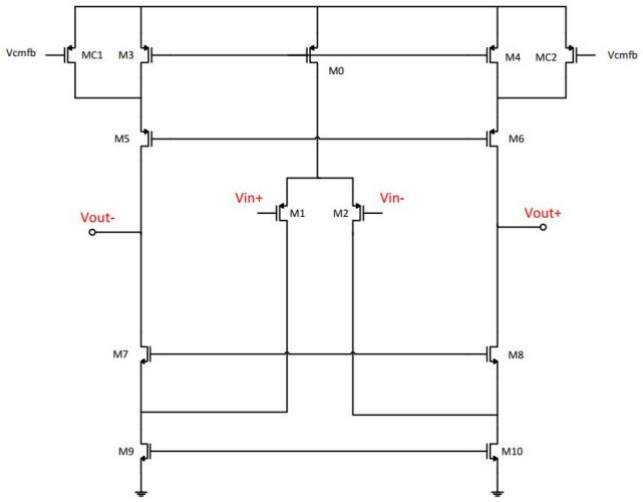


Fig5: Folded Cascode with CMFB Transistors

Positive Feedback Technique for Gain Enhancement.

The figure below illustrates a folded cascode amplifier that incorporates a positive feedback (PFB) technique to further increase the voltage gain. This method leverages controlled regenerative feedback to boost the effective output resistance, thereby enhancing the overall gain without significantly affecting bandwidth or power consumption.

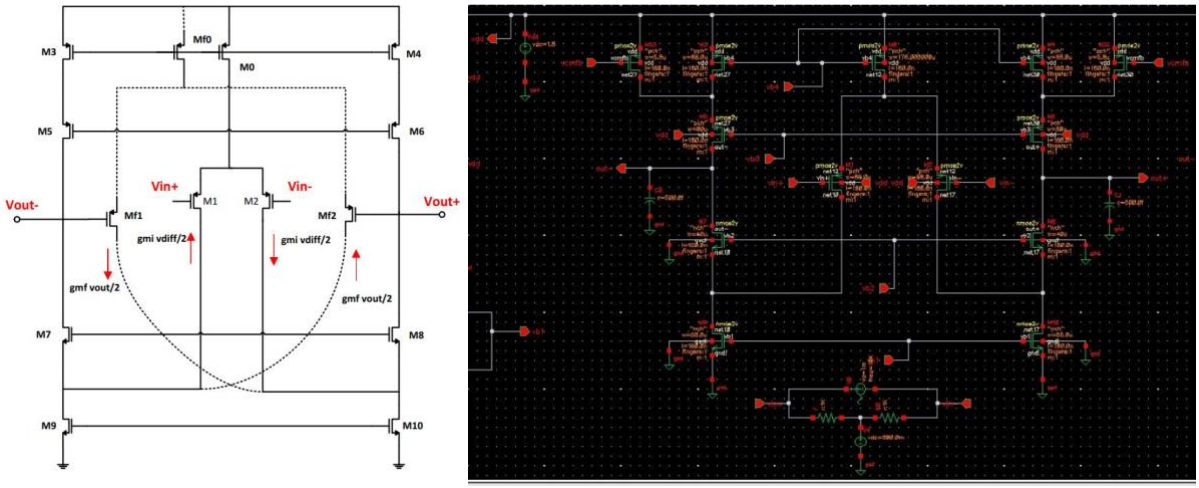


Fig6: Enhanced Gain Folded Cascode with Positive Feedback Method

The small-signal gain of the amplifier with positive feedback can be expressed as:

$\frac{\text{Vout}}{2} = (\text{gmi}\,\frac{\text{Vdiff}}{2} + \text{gmf}\,\frac{\text{Vout}}{2})\,\text{Rout}$ From which the voltage gain becomes: $\frac{\text{Vout}}{\text{Vdiff}} = \frac{\text{gmi Rout}}{1-\text{gmf Rout}}$

As evident from this expression, when the term gmf Rout approaches unity, the denominator tends to zero, leading to a theoretically infinite gain If $\text{gmf Rout} \approx 1 \implies \text{gain} \to \infty$ Therefore, by properly selecting circuit parameters, the gain can be significantly increased**.** However, care must be taken to ensure that the denominator does not become negative (i.e., gmf Rout > 1), as this would make the circuit unstable and potentially lead to oscillations. In small-signal operation, this configuration functions correctly and provides substantial gain improvement. However, under large-signal conditions, the feedback transistors (Mf1 and Mf2) may enter cutoff when the gate-source voltage difference drops below the threshold voltage (Vth0). In such a case, the positive feedback path is disrupted, causing a sudden reduction in gain and introducing distortion into the output signal. To overcome this limitation, an improved circuit structure is proposed. In this modified design, the voltage applied to the gates of the feedback transistors is attenuated, preventing them from turning off during large output swings and thus maintaining the amplifier's linearity and maximizing its output dynamic range. In the modified circuit, resistors are placed at the output nodes to act as voltage attenuators. These resistors reduce the

gate voltage of the feedback transistors during large signal excursions, ensuring that they remain in the active region and continue providing positive feedback. As a result, the amplifier achieves higher output swing while maintaining enhanced gain and improved linearity.

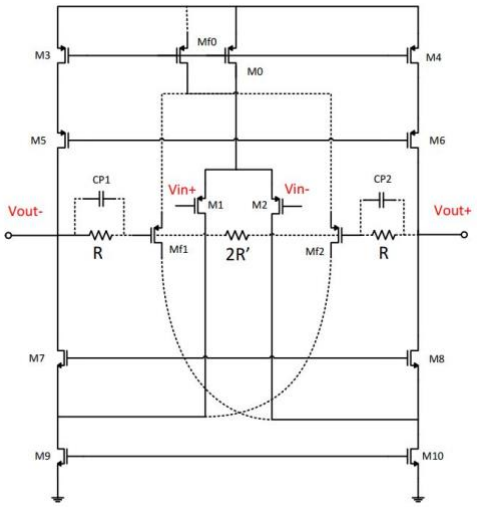


Fig7: Enhanced Gain Folded Cascode with Positive Feedback Method (Swing Compensated)

With the introduction of the attenuation network, the voltage gain is modified as follows: $\frac{\text{Vout}}{\text{Vdiff}} = \frac{\text{gmi Rout}}{1-k\text{gmf Rout}}$

Where k is the attenuation factor, defined as: $K = \frac{R\prime}{R+R\prime}$

This expression shows that by adjusting the ratio of the resistors R and R′, the designer can control the degree of positive feedback and thus fine-tune the amplifier's gain without compromising stability. The proposed structure effectively combines gain enhancement**,** stability, and large-signal robustness**,** making it a practical choice for high-performance analog circuit design.

Transistor Sizing and Bias Circuit Design

The transistor sizes are calculated based on their required current levels. The required current for each transistor is determined by the unity-gain bandwidth (UGBW) of the amplifier, which relates to the transconductance of the input transistors and the output load capacitance as follows: $Wu = \frac{\text{gmi}}{\text{CL}}$

Ingeneral, the transconductance can be approximated by: $gm = \frac{2ID}{\Delta v}$ However, for submicron technologies, a more accurate empirical relationship is used: $gm = \frac{1.2\ ID}{\Delta v}$ The main objective here is to analyze a conventional folded cascode amplifier and compare it with an improved version that uses a transconductance enhancement technique to increase the gain. Therefore, the design starts with an assumed bias current. By selecting a bias current of 1 mA for each transistor branch and an output load capacitance of 0.5 pF**,** the transistor dimensions can be determined using the standard current equations for NMOS and PMOS devices: $ID_{nmos} = \frac{1}{2}\,\text{un cox}\,\frac{wn}{l}\,\Delta v^2$

$ID_{pmos} = \frac{1}{2}\,\text{up cox}\,\frac{wn}{l}\,\Delta v^2$ Assuming ΔVnmos=150mV , ΔVnmos=150mV, and Cox=500μA/V2, while considering that the electron mobility is approximately 2.5 times greater than hole mobility (μn/μp≈2.5), the transistor widths are calculated as follows (with minimum channel length L=0.18μm):

$1\text{mA} = \frac{1}{2}\,500\ \frac{wn}{l}\,0.15^2 \implies$ Wn=32u For PMOS transistors: $Wp = \frac{\text{un}}{\text{up}}\,\text{wn} \implies$ wp=80u

These values correspond to the transistor dimensions of the folded cascode amplifier for a 1 mA bias current. To establish the bias voltages for the transistors, a high-swing current mirror is used. This topology minimizes output swing limitations and allows the output voltage to reach its maximum range without pushing transistors out of saturation. It is important to note that the bias circuit does not influence the amplifier's small-signal behavior (such as gain, frequency response, or linearity). Therefore, its transistors are typically sized at 1/10th of those in the main amplifier to minimize power consumption. In this design, the high-swing current mirror is configured with **a** reference current (Iref) of 100 µA, and the PMOS and NMOS transistor sizes are set to one-tenth of the corresponding transistors in the folded cascode stage to properly generate the required bias voltages.

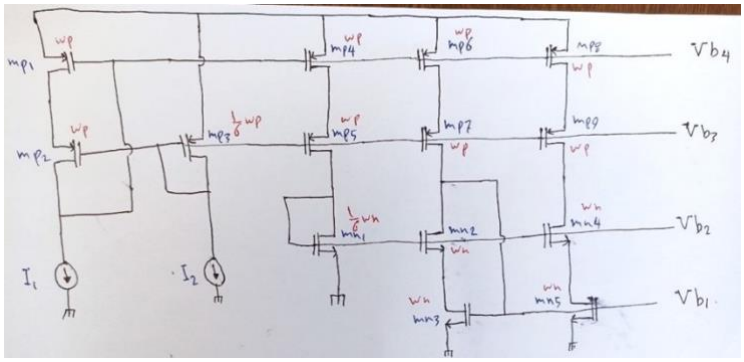
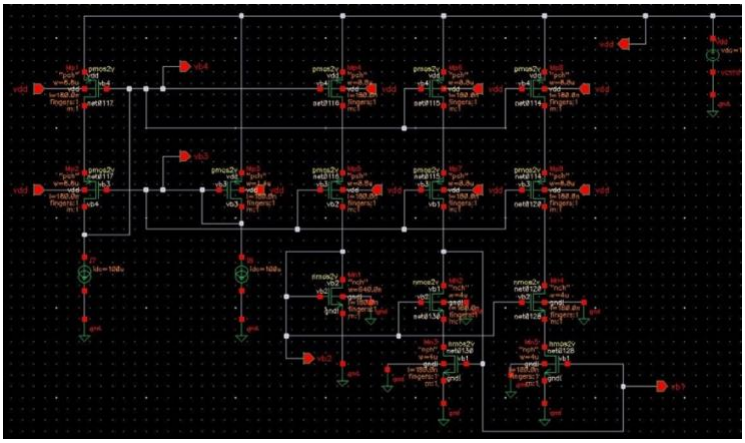


Fig8. Bias Circuit



Finally, it should be noted that theoretical calculations rarely match practical simulation or fabrication results exactly. This discrepancy arises because theoretical models assume ideal conditions and neglect secondary transistor effects such as channel-length modulation, body effect, velocity saturation, and hot-carrier effects. Therefore, in practice, transistor dimensions must often be fine-tuned through iterative simulations to achieve the desired performance.

Simulation Results

The frequency-domain simulation results confirm the correct operation of the folded cascode amplifier designed in the Cadence environment using 0.18 µm CMOS technology. As observed from the AC analysis, the conventional folded cascode amplifier achieves a voltage gain of approximately 77 V/V, which corresponds to 38 dB. The transient analysis results also verify this performance, confirming the amplifier's proper functionality in the time domain.

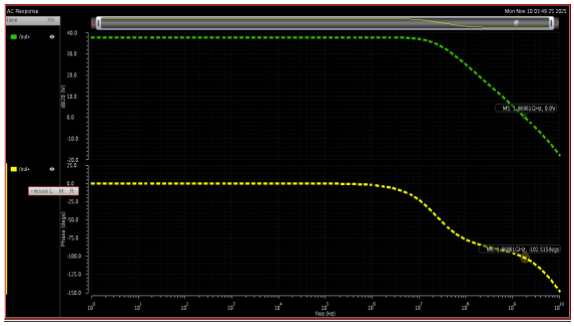


Fig9: AC Analysis for Conventional Folded Cascode (Frequency Domain)

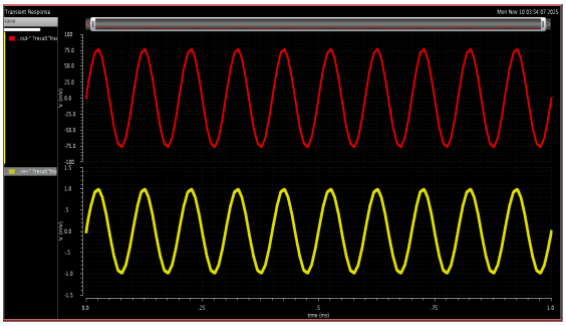


Fig10: Transient Analysis for Conventional Folded Cascode (Time Domain)

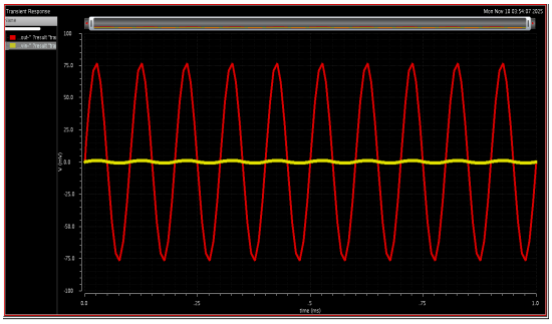


Fig11: Transient Analysis for conventional Folded Cascode (Two Waves in one plot)

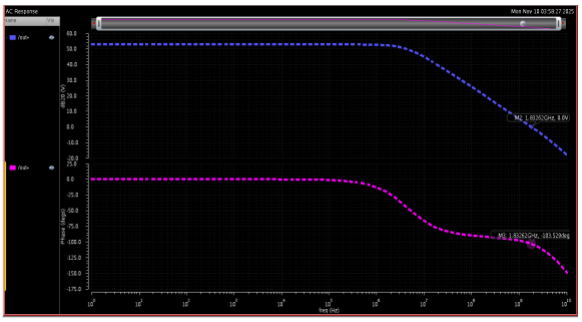


Fig12: AC Analysis for Enhanced Folded Cascode with Positive Feedback (Frequency Domain)

The unity-gain bandwidth (UGBW) of the amplifier is measured to be 1.86861 GHz, indicating a wide bandwidth suitable for high-speed analog applications. The phase margin (PM) is calculated using the standard relationship:
PM=180°+Phase at UGBW Since the phase at the unity-gain frequency is approximately –102°, the resulting phase margin is about 78°, which indicates excellent stability and phase response. Furthermore, the simulation results for the folded cascode amplifier with positive feedback enhancement clearly demonstrate a significant increase in voltage gain, reaching approximately 53 dB. By further optimizing transistor dimensions and resistor values, even higher gain levels can be achieved while maintaining stability and linearity.

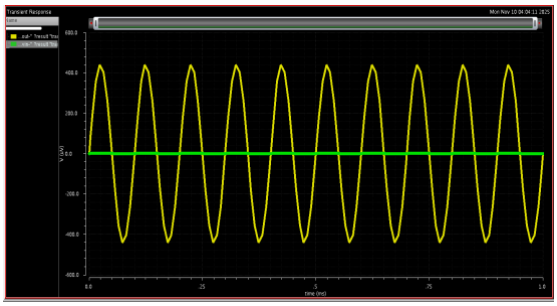


Fig13: Transient Analysis for Enhanced Folded Cascode with Positive Feedback (Time Domain)

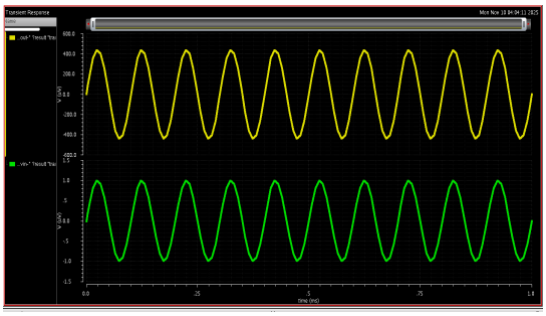


Fig14: Transient Analysis for Enhanced Folded Cascod. with Positive Feedback (Two Waves in one plot)

All the key performance parameters of the conventional folded cascode amplifier and the folded cascode amplifier with positive feedback are summarized in the table below.

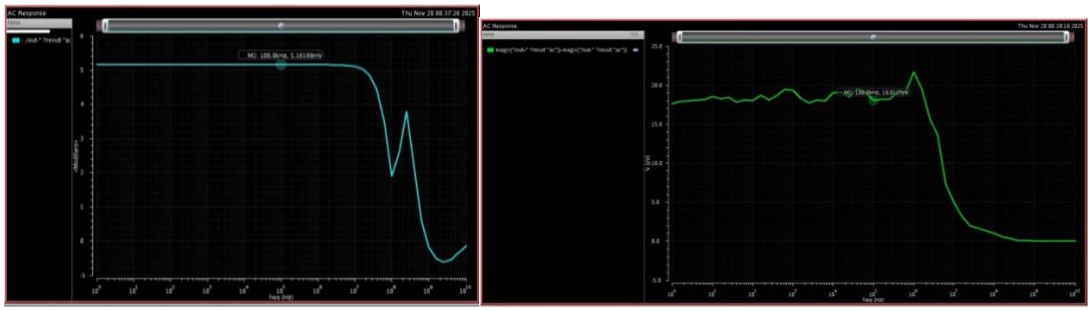
CMRR/PSRR

Aps Folded-Cascode = (512) fv Aps Folded-Cascode+ = (18) pv Acm Folded-Cascode = 0.005

Ad Folded Cascode = 77 Ad Feedback+ = 450

PSRR(dB)=20 log(Aps/Ad)

$$\mathrm{CMRR} = \left(\frac{A_\mathrm{d}}{|A_\mathrm{cm}|}\right) = 10\log_{10}\left(\frac{A_\mathrm{d}}{A_\mathrm{cm}}\right)^2 \mathrm{dB} = 20\log_{10}\left(\frac{A_\mathrm{d}}{|A_\mathrm{cm}|}\right)\mathrm{dB}$$



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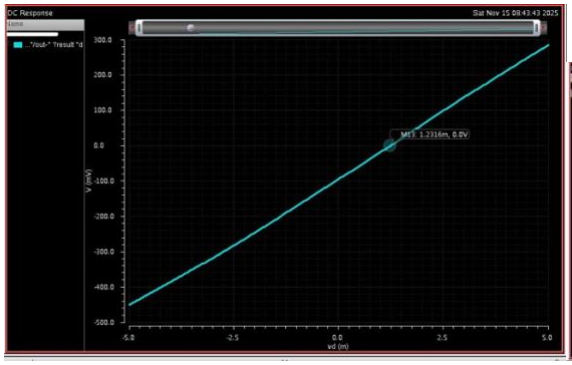
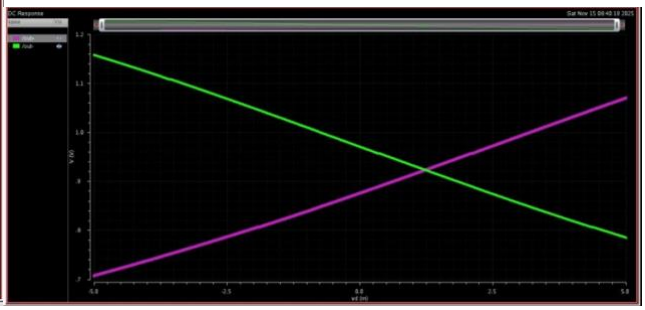
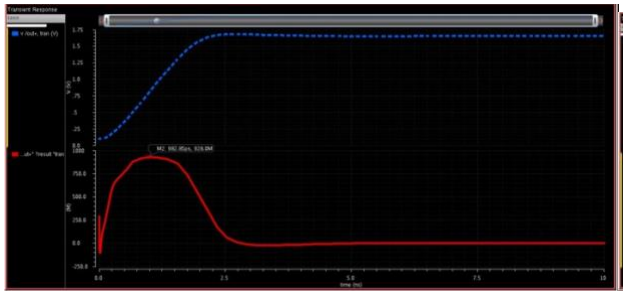
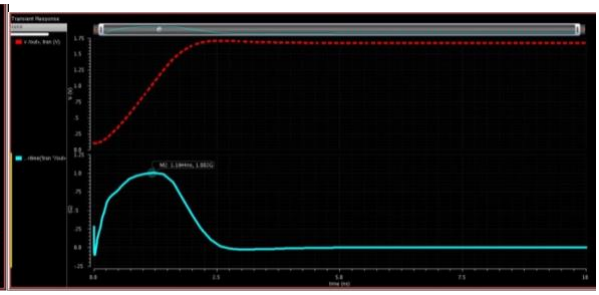
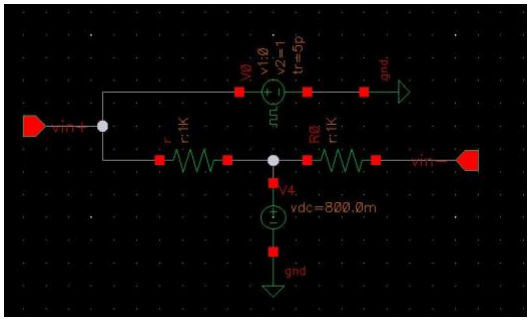



Noise:


Slew Rate:

Improved Positive-Feedback Amplifier Design and CMFB Optimization

In the second phase of this project, the positive-feedback amplifier was redesigned and optimized to achieve higher gain, improved common-mode stability, and a structure that is more suitable for practical CMOS implementation. While the core differential topology and transistor sizing philosophy remained unchanged, significant architectural modifications were introduced in the biasing network, the CMFB circuitry, and the positive-feedback resistive network.

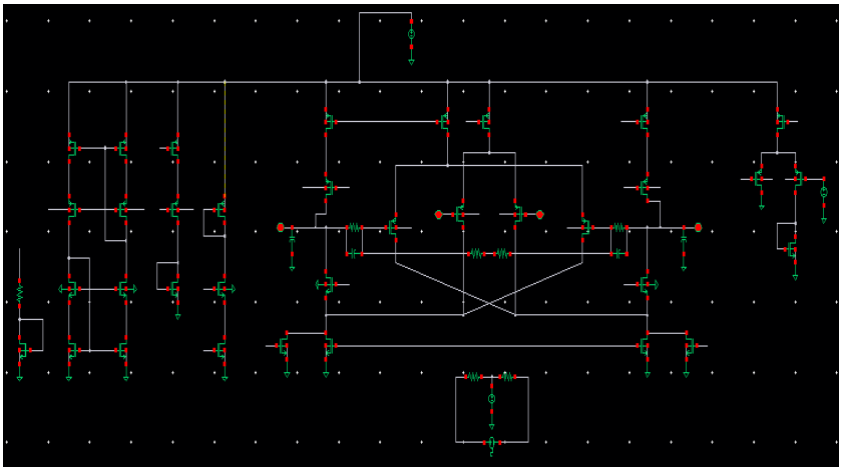


Figure 15: Improved Positive-Feedback Amplifier

Redesign of the Biasing Network

The first improvement was a complete reconstruction of the biasing circuitry. The original multi-stage biasing scheme was replaced with a more compact and robust structure, reducing sensitivity to process variations and simplifying the overall layout. Although the transistor widths (W/L) used in the main amplification core remained identical to the previous design, the implementation was made more practical by replacing ultra-wide devices with multi-finger transistors. For example, a device previously sized at *W = 88 µm* was implemented as *W = 8.8 µm with 10 fingers*, maintaining the same effective width while significantly improving matching, parasitics, and layout feasibility.

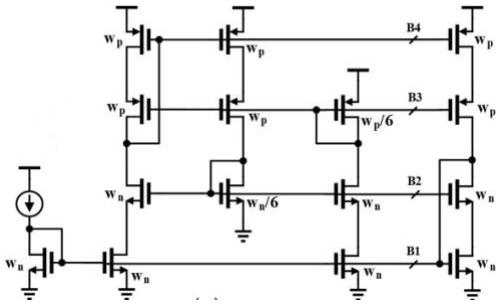


Figure 16: Biasing Circuit

Simplified CMFB Architecture

A major enhancement was introduced in the Common-Mode Feedback (CMFB) circuit.
Instead of extracting the common-mode voltage from the differential outputs (as done in the previous version), the proposed design employs a simplified CMFB structure derived from a portion of the existing positive-feedback network.

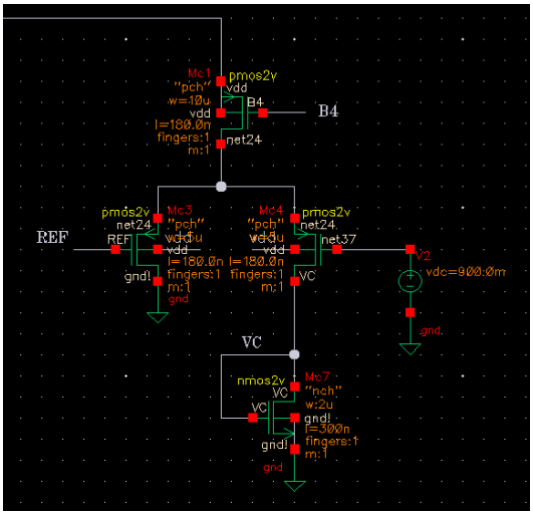


Figure 17: Simplified CMFB Circuit

Feedback Extraction Method

The two resistors of the positive-feedback path were divided into equal segments, and the mid-point node was used as the CMFB sensing point. This method eliminates the need for dedicated output-sensing circuitry and reduces the load on the differential nodes.

CMFB Circuit Description

The redesigned CMFB consists of only four transistors, making it significantly simpler while maintaining stable common-mode regulation:

- One transistor acts as the current-setting device for the CMFB loop.
- A second transistor receives the feedback voltage derived from the midpoint of the split resistors.
- This feedback voltage is compared to a reference voltage applied to the gate of a complementary transistor.
- Based on the difference between these two voltages, the CMFB adjusts the current in the associated branch.
- The output of the CMFB loop is then applied directly to the gates of the lower-tail transistors of the differential pair.

One of the transistors in the CMFB path operates with gate and drain shorted, effectively acting as a MOS resistor and providing a clean control voltage for the differential pair. This architecture ensures that the output common-mode voltage remains constant, while minimizing circuit complexity and power consumption.

Modifications to the Positive-Feedback Network

Beyond the improved sensing strategy, the values of the positive-feedback resistors were optimized to increase the amplifier gain while avoiding instability. Through iterative simulation and fine-tuning of the resistor ratios, the open-loop gain increased significantly, reaching approximately 76 dB, which represents a substantial improvement over the original design. Importantly, the fundamental analytical relationships derived for the previous design remain valid, as the transistor-level structure and operating points have not changed. Only the feedback path and biasing arrangements were enhanced to improve overall performance.

Simulation Results and Performance Summary

Extensive simulations were conducted to evaluate the redesigned positive-feedback amplifier and the simplified CMFB circuit. The results indicate consistent improvement across all major performance parameters compared to the initial design.

AC Gain, UGBW, Power and Phase Response

Comprehensive simulations were performed to evaluate the performance of the improved amplifier. The results confirm that the proposed architecture provides better AC characteristics, stable DC operating points, and reliable transient behavior.

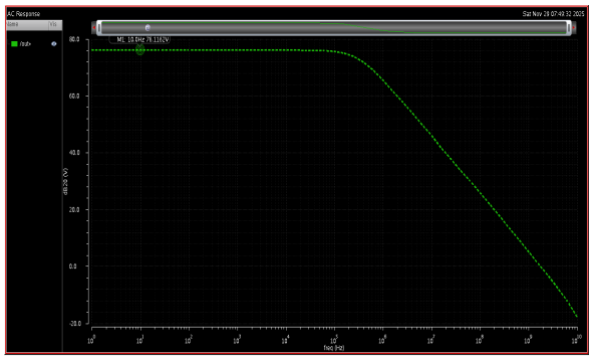


Figure 18: AC Gain Response

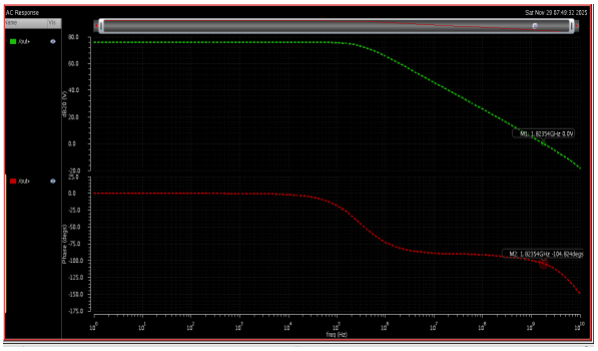


Figure 19: UGBW and Phase Margin Response

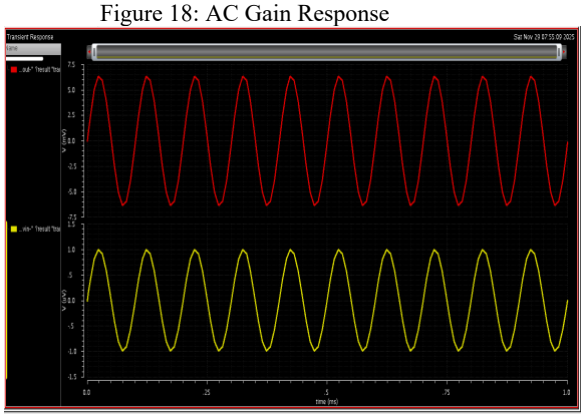


Figure 20: Transient Analysis

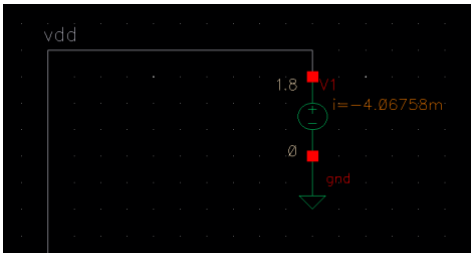


Figure 21: The Current Drawn from Vdd

CMFB Behavior and Common-Mode Regulation
The simplified CMFB circuit effectively maintains the output common-mode voltage at the desired level.
By extracting the feedback from the midpoint of the split positive-feedback resistors, the CMFB loop operates with lower complexity while providing:

- Stable common-mode regulation
- Faster settling
- Reduced loading on differential outputs

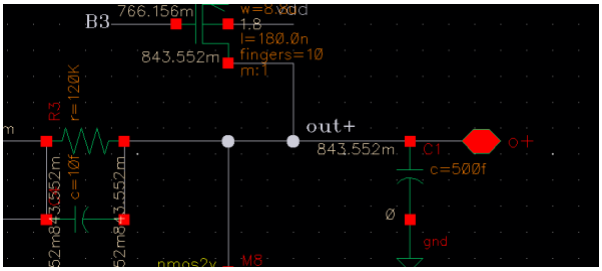


Figure 22: The Common Mode Output Voltage

Overall Performance Summary
A complete comparison of all simulated parameters including gain, phase margin, bandwidth, common-mode error, and power consumption is provided in Table 1. All metrics show clear improvement over the previous version of the design.

Table 2: Tabulated Parameters of Modified Amplifier

Parameters	Positive Feedback
Voltage Gain (dB)	76.1162
UGBW (GHz)	1.82354
Phase Margin (Degree °)	75.176
Load Capacitance (Pico Farad)	0.5
Power (Milli Watt)	7.321644
Supply Voltage (V)	1.8
Input Common Mode Voltage (V)	0.8
Output Common Mode Voltage (V)	843.552mV
Input Noise (V**2/Hz) from (1Hz-2GHz)	14.33 E-9
Output Noise (V**2/Hz) from (1Hz-2GHz)	91.63E-6
Slew Rate (V/µs)	1208
Input Referred Offset Voltage(mV) (ΔWin=1u)	1.35
CMRR (dB)	96.1162
PSRR (dB)	157.944
SC Filter Gain (dB)	6.356
SC Filter Bandwidth (MHz)	1.968
1st Order RC Filter Gain (dB)	5.82993
1st Order RC Filter Bandwidth (MHz)	1.99
2nd Order RC Filter Gain (dB)	5.82993
2nd Order RC Filter Bandwidth (MHz)	1.968

First-Order Differential RC Low-Pass Filter
In this stage of the project, a fully differential first-order RC low-pass filter was designed and simulated. The objective was to achieve a −3 dB cutoff frequency of approximately 2 MHz while maintaining a unity voltage gain. The design is based on the standard transfer function of a first-order passive RC filter, extended to the differential domain.

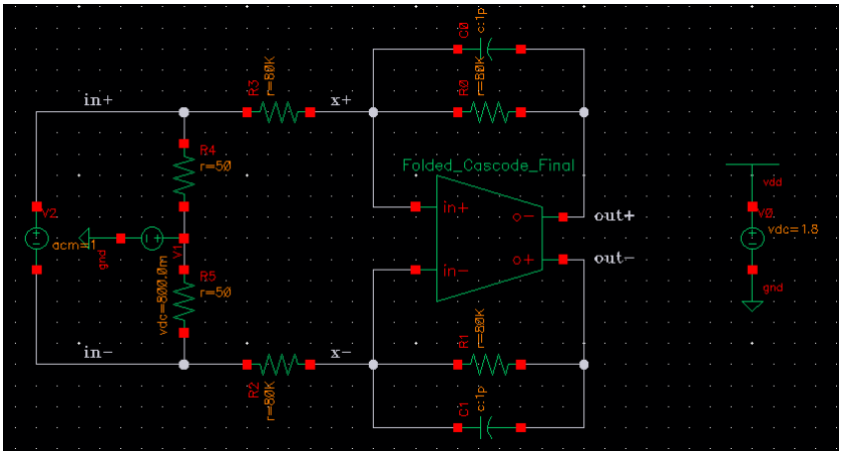


Figure 23: Schematic of a First Order Differential Active RC Filter

Filter Structure and Transfer Function

The implemented filter consists of two identical RC branches configured in a fully differential manner. Each branch uses a resistor–capacitor pair (R, C), ensuring symmetry and proper common-mode rejection. The single-ended transfer function of a first-order RC low-pass filter is:

$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{1}{1+RCs}$ $fc = \frac{1}{2\pi RC}$

Since the differential filter simply duplicates the single-ended structure with symmetric components, the same cutoff expression applies.

Component Selection and Gain Setting

To achieve the target cutoff frequency of fc≈2 MHz, the resistor and capacitor values were selected as: R = 80KΩ, C = 1Pf

which corresponds to an expected cutoff frequency of: fc ≈ 1.99 MHz

This is in excellent agreement with the simulation result of 1.968 MHz, demonstrating consistency between theoretical calculation and circuit-level behavior.

Because the desired filter gain is unity, equal resistor values were used for both the input and feedback paths:

- Rin = 80 kΩ
- Rout = 80 kΩ

This guarantees: $Gain = \frac{R2}{R1} = 1$

To achieve a greater gain, the resistor value was selected as: R = 40KΩ

This guarantees: $Gain = \frac{R2}{R1} = 2$

Phase Response

The filter exabits the typical phase characteristic of a first-order low-pass network. Due to the negative polarity introduced by the resistor ratio: $H(s) = -\frac{R2}{R1} \cdot \frac{1}{1+RCs}$

and with unity gain defined by $\frac{R2}{R1} = 1$

the phase response starts at −180° at low frequencies and approaches −270° as the frequency increases well beyond the pole.

This is consistent with the differential implementation because the two output nodes produce equal and opposite phase shifts, preserving differential behavior.

Simulation Results of 1st Order Filter

The simulation results validate the analytical derivation:

- Cutoff frequency: 1.968 MHz (close to the calculated 1.99 MHz)
- Magnitude response: −3 dB at expected cutoff
- Unity gain: confirmed for differential input/output
- Phase: starts near −180° and follows the theoretical first-order slope
- As expected for a first-order low-pass network, the magnitude rolls off with a slope of −20 dB/decade beyond the cutoff frequency.

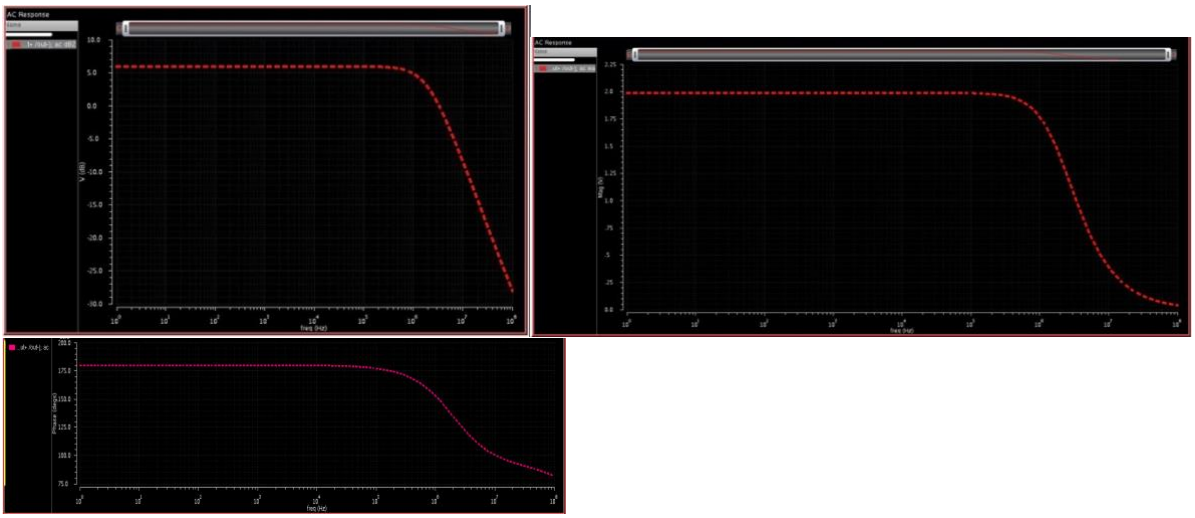


Figure 24: Simulation Result of a First Order Differential Active RC Filter

Second-Order RC Low-Pass Filter (Cascaded First-Order Stages)

A second-order low-pass response was implemented by cascading two identical first-order RC stages in series. This approach preserves a simple design methodology while achieving a steeper roll-off than a single pole. Unlike the single-pole differential stage described earlier, the overall cascaded output is not inverted at low frequencies (low-frequency phase ≈ 0°) because each passive RC stage is non-inverting; the combined phase tends toward −180° at frequencies well above the pole pair.

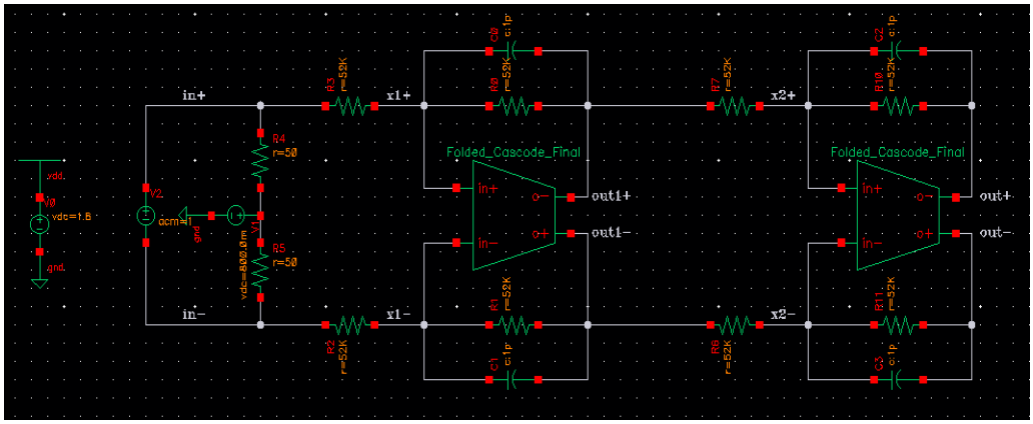


Figure 25: Schematic of a Second Order Differential Active RC Filter

Structure and Transfer Function

For two identical first-order RC stages cascaded, the overall transfer function is: $H(s) = \left(\frac{1}{1+RCs}\right)^2 = \frac{1}{(1+RCs)^2}$

In the frequency domain (with $s = j\omega$) the magnitude is $|H(j\omega)| = \frac{1}{1+(WRC)^2}$

and the phase is the sum of the two single-pole phase contributions; at low frequency the phase is approximately 0∘ and it approaches −180∘ for $\omega \gg 1/RC$.

Because two poles are present, the high-frequency magnitude roll-off follows a slope of −40 dB/decade (i.e. −20 dB/dec per pole).

Cutoff Frequency: Single-Stage vs. Cascaded −3 dB Point

The pole frequency of each identical RC stage is $f_{c,single} = \frac{1}{2\pi RC}$

However, the overall −3 dB point of the cascaded pair (the frequency where the combined magnitude falls by 3 dB) is shifted relative to the single-stage pole. For two identical stages, the combined −3 dB frequency f3db total relates to the single-stage pole $f_{c,single}$ by: $|H(j\omega)|^2 = \frac{1}{\left(1+(f/f_{c,\,\text{single}})^2\right)^2} \Rightarrow$ At $|H| = \frac{1}{\sqrt{2}}: 1 + \left(f/f_{c,\,\text{single}}\right)^2 = \sqrt{2}$.

Hence: $f_{3dB,\,\text{total}} = f_{c,\,\text{single}} \cdot \sqrt{\sqrt{2}-1} \approx 0.64359 f_{c,\,\text{single}}$

To target an overall -3 dB frequency of approximately 2.0 MHz, the single-stage pole must therefore be set to:

$$f_{c,\,\text{single}} \approx \frac{2.0\text{MHz}}{0.64359} \approx 3.11\text{MHz}$$

Component Selection and Numerical Calculation

Using the selected component values:

- R=52 kΩ
- C=1 pF

so the single-stage pole is: $f_{c,single} = \frac{1}{2\pi RC} \approx 3.0607$ MHz.

Applying the cascade relation above gives the combined −3 dB frequency: $f_{3dB,total} \approx 0.64359 \times 3.0607$ MHz ≈ 1.9698 MHz,

which matches the simulation result (~1.968 MHz) and confirms consistency between analytical design and circuit simulation.

Because unity gain was required, the input and feedback resistances of each stage were chosen to produce an overall gain of **1** (i.e., Rin = Rout=52 kΩ where appropriate in the implemented topology).

To achieve a greater gain, the resistor value was selected as: R = 26KΩ

This guarantees: Gain = $\frac{R2}{R1} = 2$

Phase and Roll-off

The cascaded response shows the expected phase behavior:

- Low frequencies: phase ≈ 0∘ (non-inverting)
- Near the combined corner: phase moves toward negative values as the poles contribute up to −90° each
- High frequencies: phase → −180∘

As stated above, the magnitude rolls off as −40 dB/decade beyond the combined corner frequency, consistent with the presence of two poles.

Simulation Results of 2nd Order Filter

Simulation results confirm the theoretical predictions:

- Single-stage pole (theoretical): ≈ 3.0607 MHz
- Combined −3 dB (simulation): ≈ 1.968 MHz
- Gain: unity across passband (differential implementation)
- High-frequency roll-off: ≈ −40 dB/decade
- Phase: 0° at low frequency → −180° at high frequency

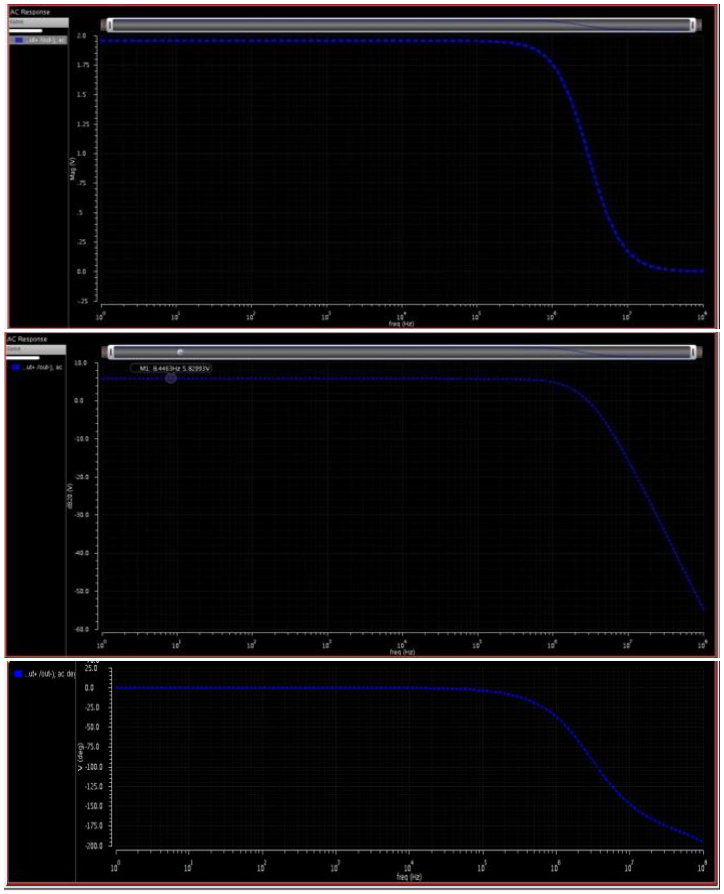


Figure 26: Simulation Result of a Second Order Differential Active RC Filter

First-Order Switched-Capacitor (SC) Low-Pass Filter

A first-order low-pass filter was implemented using a switched-capacitor (SC) structure to replace the passive resistor in the RC network. In this topology, the resistance is emulated by periodically transferring charge through a switched capacitor driven by a clock signal. Because the circuit operates periodically and is time-variant, the analysis requires periodic steady-state (PSS) and periodic AC (PAC) simulations instead of conventional AC analysis.

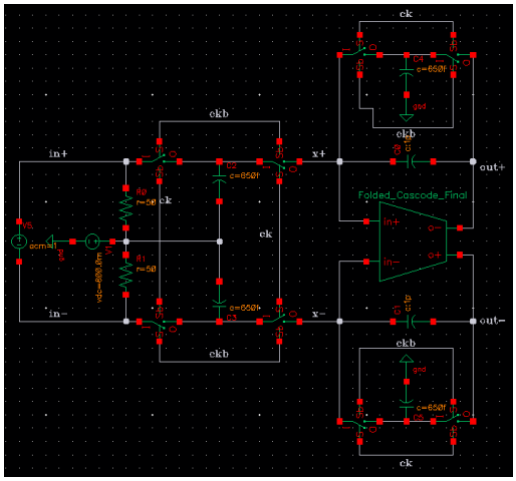


Figure 28: Schematic of a First Order Differential Active SC Filter

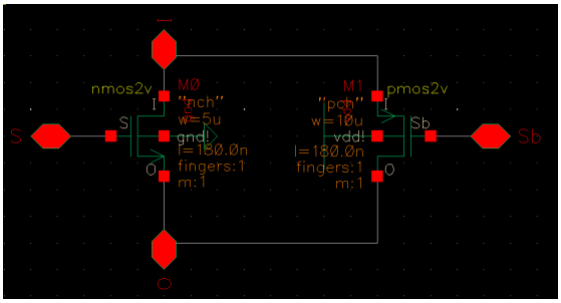


Figure 29: Transmission Gate Switch

Time-Variant Nature and Need for PSS/PAC Analysis

In a conventional RC filter, the resistor is a time-invariant element; therefore, standard AC analysis can be applied.

In contrast, the SC resistor is implemented using switching elements (here replaced by transmission gates), which open and close at high frequency, causing the circuit to have parameters that vary with time.

The system therefore becomes Linear Periodically Time-Varying (LPTV).

Because:

- The effective impedance only exists after time averaging over one clock cycle,
- The instantaneous circuit changes topology during switching events,
- And the AC small-signal operating point depends on the periodic solution,

the simulator cannot find a linearization point using standard .ac analysis.

Therefore:

- PSS (Periodic Steady State) finds the steady repeating waveform over each clock period.
- PAC (Periodic AC) linearizes the circuit around the PSS orbit and computes small-signal AC transfer characteristics.

Thus, PSS+PAC is the correct and standard method for analyzing switched-capacitor filters.

Equivalent Resistance of the Switched Capacitor

The SC resistor is implemented using:

- Two switches (transmission gates)
- One capacitor C

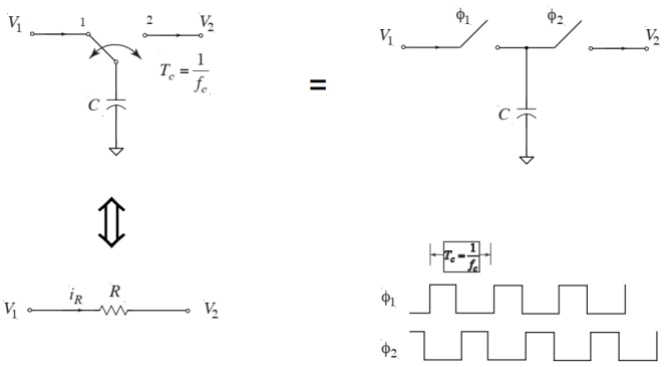


Figure 30: Equivalent Resistance

During each clock cycle of period TC, a charge packet is transferred from input to output. The average current equals the transferred charge divided by the clock period: $I = \frac{Q}{CT} = \frac{C(Vin-Vout)}{CT}$

This mimics Ohm's law: $I = \frac{(Vin-Vout)}{Req}$

Thus, the equivalent resistance of the SC network is: $Req = \frac{Tc}{C}$

or equivalently: $Req = \frac{1}{fclk\ C}$

Component Selection for Target Cutoff Frequency

To match the earlier RC design (where R=80 kΩ), the SC network must satisfy: $Req = 80k\Omega = \frac{Tc}{C}$
With initial capacitor value: C=1 pF

we obtain: $TC = Req \times C = 80k\Omega \times 1pF = 80ns$

corresponding to: $f_{clk} = \frac{1}{Tc} = 12.5MHz$

With these values, the expected cutoff is: $f\,c \approx \frac{1}{2\,\pi\,Req\,Cfilter} \approx 2Mhz$

However, simulations show that the actual cutoff frequency is noticeably higher than the theoretical value.

Reason for Higher-Than-Expected Cutoff Frequency

Several practical effects in switched-capacitor structures cause the effective resistance to become smaller than the ideal value, leading to a higher cutoff frequency:

Finite Switch Resistance (Ron) Reduces Effective Averaged Resistance

Transmission gates add a finite resistance Ron that is in series with the switched-capacitor resistance only part of the time.

This reduces the "overall averaged resistance," lowering Req and increasing fc.

Charge Injection and Clock Feedthrough Increase Effective Capacitance Transfer

More charge is transferred per cycle than predicted by the ideal Q=CΔV

Extra charge → higher equivalent current → lower Req → higher cutoff.

Non-ideal Clock Waveforms

Finite rise/fall times allow partial charge transfer outside the ideal switching window, again reducing the effective resistance.

Parasitic Capacitors in the Transmission Gate

These parasitics create additional coupling paths, effectively reducing the net RC time constant

Because of these effects, the actual equivalent resistance becomes: $R_{eq,real} < R_{eq,ideal}$

leading to: $f_{c,real} > f_{c,ideal}$

which matches the observed behavior in simulation.

Adjustment of Capacitor Value to Achieve 2 MHz Cutoff

To correct the increased cutoff frequency, the capacitor value was reduced: $C = 650\ fF$

Recomputing the equivalent resistance: $R_{eq} = \frac{Tc}{C} = \frac{80n}{650fF} \approx 123k\Omega$

This higher equivalent resistance compensates for the non-idealities and shifts the cutoff back toward the design target of 2 MHz, yielding a value consistent with simulation results.

Then the capacitor value was doubled, this is equivalent to the resistance being halved.

Simulation Results (PSS/PAC)

Using PSS+PAC:

- The magnitude plot confirms a **first-order roll-off of −20 dB/dec**, matching theoretical expectations.
- The cutoff frequency aligns with the adjusted design (≈ 2 MHz).
- The phase response follows first-order behavior, starting near 0° and approaching −90° at high frequencies.
- No inversion occurs (same as RC first-order case without negative gain).

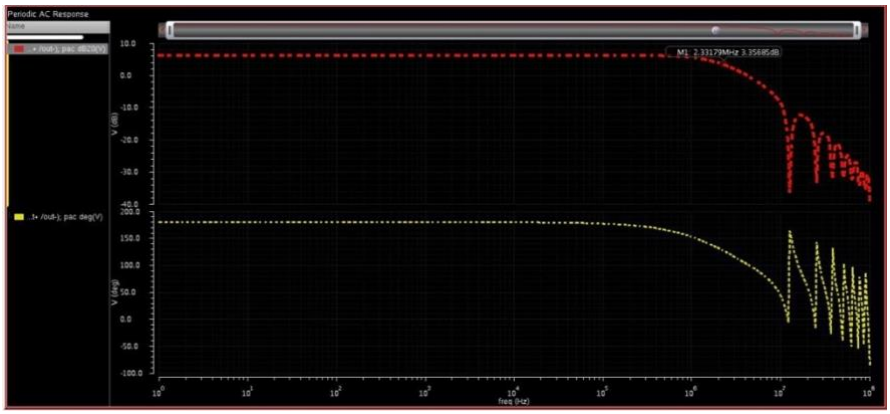


Figure 31: Simulation Result of a First Order Differential Active SC Filter

References:

Razavi, B. (2017). Design of analog CMOS integrated circuits. McGraw-Hill Education

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