Prelab Report: Constant Current Source Design

Arye Mindell
Loyola Marymount University, Department of Electrical Engineering and Computer Science

***Abstract*—This prelab report presents the design and simulation of a Widlar constant current source to supply a stable 1mA current. The circuit is analyzed under varying load resistances using MultiSim to verify its constant current characteristics. A parametric sweep analysis is conducted to determine the operational range of load resistance, ensuring stable current delivery.**

I. Introduction

Constant current sources are essential in analog circuit design, providing stable current regardless of variations in load resistance. They are often used to bias amplifiers or serve as an active load. This lab involves the design of a current mirror, which makes a perfect copy of a reference current. The particular design used here is a Widlar current mirror, which scales down the copy current in order to reduce sensitivity to variations in the reference current.[1]

II. Design

The Widlar current source consists of two NPN transistors from a CA3046 transistor array, a resistor R_1 which sets the reference current, and an emitter resistor R_E which adjusts the base-emitter voltage of Q_2 to lower the current output. The circuit layout is detailed in 1.

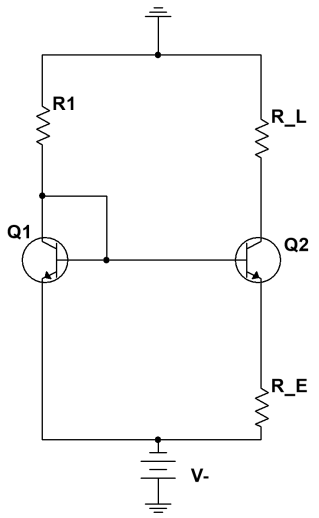

Fig. 1. Circuit layout of the Widlar constant current source using a CA3046 transistor array.

Since BJT transistors exhibit an exponential relationship between voltage and current, a small change in V_{BE} leads to a large difference in output current. Therefore the Voltage across R_E must be very small. Furthermore, since the collector current is specified at $1mA$, the value of R_E will be in the 100-Ohm range.

I_{REF} should be much larger than I_o in order to achieve the desired output stability, maintaining a total current below $20mA$ for safety and power purposes. Thus, I_{REF} is set to $12mA$.

The emitter resistance R_E is calculated by (1) where $I_{REF} = 12mA$ and $I_o = 1mA$, resulting in a value of 64.61Ω for R_E. [2]

$$R_E = \frac{V_T \ln(I_{REF}/I_o)}{I_o} \tag{1}$$

While there is no specification for the supply voltage, the value should remain below an absolute maximum of 20V. Furthermore, since the current source may be used in future amplifier designs, it should be designed to provide a maximal small-signal voltage swing. With this in mind, the upper supply is grounded while the lower supply is set to -15V. The Widlar resistor R_1 is given by (2) where $V_+ = 0V$, $V_- = -15V$, and $V_{BE1} = 0.7V$. This gives a value of $1.192k\Omega$ for R_1.

$$R_1 = \frac{V_+ - V_{BE1} - V_-}{I_{REF}} \tag{2}$$

III. Design Check

To validate the design, I_o, I_{REF} are determined by (3) and (4) using standard resistance values for R_1 and R_E.

$$I_{REF} = \frac{V_+ - V_{BE1} - V_-}{R_1} \tag{3}$$

$$I_o = \frac{V_T \ln(I_{REF}/I_o)}{R_E} \tag{4}$$

Substituting:

$$I_{REF} = \frac{0V - 0.7V - (-15V)}{1.2k\Omega} = 11.92mA \tag{5}$$

$$I_o = \frac{26mV \ln(11.92mA/I_o)}{62\Omega} \quad I_o = 1.03mA \tag{6}$$

This confirms that I_o is very close to $1mA$ and I_{REF} is much larger than I_o.

The maximum allowable load resistance is determined by the voltage drop that can be sustained across the load before the collector voltage falls below the base voltage and Q_2 enters saturation. This relationship is given by:

$$R_{L_{max}} = \frac{I_{REF} R_1}{I_o} \tag{7}$$

Substituting:

$$R_{L_{max}} = \frac{11.92mA \cdot 1.2k\Omega}{1.03mA} = 12.53k\Omega \tag{8}$$

Therefore, the design is validated to provide the specified output current for a load range of $0 - 12k\Omega$.

IV. Simulation and Analysis

The circuit is simulated in MultiSim to observe its performance over a range of load resistances. The following steps are performed:

1) DC analysis to verify the expected output current of 1mA.
2) Parameter sweep analysis for load resistance from 0 to $3 \times R_{L_{max}}$.

Fig. 2 displays the simulated DC operating point with a $1k\Omega$ load, confirming that the designed circuit provides a stable output current of approximately $1mA$ under nominal conditions.

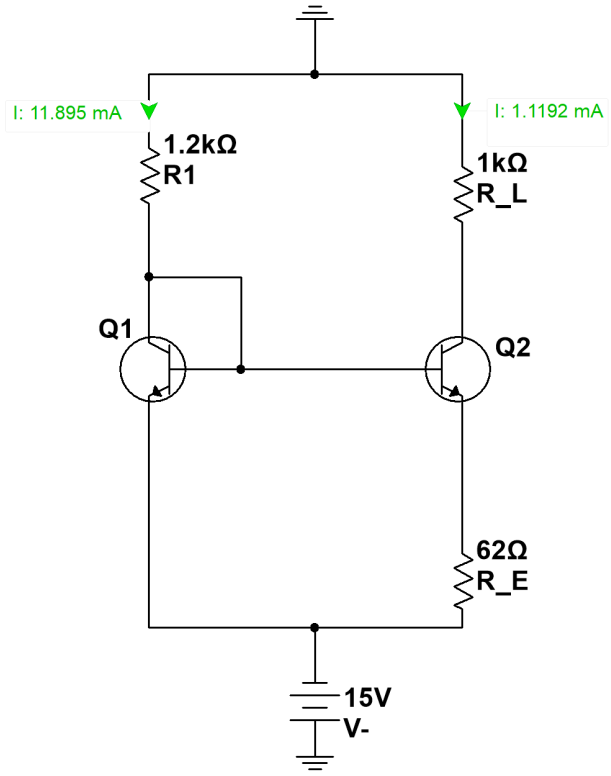

Fig. 2. Simulation results showing the DC operating point of the Widlar current source.

The results of the DC Analysis, displayed in Table I, show that the circuit operates as expected with no load, and with the maximum expected load of $12k\Omega$, while breaking down as expected at a load of $36k\Omega$, 3x the maximum.

TABLE I
Simulated Operating Point Values for Varying Load Resistances

Parameter	No Load	$R_L = 12k\Omega$	$R_L = 36k\Omega$
I_{REF} (mA)	11.895	11.895	11.897
I_O (mA)	1.122	1.084	0.413

A more detailed display of these results is shown in Fig. 3, which shows the output current plotted as a function of load resistance. The output current is a stable $1mA$ for a load resistance of up to $12k\Omega$. As the load resistance continues to increase past this point, the output current drops steeply as Q_2 enters saturation.

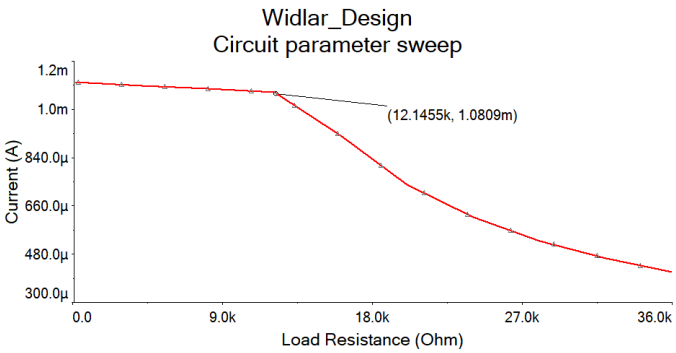

Fig. 3. Simulation results of the Widlar constant current source showing output current stability over varying load resistances.

V. Expected Results

The implemented circuit is expected to demonstrate:

- A stable 1mA current over a range of load resistances.
- Deviation in current for excessively high load resistances.
- A clear operational limit for the designed current source.

VI. Conclusion

The prelab provides a theoretical framework and simulation approach for designing a Widlar current source. The expected results will validate the design's effectiveness, ensuring a stable current output within a specified load resistance range.

References

[1] Loyola Marymount University, Department of Electrical Engineering and Computer Science, "EECE3200 Lab 4: Constant Current Source," 2025.

[2] D. A. Neamen, *Microelectronics: Circuit Analysis and Design*, 4th ed. New York, NY: McGraw-Hill, 2010, sec. 10.1.