

# LM3046 Transistor Array

Check for Samples: LM3046

## **FEATURES**

- Two Matched Pairs of Transistors
  - V<sub>BE</sub> Matched ±5 mV
  - Input Offset Current 2  $\mu$ A Max at I<sub>C</sub> = 1 mA
- Five General Purpose Monolithic transistors
- Operation from DC to 120 MHz
- Wide Operating Current Range
- Low Noise Figure: 3.2 dB typ at 1 kHz

## **APPLICATIONS**

- General Use in All Types of Signal Processing Systems Operating Anywhere in the Frequency Range from DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

## **DESCRIPTION**

The LM3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3046 is supplied in a 14-lead SOIC package.

## **Schematic and Connection Diagram**

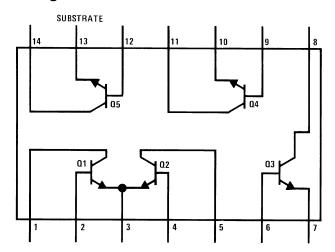


Figure 1. SOIC Package
Top View
See Package Number D (R-PDSO-G14)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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# Absolute Maximum Ratings(1)(2)(3)

		Each Transistor	Total Package	Units	
	T <sub>A</sub> = 25°C	300	750		
	T <sub>A</sub> = 25°C to 55°C	300	750	mW	
Power Dissipation	T <sub>A</sub> > 55°C	Derate a	mW/°C		
	T <sub>A</sub> = 25°C to 75°C			mW	
	T <sub>A</sub> > 75°C			mW/°C	
Collector to Emitter Voltage, V <sub>CEO</sub>	15				
Collector to Base Voltage, V <sub>CBO</sub>		20		.,	
Collector to Substrate Voltage, V <sub>CIO</sub> <sup>(4)</sup>		20		V	
Emitter to Base Voltage, V <sub>EBO</sub>		5			
Collector Current, I <sub>C</sub>		50		mA	
Operating Temperature Range		-40°C to	+85°C		
Storage Temperature Range		-65°C to	+85°C		
	Dual-In-Line Package Soldering (10 Sec.)	260°C			
Coldering Information	SOIC Package				
Soldering Information	Vapor Phase (60 Seconds)	215°C			
	Infrared (15 Seconds)	220°C			

<sup>(1) &</sup>quot;Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

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<sup>(2)</sup> See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

<sup>(3)</sup> If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

<sup>(4)</sup> The collector of each transistor is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



## Electrical Characteristics(1)

Parameter	Conditions	Min	Тур	Max	Units
Collector to Base Breakdown Voltage (V <sub>(BR)CBO</sub> )	$I_C = 10 \ \mu A, \ I_E = 0$	20	60		V
Collector to Emitter Breakdown Voltage (V <sub>(BR)CEO</sub> )	$I_C = 1 \text{ mA}, I_B = 0$	15	24		V
Collector to Substrate Breakdown Voltage (V <sub>(BR)CIO</sub> )	$I_C = 10 \mu A, I_{CI} = 0$	20	60		V
Emitter to Base Breakdown Voltage (V <sub>(BR)EBO</sub> )	I <sub>E</sub> 10 μA, I <sub>C</sub> = 0	5	7		V
Collector Cutoff Current (I <sub>CBO</sub> )	V <sub>CB</sub> = 10V, I <sub>E</sub> = 0		0.002	40	nA
Collector Cutoff Current (I <sub>CEO</sub> )	$V_{CE} = 10V, I_B = 0$			0.5	μA
	$V_{CE} = 3V$ $I_{C} = 10 \text{ mA}$		100		
Static Forward Current Transfer Ratio (Static Beta) (hFE)	$I_C = 1 \text{ mA}$	40	100		
	I <sub>C</sub> = 10 μA		54		
Input Offset Current for Matched Pair $Q_1$ and $Q_2 \mid I_{O1} - I_{IO2} \mid$	$V_{CE} = 3V$ , $I_C = 1$ mA		0.3	2	μΑ
Door to Fasition Valtage (V.)	$V_{CE} = 3V$ $I_{E} = 1 \text{ mA}$		0.715		V
Base to Emitter Voltage (V <sub>BE</sub> )	$I_E = 10 \text{ mA}$		0.800		
Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $	V <sub>CE</sub> = 3V, I <sub>C</sub> = 1 mA		0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors  V <sub>BE3</sub> - V <sub>BE4</sub>  ,  V <sub>BE4</sub> - V <sub>BE5</sub>  ,  V <sub>BE5</sub> - V <sub>BE3</sub>	V <sub>CE</sub> = 3V, I <sub>C</sub> = 1 mA		0.45	5	mV
Temperature Coefficient of Base to Emitter Voltage					
$\left(\frac{\Delta V_{BE}}{\Delta T}\right)$ (1)	$V_{CE} = 3V$ , $I_C = 1$ mA		-1.9		mV/°C
Collector to Emitter Saturation Voltage (V <sub>CE(SAT)</sub> )	I <sub>B</sub> = 1 mA, I <sub>C</sub> = 10 mA		0.23		V
Temperature Coefficient of Input Offset Voltage					
$\left(\frac{\Delta V_{10}}{\Delta T}\right)$ (2)	V <sub>CE</sub> = 3V, I <sub>C</sub> = 1 mA		1.1		μV/°C
Low Frequency Noise Figure (NF)	$f = 1 \text{ kHz}, V_{CE} = 3V, I_{C} = 100$ $\mu A, R_{S} = 1 \text{ k}\Omega$		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRC	JIT CHARACTERISTICS	1.			"
Forward Current Transfer Ratio (hfe)			110		
Short Circuit Input Impednace (hie)	f = 1 kHz, V <sub>CE</sub> = 3V, I <sub>C</sub> = 1		3.5		kΩ
Open Circuit Output Impedance (hoe)	mA		15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (hre)			1.8 x 10 <sup>-4</sup>		
ADMITTANCE CHARACTERISTICS		1.			"
Forward Transfer Admittance (Y <sub>fe</sub> )			31 - j 1.5		
Input Admittance (Yie)			0.3+J 0.04		
Output Admittance (Yoe)	$f = 1 \text{ MHz}, V_{CE} = 3V, I_{C} = 1$ mA		0.001+j 0.03		
Reverse Transfer Admittance (Y <sub>re</sub> )			See Figure 16		
Gain Bandwidth Product (f <sub>T</sub> )	$V_{CE} = 3V, I_{C} = 3 \text{ mA}$	300	550		
Emitter to Base Capacitance (C <sub>EB</sub> )	$V_{EB} = 3V, I_{E} = 0$		0.6		pF
Collector to Base Capacitance (C <sub>CB</sub> )	$V_{CB} = 3V, I_{C} = 0$		0.58		pF
Collector to Substrate Capacitance (C <sub>Cl</sub> )	$V_{CS} = 3V, I_{C} = 0$		2.8		pF

<sup>(1)</sup>  $(T_A = 25^{\circ}C \text{ unless otherwise specified})$ 



## **Typical Performance Characteristics**

### Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor

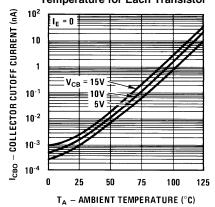


Figure 2.

# Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors $\mathbf{Q}_1$ and $\mathbf{Q}_2$ vs Emitter Current

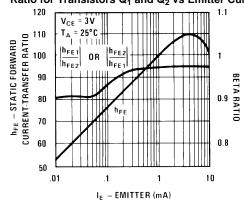
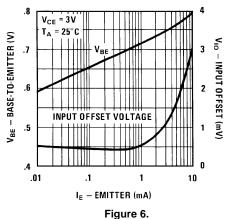


Figure 4.

# Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

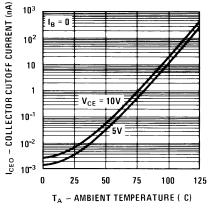
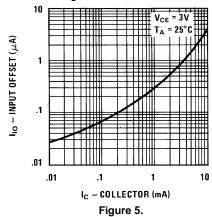


Figure 3.

# Typical Input Offset Current for Matched Transistor Pair $\mathbf{Q}_1$ vs Collector Current



### Typical Base To Emitter Voltage Characteristic forEach Transistor vs Ambient Temperature

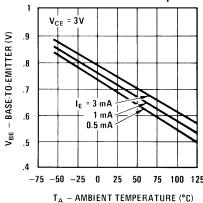


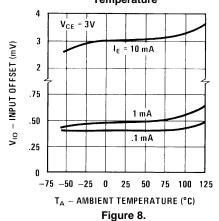
Figure 7.

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## Typical Performance Characteristics (continued)

# Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature



**Typical Noise Figure vs Collector Current** 

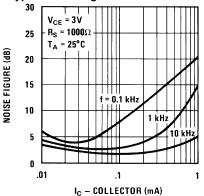


Figure 10.

# Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

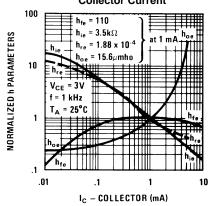
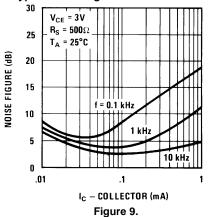
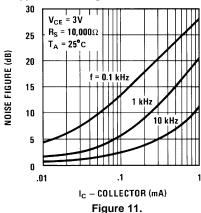


Figure 12.

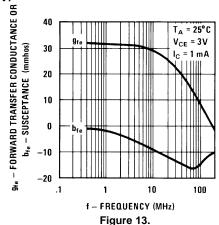
## **Typical Noise Figure vs Collector Current**



**Typical Noise Figure vs Collector Current** 

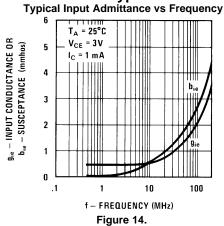


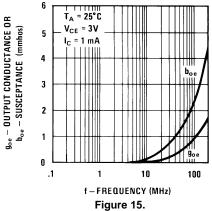
Typical Forward Transfer Admittance vs Frequency



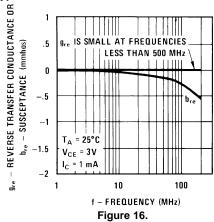


# Typical Performance Characteristics (continued) mittance vs Frequency Typical Output Admittance vs Frequency





## Typical Reverse Transfer Admittance vs Frequency



## Typical Gain-Bandwidth Product vs Collector Current

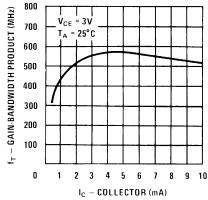


Figure 17.

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## **REVISION HISTORY**

Cł	hanges from Revision A (March 2013) to Revision B	Page
•	Changed layout of National Data Sheet to TI format	4





11-Aug-2017

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
LM3046M	LIFEBUY	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM3046M	
LM3046M/NOPB	LIFEBUY	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM3046M	
LM3046MX/NOPB	LIFEBUY	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM3046M	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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11-Aug-2017

## PACKAGE MATERIALS INFORMATION

www.ti.com 2-Sep-2015

## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



## \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3046MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

www.ti.com 2-Sep-2015



## \*All dimensions are nominal

ĺ	Device	Package Type	ckage Type Package Drawing Pins		SPQ	Length (mm)	Width (mm)	Height (mm)	
I	LM3046MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0	

# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



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