Prelab Report: Multi-Stage BJT Amplifier Design

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***Abstract*—This report presents the design and simulation of a multi-stage BJT amplifier. The goal is to achieve a voltage gain of at least 100 while satisfying input and output resistance constraints. The amplifier is designed to operate within specified supply voltage and current limits while ensuring symmetrical output swing. Simulations in MultiSim validate the design under varying transistor parameters, and AC analysis confirms the required gain and impedance characteristics.**

I. Introduction

THIS lab focuses on designing and analyzing the characteristics of multi-stage BJT amplifiers. The objective is to meet specified performance criteria, including voltage gain, input resistance, and output resistance, while maintaining power efficiency and maximizing the undistorted output swing. The design process involves selecting appropriate biasing and coupling components to ensure stable operation across different transistor parameter variations.

II. Design Specifications

The amplifier must satisfy the following constraints:

- Voltage gain $|A_v| \geq 100$
- Load resistance $R_L = 10k\Omega$
- Input resistance $R_{in} \geq 600\Omega$
- Output resistance $R_{out} \leq 8\Omega$
- Transistor current gain range: $150 \leq \beta \leq 250$
- Maximum supply voltage: $V_{CC} = 15V$
- Maximum supply current: $I_{supply} = 20mA$
- Symmetrical output voltage swing
- Standard resistor and capacitor values

III. Design

The amplifier circuit, shown in Figure 1, implements a two-stage cascaded amplifier topology, with a common emitter stage followed by an emitter-follower stage.

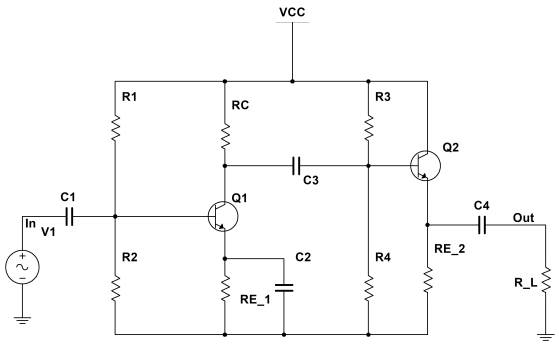

Fig. 1. Two-stage Amplifier Circuit.

. To meet the design constraints, the operating points for the transistors were set at $V_{CE1} = 4.5V$, $I_{C1} = 6mA$ for the first stage, and $V_{CE2} = 13V$, $I_{C2} = 6mA$ for the second stage. The first-stage transistor utilizes approximately one-third of the supply voltage, while the second-stage transistor operates at two-thirds to ensure proper signal amplification.

The collector resistor for each stage was chosen to achieve the desired voltage gain using the relation $A_v = g_m R_C$, ensuring a sufficient margin for variations in component values. Biasing resistors were selected to draw approximately one-tenth of the collector current as a general rule of thumb. However, for the second stage, biasing resistances were increased to minimize gain degradation caused by the loading effect while maintaining compliance with the output resistance constraint. This relationship is defined by:

$$R_{out} \leq R_E 2 \parallel \left(\frac{V_T}{I_{C2}} + \frac{R_{th} \parallel R_{C1}}{\beta + 1} \right) \tag{1}$$

Large coupling capacitors were incorporated at key circuit locations to decouple the AC signal from the DC biasing conditions. Since no strict constraints were placed on capacitor sizes, they were selected to be sufficiently large to avoid signal attenuation. However, in practical implementation, smaller components may be substituted based on availability.

TABLE I
Component Values Used in Design

Component	Value
R_C	620Ω
$R_E 1$	1.2 kΩ
$R_E 2$	240 Ω
R_1	90 kΩ
R_2	200 kΩ
R_3	200 kΩ
R_4	90 kΩ
Coupling Capacitors	Large (TBD)

IV. Design Validation

To validate the design, nominal component values were substituted into output resistance and gain equations, ensuring that all specifications were met.

Substituting the updated values into the gain and impedance equations:

The voltage gain of the first stage is given by:

$$A_{v1} = g_{m1} R_C = \left(\frac{I_{C1}}{V_T} \right) R_C \tag{2}$$

where $V_T \approx 25mV$, $I_{C1} = 6mA$, and $R_C = 620\Omega$. Substituting:

$$A_{v1} = \left(\frac{6mA}{25mV} \right) \times 620\Omega = 148.8 \tag{3}$$

For the second stage (emitter follower), the voltage gain is:

$$A_{v2} = \frac{R_E2}{\frac{1}{g_{m2}} + R_E2} \tag{4}$$

where $R_E2 = 240\Omega$ and $g_{m2} = I_{C2}/V_T = 6mA/25mV = 0.24S$. Substituting:

$$A_{v2} = \frac{240\Omega}{\frac{1}{0.24S} + 240\Omega} = \frac{240\Omega}{4.167\Omega + 240\Omega} = 0.983 \tag{5}$$

The total gain is:

$$A_v = A_{v1} \times A_{v2} = 148.8 \times 0.983 = 146.2 \tag{6}$$

The output resistance is:

$$R_{out} = R_E2 \parallel \left(\frac{V_T}{I_{C2}} + \frac{R_{th} \parallel R_C}{\beta + 1} \right) \tag{7}$$

where $R_E2 = 240\Omega$, $R_C = 620\Omega$, and assuming $\beta = 150$:

$$R_{out} = 240\Omega \parallel \left(\frac{25mV}{6mA} + \frac{90k\Omega \parallel 200k\Omega \parallel 620\Omega}{151} \right) \tag{8}$$

$$R_{out} = 240\Omega \parallel (4.167\Omega + 3.98\Omega) = 4.83\Omega \tag{9}$$

The input resistance is:

$$R_{in} = R_1 \parallel R_2 \parallel r_{\pi 1} \tag{10}$$

where $r_{\pi 1} = \frac{\beta V_T}{I_{C1}} = \frac{150 \times 25mV}{6mA} = 625\Omega$. Substituting:

$$R_{in} = 90k\Omega \parallel 200k\Omega \parallel 625\Omega \tag{11}$$

$$R_{in} = 890\Omega \tag{12}$$

These calculations confirm that the design meets the required specifications.

V. Simulation and Expected Results

The designed amplifier was simulated in MultiSim to verify performance under varying transistor parameters. Using the Bode Plotter tool, gain and frequency response were analyzed from 10Hz to 100kHz. The results confirm that the midband gain satisfies the specification across the range of beta values.

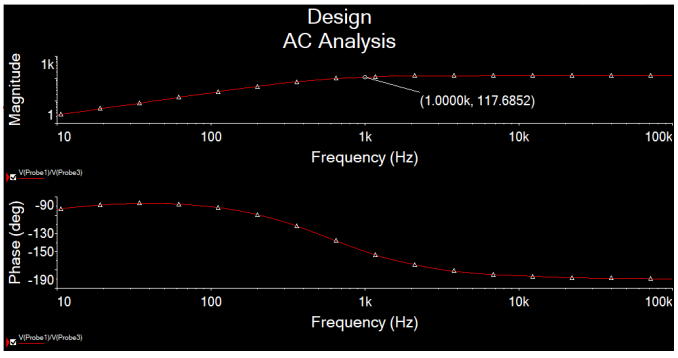

Fig. 2. Midband Gain (Beta = 150)

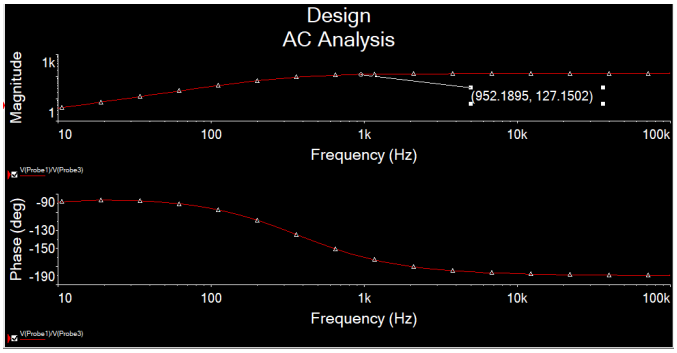

Fig. 3. Midband Gain (Beta = 250)

The input resistance was evaluated by the ratio of input voltage to input current. The results show that the input resistance satisfies the constraint across the range of beta values.

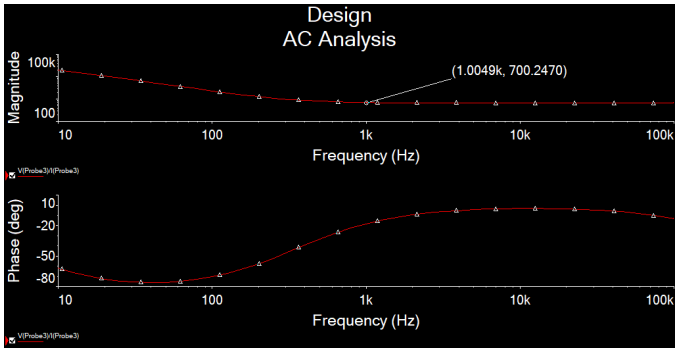

Fig. 4. Input Impedance (Beta = 150)

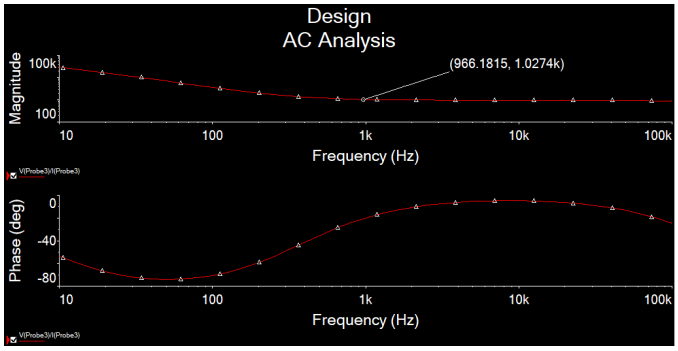

Fig. 5. Input Impedance (Beta = 250)

Simulation results will be compared against theoretical calculations to confirm compliance with design requirements.

The output resistance will be calculated by measuring the loading effect of the 10 kΩ load on the output voltage. The maximum voltage swing will be observed by applying a sinusoidal input and increasing the amplitude until noticeable clipping occurs, ensuring that the output remains within the designed limits.

In simulation, the output resistance was confirmed to satisfy the specification: $R_{out} < 8\Omega$. The maximum voltage swing was also evaluated in transient analysis, showing symmetrical

operation without significant distortion. The simulation determined that the maximum symmetric swing of the amplifier is approximately $\pm 2V$, ensuring proper signal amplification while avoiding saturation or cutoff regions.

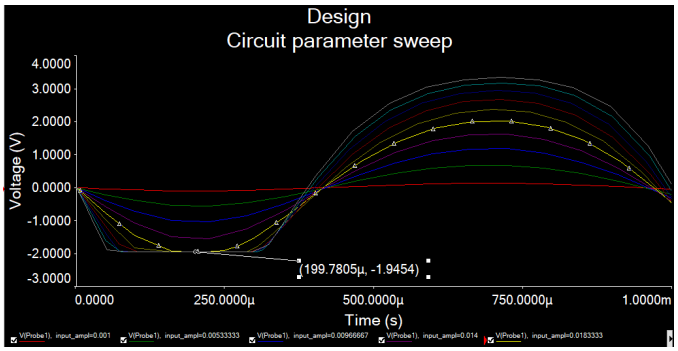

Fig. 6. Transient Analysis of Maximum Symmetrical Voltage Swing

VI. Conclusion

This prelab outlines the methodology for designing a multi-stage BJT amplifier that meets specified electrical requirements. The simulation approach ensures that the amplifier operates correctly under varying conditions, and further experimental validation will confirm its real-world performance.

References

[1] Loyola Marymount University, Department of Electrical Engineering and Computer Science, "EECE 3200: Lab 3 - Multi-Stage BJT Amplifier Design," Spring 2025.