Prelab Report: Multi-Stage BJT Amplifier Design

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***Abstract*—This report presents the design and simulation of a BJT amplifier. The goal is to achieve a voltage gain of at least 100 while satisfying input and output resistance constraints. The amplifier is designed to operate within specified supply voltage and current limits while ensuring symmetrical output swing. Simulations in MultiSim validate the design under varying transistor parameters, and AC analysis confirms the required gain and impedance characteristics.**

I. Introduction

THIS lab focuses on designing and analyzing the characteristics of a BJT amplifier. The objective is to meet specified performance criteria, including voltage gain, input resistance, and output resistance, while maintaining power efficiency and maximizing the undistorted output swing. The design process involves selecting appropriate biasing and coupling components to ensure stable operation across different transistor parameter variations.

II. Design Specifications

The amplifier must satisfy the following constraints:

- Voltage gain $|A_v| \geq 100$
- Load resistance $R_L = 10k\Omega$
- Input resistance $R_{in} \geq 600\Omega$
- Output resistance $R_{out} \leq 8\Omega$
- Transistor current gain range: $150 \leq \beta \leq 250$
- Maximum supply voltage: $V_{CC} = 15V$
- Maximum supply current: $I_{supply} = 20mA$
- Symmetrical output voltage swing
- Standard resistor and capacitor values

III. Design Process

Due to the tight constraint on the output resistance and high gain requirement, a cascaded multi-stage amplifier is needed. The topology is shown in Fig. 1.

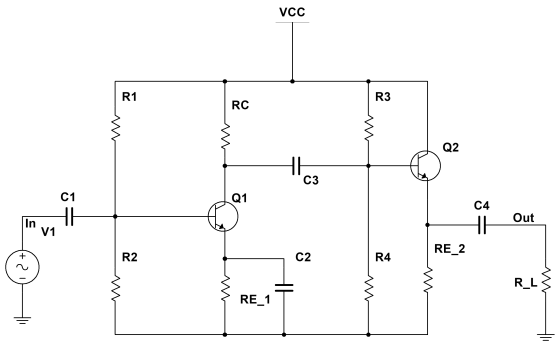

Fig. 1. Two-stage Amplifier Circuit.

The first stage is a Common-Emitter Amplifier, which can achieves a high gain while meeting the input resistance requirement. The second stage is an Emitter-Follower, which reduces the output resistance by roughly a factor of beta (two orders of magnitude), enabling the design to meet the tight output resistance requirement.

The output resistance of the circuit is given by:

$$R_{out} = R_E2 \parallel \left(1/g_{m2} + \frac{R_{in2} \parallel R_C}{\beta + 1}\right) \tag{1}$$

R_{E2} can be neglected since it is much larger than the second term in the equation. Half of the output resistance budget is allocated to $1/g_{m2}$ with a safety margin of 3/4:

$$\frac{1}{g_{m2}} = I_{C2}/V_T = 0.75 \times \left(\frac{R_{out}}{2}\right) \tag{2}$$

Solving for I_{C2}:

$$I_{C2} = \frac{26mV}{1.33 \times (4\Omega)} = 8.67mA \tag{3}$$

The remaining output resistance is split between the first stage's output resistance and the second stage's input resistance, which are matched to maximize power transfer between stages.

$$R_C = R_{in2} = 2 * (\beta + 1) \times (4\Omega) = 1.208k\Omega \tag{4}$$

To maximize symmetrical output swing of the second stage, the supply voltage is split evenly between V_{CE2} and V_{E2}, and R_{E2} is calculated by Ohm's law:

$$V_{CE2} = V_{E2} = \frac{V_{CC}}{2} = 7.5V, \quad R_{E2} = \frac{V_{E2}}{I_{C2}} = 865.4\Omega \tag{5}$$

The values of R_3 and R_4 are calculated to bias the transistor while setting the input resistance as specified above.

$$V_{th} = V_{E2} + V_{BE\_On} = 8.2V, \quad R_{th} = Rin2 = 1.2k\Omega \tag{6}$$

$$V_{th} = \frac{R_4}{R_3 + R_4} V_{CC}, \quad R_{th} = R_3 \parallel R_4 \tag{7}$$

Solving for R_3 and R_4:

$$R_3 = 2.66k\Omega, \quad R_4 = 2.21k\Omega \tag{8}$$

For the second stage (emitter follower), the voltage gain is:

$$A_{v2} = \frac{R_{E2}}{\frac{1}{g_{m2}} + R_{E2}} \tag{9}$$

Substituting:

$$A_{v2} = \frac{865.4\Omega}{\frac{1}{0.33S} + 865.4\Omega} = 0.996V/V \tag{10}$$

The lower bound for the current I_{C1} is set by the voltage gain requirement:

$$A_v = A_{v2} \cdot g_{m1} \left(R_C \parallel R_{in2} \right) \tag{11}$$

$$A_v = 0.996 \cdot g_{m1} \cdot 604\Omega = 105V/V \tag{12}$$

Solving for trans-conductance and current:

$$g_{m1} = 0.176S = \frac{I_{C1}}{V_T}, \quad I_{C1,min} = 4.53mA \tag{13}$$

The upper bound for the current I_{C1} is set by the input resistance requirement:

$$Rin \approx r_\pi = \frac{\beta * I_{C1}}{V_T} \tag{14}$$

$$I_{C1,max} = \frac{V_T \cdot R_{in}}{\beta} = \frac{26mV \cdot 604\Omega}{150} \cdot = 6.5mA \tag{15}$$

The range for I_{C1} is $4.53mA$ to $6.5mA$. I_{C1} is set to $5mA$, on the low end of the range to ensure that the input resistance is specification is met.

V_{RC1} is calculated by Ohm's law, and V_{CE1} is set to maximize the symmetric voltage swing of the first stage:

$$V_{RC1} = I_{C1} \cdot R_C, \quad V_{CE1} = V_{RC1} + V_{CE,Sat} \tag{16}$$

$$V_{RC1} = 6.07V, \quad V_{CE1} = 6.67 \tag{17}$$

From KVL and Ohm's Law:

$$V_{E1} = V_{CC} - V_{RC1} - V_{CE1} = 2.26V \tag{18}$$

$$R_{E1} = \frac{V_{E1}}{I_{C1}} = 448.7\Omega \tag{19}$$

The values of R_1 and R_2 are calculated to bias the transistor while drawing roughly ten times the base current

$$V_{th} = V_{E1} + V_{BE\_On} = 2.96V, \frac{V_{CC}}{R1 + R2} = 10 \times \frac{I_{C1}}{\beta} \tag{20}$$

$$V_{th} = \frac{R_2}{R_1 + R_2} V_{CC}, \quad R_{th} = R_1 \parallel R_2 \tag{21}$$

Solving for R_1 and R_2:

$$R_1 = 35.9k\Omega, R_2 = 8.82k\Omega \tag{22}$$

The final values, after being adjusted to standard component sizes, are listed in Table I:

TABLE I
COMPONENT VALUES

Component	Value
R_C	1.2kΩ
R_{E1}	430Ω
R_{E2}	820Ω
R_1	36kΩ
R_2	8.9kΩ
R_3	2.2kΩ
R_4	2.7kΩ
Coupling Capacitors	Large (TBD)

IV. DESIGN VALIDATION

To validate the design, the nominal component values were substituted into the gain and impedance equations, ensuring that all specifications were met. The design calculations were performed using MATLAB.

A. Current Limit

Using KVL, we calculate the actual value of the current I_{C1}:

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{BE,on} + I_{C1} R_{E1}, \quad I_{C1} = 5.29mA \tag{23}$$

Similarly for I_{C2}:

$$\frac{R_4}{R_3 + R_4} V_{CC} = V_{BE,on} + I_{C2} R_{E2}, \quad I_{C2} = 7.56mA \tag{24}$$

The biasing currents are given by Ohm's law:

$$I_{B1} = \frac{V_{CC}}{R_1 + R_2} = 334\mu A \tag{25}$$

$$I_{B2} = \frac{V_{CC}}{R_3 + R_4} = 3.06mA \tag{26}$$

Thus the total current is $16.25mA$ which falls within the $20mA$ specification.

B. Voltage Gain

The voltage gain of the first stage is given by:

$$A_{v1} = g_{m1}(R_C \parallel R_{in}) \tag{27}$$

where $g_{m1} = I_{C1}/V_T = 0.186S$. Substituting:

$$A_{v1} = 0.203S \times 600\Omega = 121.8V/V \tag{28}$$

For the second stage (emitter follower), the voltage gain is:

$$A_{v2} = \frac{R_{E2}}{\frac{1}{g_{m2}} + R_{E2}} \tag{29}$$

where $g_{m2} = 0.291S$. Substituting:

$$A_{v2} = \frac{820\Omega}{\frac{1}{0.291S} + 820\Omega} = 0.996V/V \tag{30}$$

The total gain is:

$$A_v = A_{v1} \times A_{v2} = 121.8 \times 0.996 = 121.4V/V \tag{31}$$

This satisfies the gain specification, $|A_v| \geq 100$.

C. Output Resistance

The output resistance is:

$$R_{out} = R_{E2} \parallel \left(\frac{1}{g_{m2}} + \frac{R_{th} \parallel R_C}{\beta + 1} \right) \tag{32}$$

where $R_{E2} = 820\Omega$, $R_C = 1.2k\Omega$, and assuming $\beta = 150$:

$$R_{out} = 820\Omega \parallel (3.44\Omega + 4.02\Omega) = 7.46\Omega \tag{33}$$

This satisfies the specification, $R_{out} \leq 8\Omega$

D. Input Resistance

The input resistance is:

$$R_{in} = R_1 \parallel R_2 \parallel r_{\pi 1} \tag{34}$$

where $r_{\pi 1} = \frac{\beta V_T}{I_{C1}} = \frac{150 \times 26mV}{5.28mA} = 739\Omega$. Substituting:

$$R_{in} = 8.9k\Omega \parallel 36k\Omega \parallel 739\Omega = 700\Omega \tag{35}$$

This satisfies the specification, $Rin \geq 600\Omega$.

These results confirm that the circuit meets the following requirements:

- Total Current: Remained below $20mA$
- Voltage Gain: Verified to be greater than 100.
- Output Resistance: Maintained below 8Ω.
- Input Resistance: Verified to exceed 600Ω.

V. Simulation and Expected Results

The designed amplifier was simulated in MultiSim to verify performance under varying transistor parameters. Using a parameter sweep, gain was analyzed at 10 kHz for β values between 150 and 250. The results in Fig. 2 confirm that the midband gain satisfies the specification across the range of β values.

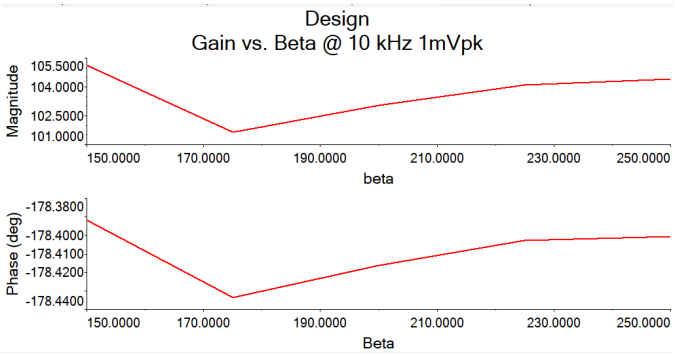

Fig. 2. Midband Gain vs. Beta

The input resistance was evaluated by the ratio of input voltage to input current, using a test voltage of $1mVpk$ at 10 kHZ, with β values between 150 and 250. The results in Fig. 3 show that the input resistance satisfies the constraint across the range of β values.

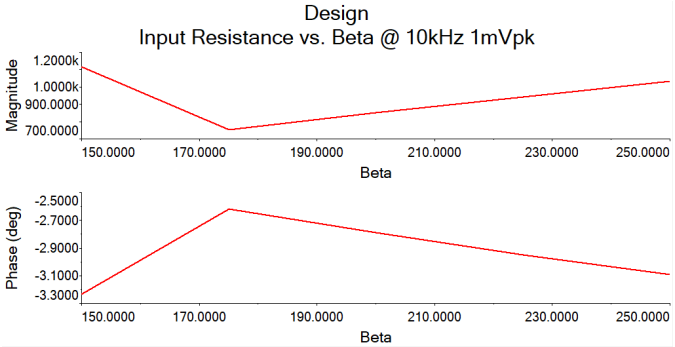

Fig. 3. Midband Input Resistance vs. Beta

The output resistance will be calculated by measuring the loading effect of the 10 kΩ load on the output voltage. The maximum voltage swing will be observed by applying a sinusoidal input and increasing the amplitude until noticeable clipping occurs, ensuring that the output remains within the designed limits.

The output voltage swing was tested through a range of input voltages between $1mV$ and $70mV$. The transient analysis shown in Fig. 4 shows symmetrical operation without significant distortion up to about 4V at the output. Therefore the maximum symmetric swing of the amplifier is above $\pm 4V$, although the output is less symmetrical than expected. This could be due to phase shifts created by the two-stage design.

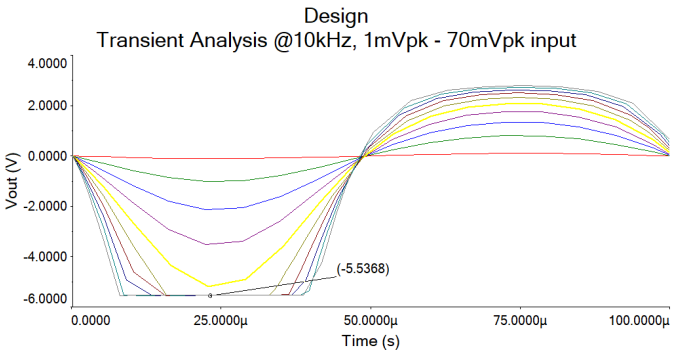

Fig. 4. Transient Analysis of Maximum Symmetrical Voltage Swing

VI. Conclusion

This prelab outlines the methodology for designing a multi-stage BJT amplifier that meets specified electrical requirements. The simulation approach ensures that the amplifier operates correctly under varying conditions, and further experimental validation will confirm its real-world performance.

References

[1] Loyola Marymount University, Department of Electrical Engineering and Computer Science, "EECE 3200: Lab 3 - Multi-Stage BJT Amplifier Design," Spring 2025.