Prelab Report: Operational Amplifier Design

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***Abstract*—This prelab report presents the design and simulation of an operational amplifier (op-amp) that meets specified gain, input resistance, and output impedance constraints. Simulations are conducted to verify key parameters, including gain, bandwidth, and voltage swing.**

I. Introduction

This lab involves designing a two-stage op-amp with a differential amplifier input stage, ensuring high input impedance and controlled gain, followed by a gain stage that enhances the voltage amplification. The design must meet the following constraints:[1]

- Small-signal voltage gain: $400 \leq A_d \leq 500$
- Input resistance: $R_{id} \geq 20k\Omega$
- Output resistance: $R_o \leq 200\Omega$
- Load resistance: $R_L = 200\Omega$
- Low-frequency cutoff: $f_{L3dB} \leq 100Hz$
- Maximum peak-to-peak output swing: $V_{o,p-p} \geq 2V$
- Offset voltage: $|V_{\text{offset}}| \leq 0.01V$

II. System Description

The operational amplifier consists of multiple stages designed to achieve high gain, low output impedance, and stability. The key components include a differential amplifier, a common-emitter gain stage, a level shifter, and an emitter follower output stage. The complete circuit layout is shown in Fig. 1.

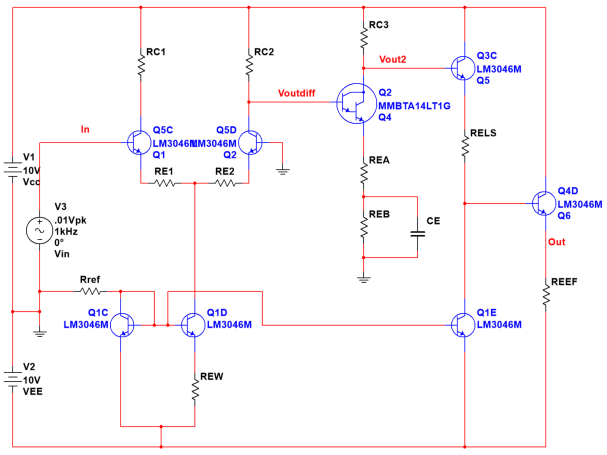

Fig. 1. Circuit layout of the designed operational amplifier.

1) **Differential Amplifier:** The first stage is a differential amplifier, which serves as a primary gain stage while also filtering common-mode noise. This stage is designed to provide high input impedance and a stable reference for signal amplification. A Widlar current source is used to bias this stage, ensuring a predictable and stable operating point.
2) **Common-Emitter Stage:** The second stage consists of a common-emitter (CE) amplifier, which provides additional voltage gain. A Darlington pair configuration is used to isolate the output resistance of the CE stage from the next stage, preventing excessive loading effects.
3) **Level Shifter:** A level shifter stage is introduced to remove the DC offset caused by the biasing of the previous stages. This ensures that the output voltage remains centered around the desired reference level, preventing distortion and maximizing the usable output swing. This stage is biased by a standard current mirror, sharing a reference current with the Widlar biasing of the first stage.
4) **Emitter Follower Output Stage:** The final stage is an emitter follower, which significantly reduces the output resistance, ensuring that the amplifier can drive low-impedance loads effectively while maintaining the designed gain characteristics.

III. Design

A. Biasing Currents

To ensure that the output swing at the emitter follower exceeds $1Vpk$, the small-signal voltage at the emitter of Q_5 must be greater than 1V, as given by:

$$I_{E5}(R_{E5} \parallel R_L) \geq 1V \tag{1}$$

The value of R_{E5} must be significantly larger than 200Ω in order to achieve a DC voltage drop of 10V from the emitter to VEE with a practical supply current. Assuming $R_{E5} \geq 200\Omega$:

$$\frac{1V}{200\Omega \parallel 200\Omega} = \frac{1V}{100\Omega} = 10mA \leq I_{E5} \tag{2}$$

To provide a safety margin for output swing,

$$I_{E5} = 12.5mA \tag{3}$$

Due to the high input resistance requirement, the differential pair emitter current I_{E1} will be in the microamp range, giving a total I_{EE} of $\approx 1mA$.

The level shifter must produce a significant voltage drop across its emitter resistor to compensate for the DC shift introduced by prior stages. The resistor R_{E4} also affects the output resistance by being reflected through Q_5 and scaled by a factor of β. Thus, I_{E4} must be large enough to generate a substantial voltage drop across R_{E4} while keeping its resistance in the 10kΩ range. Since the level shifter is biased

by a current mirror, I_{E4} must match the reference current I_{REF}, and both must share the remaining current budget of 6.5mA with the biasing current of the CE stage.

$$I_{E4} = I_{REF} = 2mA \tag{4}$$

I_{E4} and I_{REF} are set to 2mA, leaving 2.5mA for biasing the CE stage.

The current I_{C3} in the CE stage influences both gain and maximum symmetrical swing. The gain can be adjusted by modifying R_{EA}; therefore, I_{C3} is chosen to ensure adequate voltage swing. To enable a swing of at least 1V at the output:

$$\frac{V_{swing,out}}{A_{vLS} \times A_{vEF}} = \frac{1}{0.95 \times .75} = 1.4V \leq V_{swing,CE} \tag{5}$$

the CE stage must provide a swing of at least 1.5V to account for the gain of the final two stages while maintaining headroom before distortion. However, the voltage drop across R_{C3} must remain moderate to preserve the differential stage's available swing, since the two stages are DC-coupled. Additionally, I_{C3} must be sufficiently large to prevent an excessively high R_{C3}, which would require an impractically large R_{EA} to stay within the gain constraints.

Setting $V_{R_{C3}} = 2V$ and selecting $I_{C3} = 1mA$ results in:

$$R_{C3} = \frac{V_{R_{C3}}}{I_{C3}} = \frac{2V}{1mA} = 2k\Omega \tag{6}$$

This sets the voltage swing and current, while the gain can be adjusted later using the emitter resistance.

B. Differential Stage

Neglecting the output resistance of the current source, the input resistance of the differential stage is approximated as:

$$R_{id} = 2(\beta + 1)(r_e) \tag{7}$$

Assuming $\beta = 100$ and setting the input resistance requirement to $R_{id} \geq 20k\Omega$, the minimum total emitter resistance r_e is given by:

$$r_e = \frac{R_{id,min}}{2(\beta + 1)} = \frac{20k\Omega}{2(100 + 1)} = 99\Omega \tag{8}$$

Solving for the emitter current using $I_E = V_T/r_e$, where $V_T \approx 26mV$ at room temperature:

$$I_E = \frac{26mV}{99\Omega} = 262\mu A \tag{9}$$

A lower biasing current limits the maximum output voltage swing, so I_E is chosen to preserve the output swing as much as possible. R_E is chosen to meet the input resistance requirement with a safety margin.The final values selected are:

$$I_{E1,2} = 200\mu A, \quad r_{e1,2} = 130\Omega \tag{10}$$

$R_{C1,2}$ is selected to set the biasing voltage at the output of the differential amplifier, $V_{C1,2} = V_{C3} - 1.5$, Assuming a 1.5V swing is needed for the common emitter stage.

$$R_{C1,2} = \frac{V_{CC} - V_{C1,2}}{I_{C1,2}} = \frac{10V - 6.5V}{200\mu A} = 17.5k\Omega \tag{11}$$

To allow for precise tuning of the voltage gain without radically changing the design, emitter-degenerating resistors are used. Their values are determined to set the differential gain to approximately 30, which provides a good base for the total gain while limiting the necessary stage output swing to $1.5V/30 = 50mV$.

The differential gain is given by:

$$A_{vd} = \frac{R_{C1,2}}{2(r_e + R_{E1,2})} = 30V/V \tag{12}$$

Solving for $R_{E1,2}$:

$$R_{E1,2} = \frac{R_{C1,2}}{2A_v} - r_e = 160\Omega \tag{13}$$

C. Current Source

The Widlar current source is designed to set the tail current as:

$$I_{EE} = 2I_{E1,2} = 400\mu A \tag{14}$$

since I_{REF} is matched to I_{E4}:

$$I_{REF} = 2mA \tag{15}$$

These values determine the resistances of R_E and R_1:

$$R_E = \frac{V_T \ln(I_{REF}/I_o)}{I_o} = 104\Omega \tag{16}$$

$$R_1 = \frac{0V - V_{BE1} - V_-}{I_{REF}} = 4.7k\Omega \tag{17}$$

D. Common-Emitter Stage

Assuming the total gain required is 450 V/V, the gain required from the common-emitter stage is:

$$A_{v2} = \frac{450}{(30 \times 0.7 \times 0.95)} = 22V/V \tag{18}$$

Using the designed values for R_{C3} and I_{C3}, R_{EA} is chosen to achieve the required gain:

$$A_{v2} = \frac{R_{C3}}{\frac{2V_T}{I_{C3}} + R_{EA}} \tag{19}$$

Substituting $R_{C3} = 2k\Omega$, $A_{v2} = 22$, $V_T \approx 26mV$, and $I_{C3} = 1mA$:

$$R_{EA} = \frac{2000\Omega}{22} - \frac{2(26mV)}{1mA} \tag{20}$$

$$R_{EA} = 90.9\Omega - 52\Omega = 38.9\Omega \tag{21}$$

The total emitter resistance is given by applying KVL from the collector of Q_2 through the darlington transistor and to ground, assuming $V_{BE,\text{darl}} = 1.3V$:

$$R_{E,\text{total}} = \frac{V_{C1} - V_{BE,\text{darl}}}{I_{C3}} \tag{22}$$

$$= \frac{6.5V - 1.3V}{1mA} = \frac{5.2V}{1mA} = 5.2k\Omega \tag{23}$$

R_{EB} is the difference between R_{EA} and $R_{E,\text{total}}$:

$$R_{EB} = R_{E,\text{total}} - R_{EA} = 5.2k\Omega - 38.9\Omega = 5.16k\Omega \quad (24)$$

The resistance seen by the capacitor is:

$$R_{CE} = R_{EB} \parallel \left(R_{EA} + \left(\frac{V_T}{I_{C4}} + \frac{R_{C1,2}}{\beta}\right)\right) \quad (25)$$

$$R_{CE} = 5.2k \parallel \left(40 + \left(\frac{0.026}{1mA} + \frac{17.5k}{10000}\right)\right) \quad (26)$$

$$R_{CE} = 5200 \parallel 62.5\Omega = 66.6\Omega \quad (27)$$

Estimating the resistance seen by the capacitor as equal to REB, the 3dB cutoff frequency is:

$$f_{L,3dB} = \frac{1}{2\pi C_E R_{CE}} \quad (28)$$

Substituting $f_{L,3dB} = 100$ Hz and solving for C_E:

$$C_E = \frac{1}{2\pi \times 100 \times 66.66} = 23.6\mu F \quad (29)$$

Therefore a standard $22\mu F$ capacitor is used.

E. Level Shifter and Emitter-Follower

The emitter resistance of the level shifter stage, R_{E4}, is chosen to set the DC offset at the output to 0. The voltage across R_{E4} and the emitter current I_{E4} are known, allowing the resistance to be determined as:

$$R_{E4} = \frac{V_{C3} - V_{BE4} - V_{BE5}}{I_{E4}} \quad (30)$$

Substituting the values $V_{C3} = 8V$, $V_{BE4} = V_{BE5} = 0.7V$, and $I_{E4} = 2mA$:

$$R_{E4} = \frac{8V - 0.7V - 0.7V}{2mA} = \frac{6.6V}{2mA} = 3.3k\Omega \quad (31)$$

Similarly, since $V_{R_{E5}}$ and I_{E5} are known, the resistance R_{E5} is determined using Ohm's law:

$$R_{E5} = \frac{V_{R_{E5}}}{I_{E5}} = \frac{10V}{12.5mA} = 800\Omega \quad (32)$$

IV. Design Check

To validate the design, the expected gain and input resistance values are calculated.

The exact equation for the input resistance is:

$$R_{id} = 2 * (\beta + 1)\,(R_{E1,2} + r_e)) \quad (33)$$

Substituting $r_e = 130\Omega$ and $\beta = 100$:

$$R_{id} = 101 \times (130\Omega + 160\Omega) = 58.6k\Omega \quad (34)$$

Since $R_{id} \geq 20k\Omega$, this satisfies the requirement.

The total gain is the product of the individual stage gains:

$$A_v = A_{v,d} \times A_{v,CE} \times A_{v,LS} \times A_{v,EF} \quad (35)$$

Neglecting the Early effect, the gain of the level shifter stage is given by:

$$R_{B5} = (\beta + 1) \times ((R_{E5} \parallel R_L) + r_{e5}) \quad (36)$$

Substituting:

$$R_{B5} = (101) \times ((800\Omega \parallel 200\Omega) + 2\Omega) = 16.362k\Omega \quad (37)$$

$$A_{v,LS} = \frac{R_{E4}}{r_{e4} + R_{E4}} \times \frac{R_{B5}}{R_{E4} + R_{B5}} \quad (38)$$

Substituting:

$$A_{v,LS} = 0.996 \times 0.832 = 0.828V/V \quad (39)$$

The gain of the Emitter-Follower stage is given by:

$$\frac{R_{E5}}{r_{e5} + R_{E5}} = 0.997V/V \quad (40)$$

Substituting the stage gains into (30):

$$A_v = 30 \times 22 \times 0.828 \times 0.997 = 541V/V \quad (41)$$

This does not satisfy the requirement, but the emitter degenerating resistors allow for the gain to be adjusted experimentally. Therefore no compensation is necessary in the design. Potentiometers will be used in the lab to implement precise gain adjustment. The output resistance is:

$$R_{out} = R_L \parallel R_{E5} \parallel \left(\frac{V_T}{I_{C5}} + \frac{R_{E4}}{\beta}\right) \quad (42)$$

$$= 200 \parallel 800 \parallel \left(\frac{0.026}{0.0125} - \frac{3.3k\Omega}{100}\right) = 29\Omega \quad (43)$$

Since $R_{out} \leq 200\Omega$, this satisfies the requirement.

The peak output voltage is:

$$V_{swing} = (V_{CG} - V_{C4}) \times A_{LS} \times A_{EF} \quad (44)$$

$$= (10 - 8) \times 0.828 \times 0.997 = 1.65V \quad (45)$$

Since $V_{swing} \geq 1V$, this satisfies the requirement. The maximum input peak-to-peak voltage is:

$$V_{ip-p} = \frac{V_{o,p-p}}{A_{\text{total}}} = \frac{2}{541} = 6mV \quad (46)$$

The resistance seen by the capacitor is:

$$R_{CE} = R_{EB} \parallel \left(R_{EA} + \left(\frac{V_T}{I_{C4}} + \frac{R_{C1,2}}{\beta}\right)\right) \quad (47)$$

$$R_{CE} = 5.2k \parallel \left(40 + \left(\frac{0.026}{1mA} + \frac{17.5k}{10000}\right)\right) \quad (48)$$

$$R_{CE} = 5200 \parallel 62.5\Omega = 66.6\Omega \quad (49)$$

The 3dB cutoff frequency is:

$$f_{L,3dB} = \frac{1}{2\pi C_E R_{CE}} = \frac{1}{2\pi \times 22\mu F \times 66.6} = 108.6Hz \quad (50)$$

this does not meet the specification, so a larger capacitor may be needed.

V. Simulation Results

To validate the design, various simulations were performed, including DC operating point analysis, AC gain analysis, input impedance measurement, and transient response analysis. The results are presented below.

A. DC Operating Conditions

The DC biasing conditions of the circuit were verified to ensure proper transistor operation. The measured DC voltages and currents confirm that the circuit operates within the expected parameters, and show that the DC offset voltage at the output is less than $10mV$

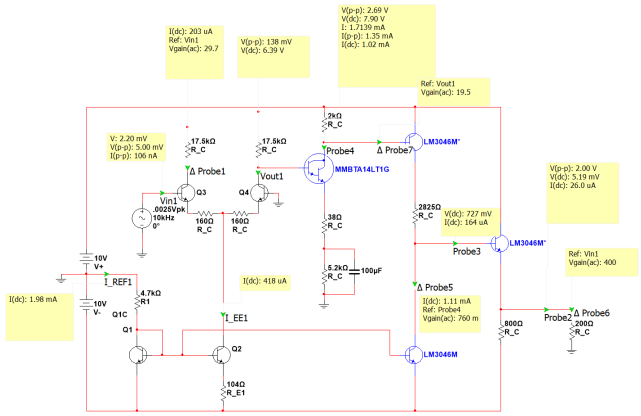

Fig. 2. Simulated DC operating conditions of the amplifier.

B. AC Gain and Frequency Response

The open-loop gain and bandwidth of the amplifier were analyzed using an AC sweep. The frequency response plot in Fig. 3 shows the midband gain of 467.87 V/V which satisfies specifications. The low-frequency cutoff occurs at about $45Hz$, which satisfies the specification.

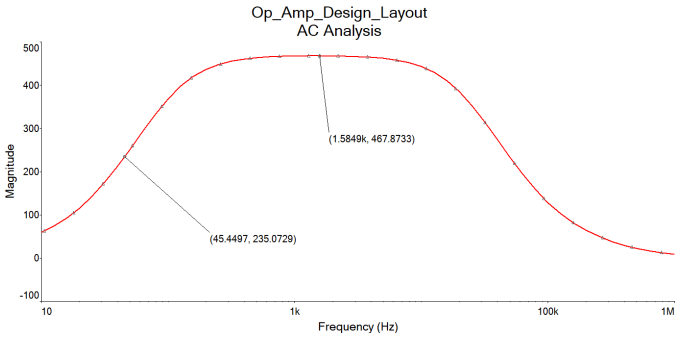

Fig. 3. Simulated AC gain and frequency response.

C. Input Impedance Measurement

The input impedance of the amplifier was measured at 1 kHz using an AC analysis. The results, shown in Fig. 4, indicate an input resistance of 47.15 kΩ, which satisfies specification.

Op_Amp_Design_Layout
Single Frequency AC Analysis @ 1000 Hz

	Variable	Real	Imaginary
1	V(Vin1)/I(Vin1)	47.15007 k	-224.94779

Fig. 4. Simulated input impedance at 1 kHz.

D. Transient Response Analysis

A transient analysis was performed to examine the time-domain behavior of the amplifier. The output waveform in Fig. 5 shows a peak-to-peak voltage swing of approximately 2.1V without distortion, which meets specification.

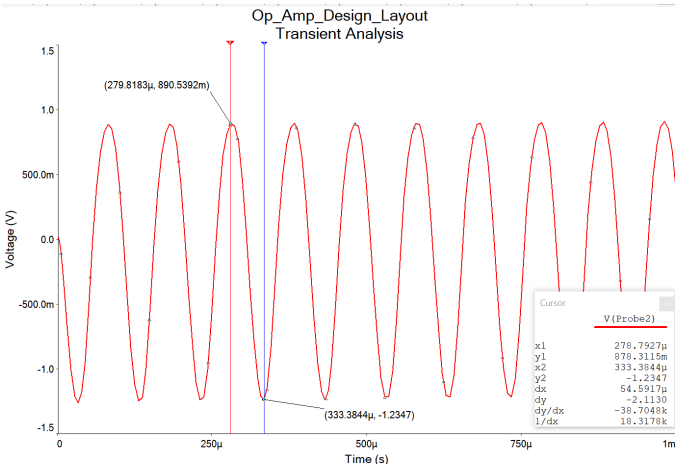

Fig. 5. Simulated transient response of the amplifier.

These simulation results validate the design, ensuring it meets the required specifications for gain, bandwidth, input impedance, and output voltage swing.

A comparison between the designed and simulated values is provided in Table I. This table summarizes key parameters, including gain, impedance, cutoff frequency, and bias currents, to verify that the circuit meets the design specifications. The simulated values closely match the designed values, confirming that the amplifier performs as expected.

TABLE I
Comparison of Designed and Simulated Values

Parameter	Designed Value	Simulated Value
$A_{v,d}$	30	29.7
$A_{v,CE}$	22	19.5
$A_{v,LS}$	0.7	0.828
$A_{v,EF}$	0.99	0.99
$A_{v,total}$	450	467.87
R_{in}	$\geq 20k\Omega$	47.15kΩ
R_o	$\leq 200\Omega$	29Ω
$f_{L,3dB}$	≤ 100 Hz	45.6 Hz
$V_{o,peak}$	$\geq 1V$	1.39V
V_{ip-p}	≥ 6 mV	6.5 mV
I_{EE}	400 μA	418 μA
$I_{C1,2}$	200 μA	203 μA
I_{C3}	1 mA	1.02 mA
I_{E4}	2 mA	1.99 mA
I_{E5}	12.5 mA	12.7 mA
V_{C1}	6.5 V	6.39 V
V_{C3}	8 V	7.90 V
V_{E4}	700 mV	727 mV
V_{E5}	$\leq 10mV$	5.19 mV

VI. Expected Results

The implemented circuit is expected to demonstrate:

- An open-loop gain between 400 and 500.
- An input resistance greater than 20kΩ.
- An output resistance below 200Ω.
- A low-frequency cutoff within specifications.
- A peak-to-peak output swing of at least 2V.

VII. Conclusion

This prelab outlines the theoretical design and expected performance of a two-stage operational amplifier. Simulations will validate the design against the required specifications, ensuring its practical feasibility.

References

[1] Loyola Marymount University, Department of Electrical Engineering and Computer Science, "EECE3200 Lab 6: Operational Amplifier Design," 2025.