ECE 574 – VLSI System Design

Homework n°3: State Machines – Experimenting with glitchy vs non-glitchy state machines

Amine Gaizi
gaizia@oregonstate.edu
Student ID: 934-044-900

1. Glitchy simulation

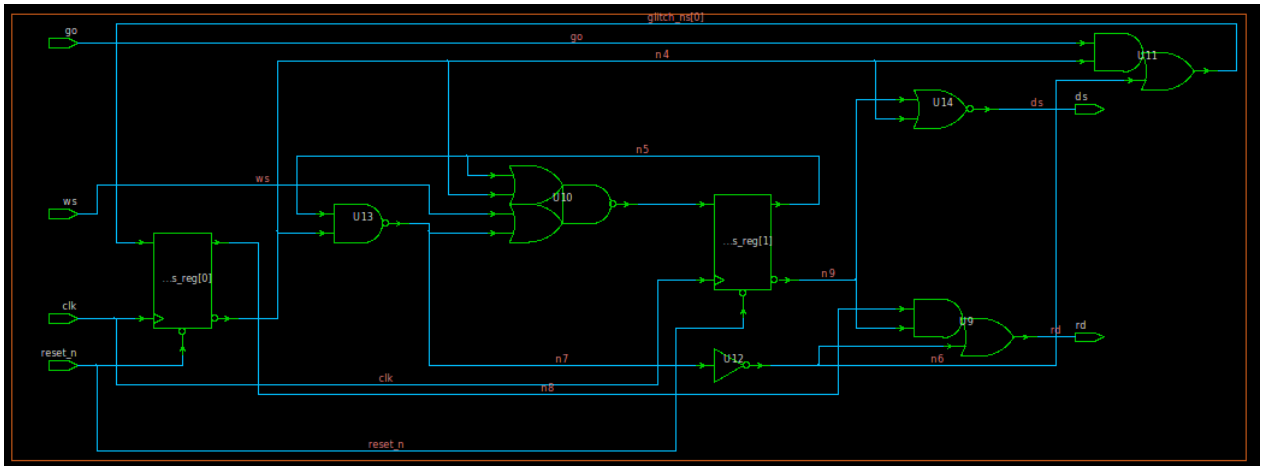

Figure 1: Glitchy FSM gate level schematic

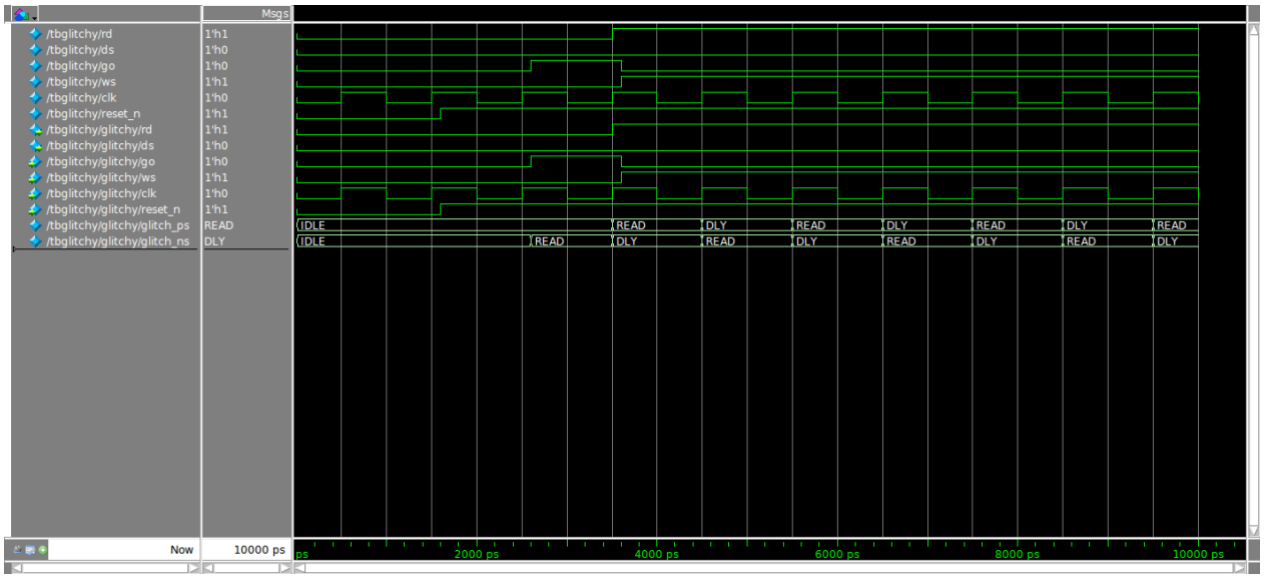

Figure 2: Glitchy FSM RTL simulation waveforms

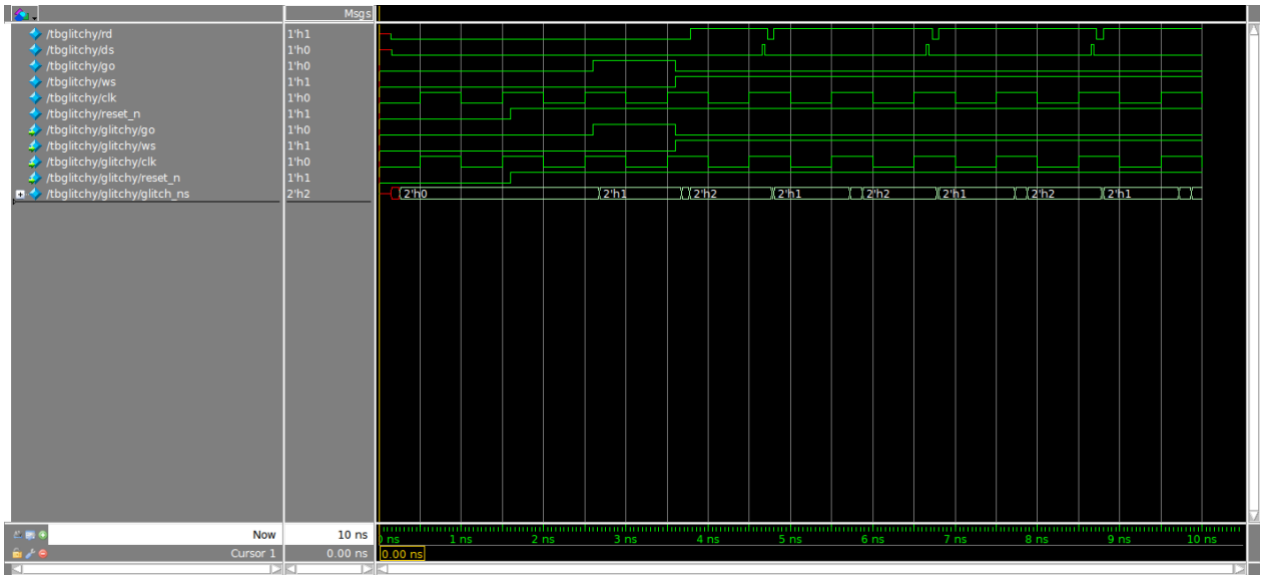

Figure 3: Glitchy FSM Gate level waveforms

Behavior of the signal ds:

In the gate level simulation, we can clearly see that in the transition between the 'READ' state (2'h1) and 'DLY' state (2'h2), there is a glitch on signals 'rd' and 'ds'.
If we pay attention to the path the signals go through, we can see that the 'go' signal goes through logic gates (combinational logic) before being passed to the first flip flop. The signal at the output of the flip flop then goes through other logic gates before going to the second flip flop. Also, we can notice that the output signals are generated by an output combinational logic block that depend on the value of the second flip flop.

We can assume that at the rising edge, the signal is loaded into the first flip flop. Because of the combinational logic in between the two flip flops, the internal signal do not have time to be loaded into the second flip flop before the end of the clock edge. Therefore, the signal value is not updated immediately and creates the glitch we see on the signal ds when performing the gate level simulations.

2. Glitch less Finite State Machine

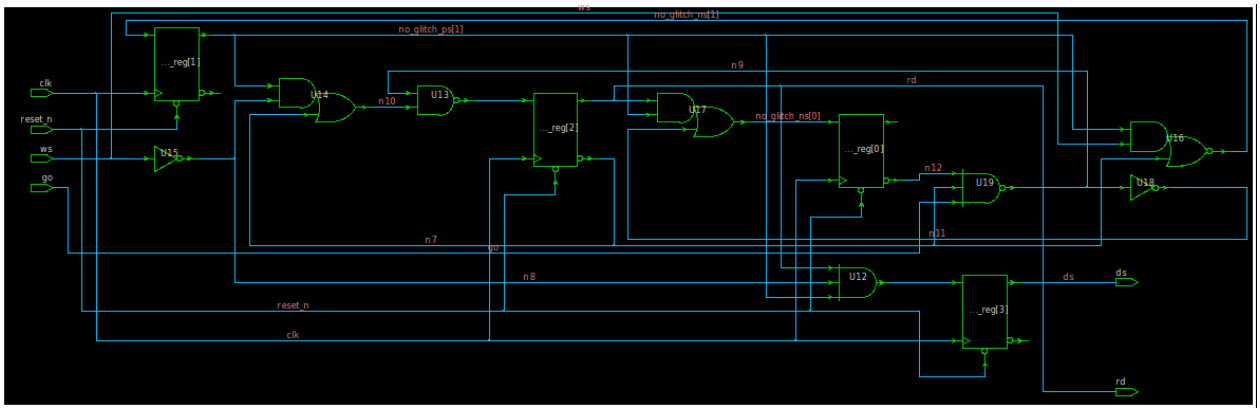

Figure 4: Glitch Less FSM gate level schematic

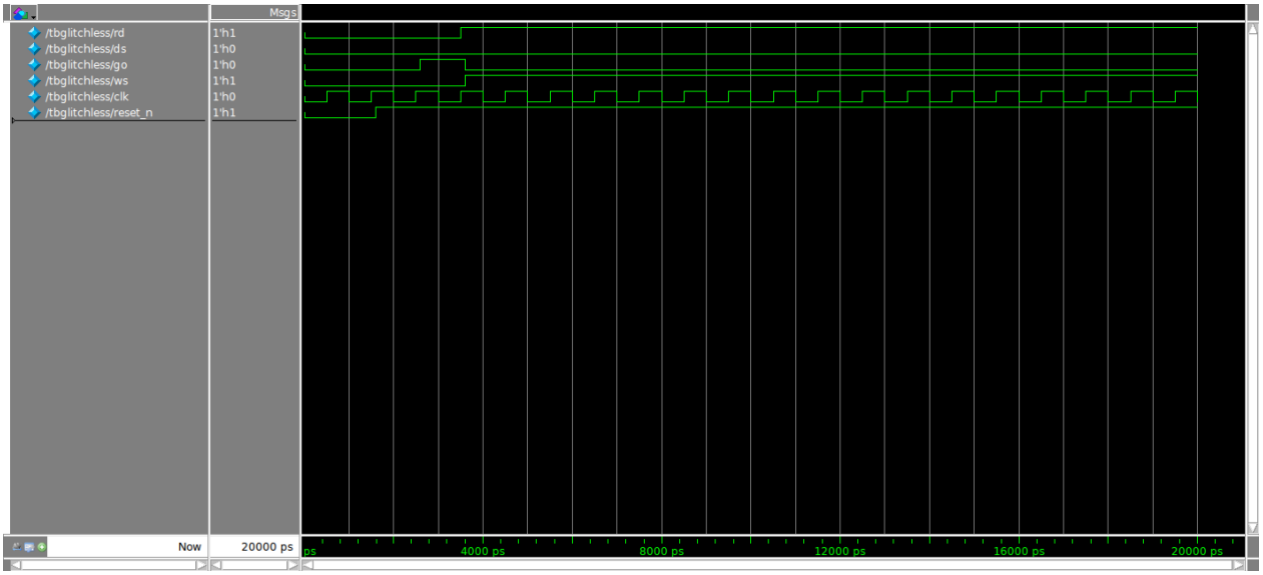

Figure 5: Glitch less FSM RTL simulation waveforms

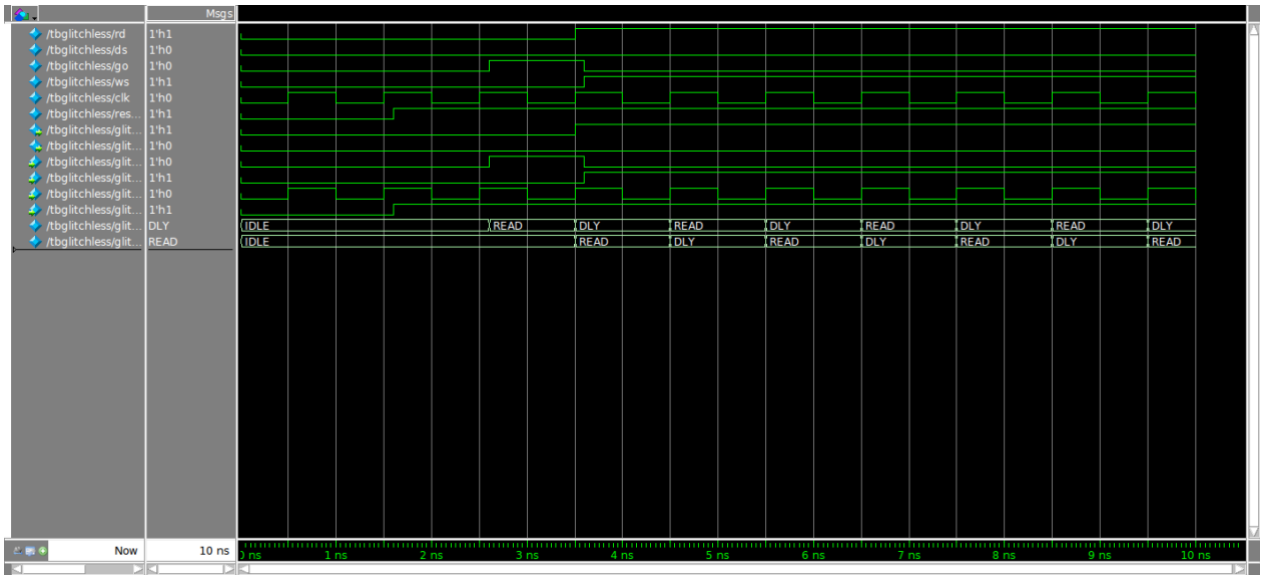

Figure 6: Glitch less FSM Gate level waveforms

Behavior of the signal ds:

In this case, we can see on the gate level schematic that the signal ‘ds’ is stored in a flip flop directly at the output. This solves the problem since the output signal does not depend on an output combinational block, but only on the clock edge that makes the flip flop output the new value of the signal.