A Survey on SGX Enclave Privileged Side-Channel Attacks

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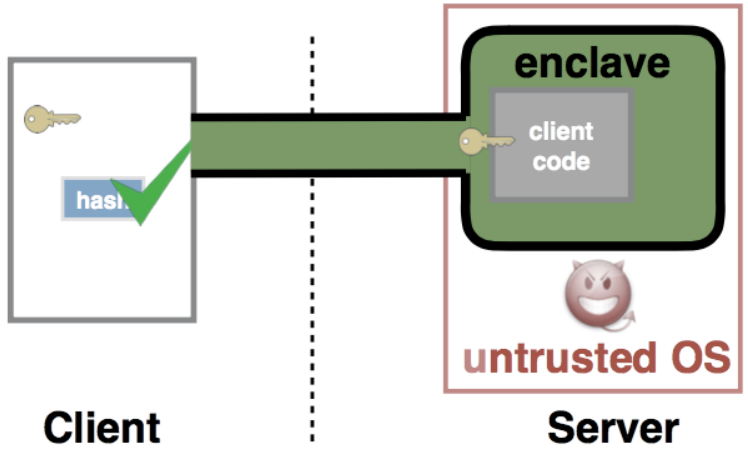
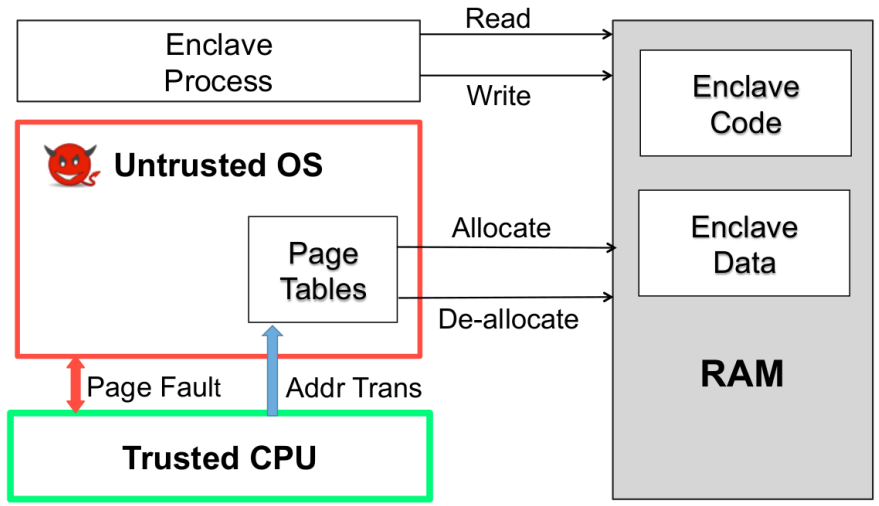
Introduction

- Computing environment
  - Shared resources executing user programs
- Security inside the cloud
  - A hardware solution needed
- Intel SGX
  - Secure user code and data in the public cloud
  - Protecting data inside the enclave
- Privileged Operating System
  - Kernel space, hardware control



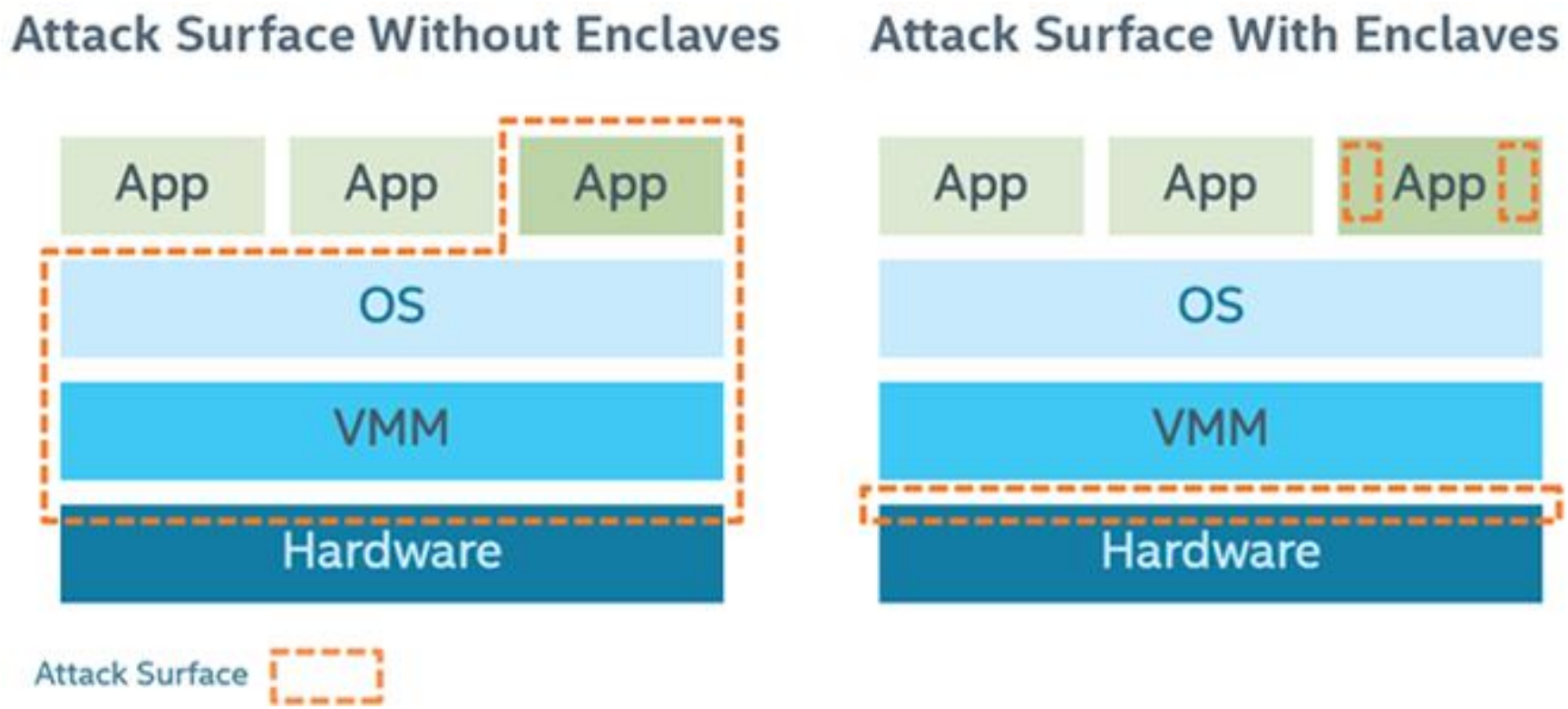
Introduction

- Side-Channels
  - Attacks by analyzing system behavior
  - Cache attacks: Monitoring cache accesses
  - Timing attacks: Measuring time between computations
  - Page-fault attack: Monitoring page-faults and analyzing the pattern



Introduction

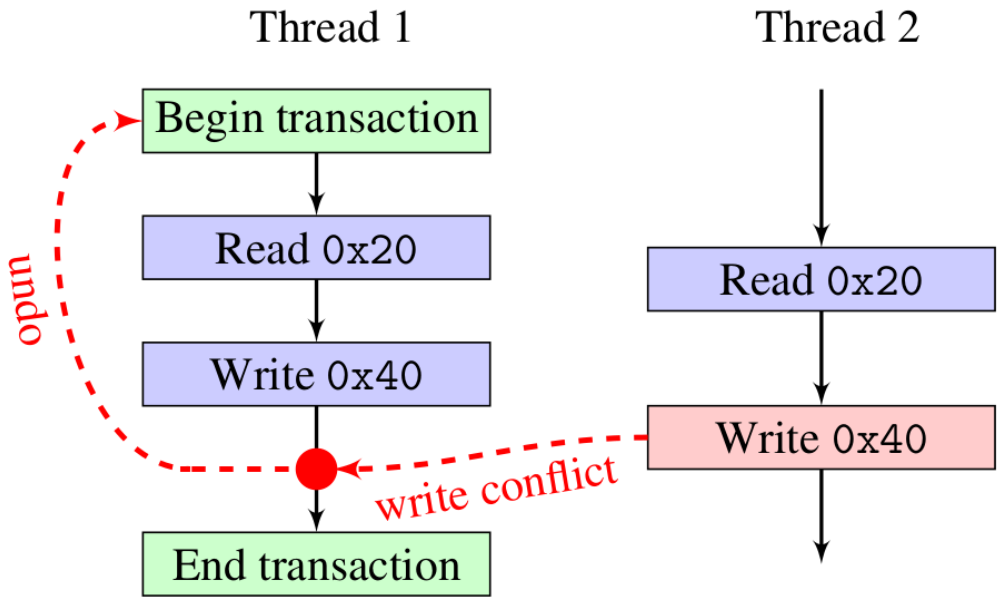
Intel SGX



Introduction

Intel TSX

- Introduced with Haswell
- Critical sections management
- Monitoring serialization
- Restricted Transactional Memory
  - New Instruction set interface



Attacks

Attack Model

- Enclave protected by SGX
  - No stranger has the key
- Operating System can manage task queues, interrupts, and exceptions
- Viewing data transfer between memories and caches
- Program pinned to one core, no excessive interrupts, isolated

Attacks

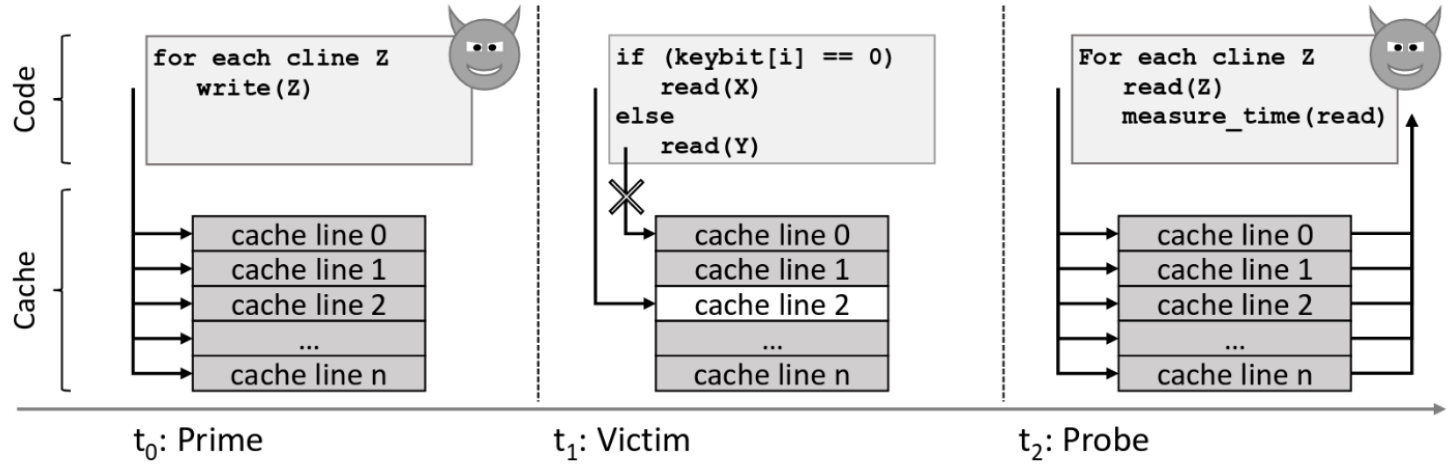
Points of attack

- TLB: shared between enclave and non-enclave programs ⇨ with hyperthreading enabled it creates side-channels
- Page faults: visible to OS
- TLB flushes: on context switch
- Page table entry flags
- Enclave memory address beginning and offset are known
- Enclave exits (AEX)

Attacks

Prime+Probe

- Prime: attacker executes conflicting cache lines ⇨ cache miss
- Probe: executing all the cache lines and measuring execution time



Attacks

Flush+Reload

- Flush target memory line
- Wait for the victim to access

```
if (secret) {
    ;
} else {
    ;
}
```

- Request to access target memory line ⇨ access time
- Based on the access time, access by the victim will be revealed

Attacks

Stealthy page table based attacks

- Introduced by Van Bulck et al.
- Basic page-fault attack:
  - OS controls page tables
  - Sets trap by making pages inaccessible
  - Observe page-fault patterns
  - Or simply monitor certain pages and cause page-faults
- Page table entry flags
  - Accessed and dirty flags

Attacks

Sneaky page monitoring attacks

- Introduced by Wang et al.
- Accessed flags monitoring
  - Flags in TLB are not updated
  - Flush the TLB (by IPI)
- Timing enhancement
  - Only one interrupt ⇨ better performance
  - Measure the time between two repeatedly accessed entries
- TLB flushing through hyperthreading
  - TLB is shared between hyperthreads
  - Invalidate TLB entries without IPI

Attacks

DRAMA

- Disable caching
  - Prevent cache based side channel attacks
- Attacker allocates two memory lines inside one bank
- Regularly access one of the memory lines
- Victim accesses the other memory line ⇨ conflict ⇨ attacker's next fetch will take more time
- Cache-DRAM attack: Prime+Probe and DRAMA

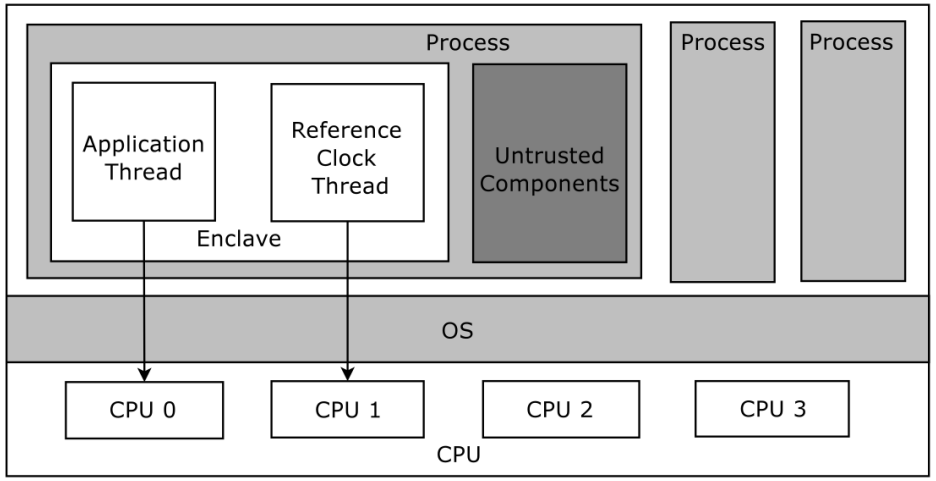
Attacks

Flush+Flush

- *clflush* instruction: flush a cache line, if empty ⇨ abort
- Abort takes less time than flush
- Use the delay ⇨ which memory address is accessed

Defenses

- Déjà vu
  - Embed a clock inside enclave
  - Protect the clock inside TSX transaction
  - Record regular execution time
  - Time runs out ⇨ AEX instability ⇨ attack detected
- Shinde et al.
  - Deterministic page access profile
  - Fake accesses



Defenses

- T-SGX
  - CPU does not deliver page-fault to the OS
  - Abort transaction and run the fallback code
  - Lots of aborts
  - Break into execution blocks
- Cloak
  - Pin data in cache: Not supported by hardware
  - Preload code/data in transaction and run the algorithm
- SGX-Shield
  - Address space layout randomization (ASLR)
    - Secure in enclave loading
    - Limited memory ⇨ small randomization entropy ⇨ brute force attacks

Analysis

- Cloak
  - Makes cache-pinning possible to some extent
  - Execution time can leak
  - Aborts do not cancel concurrent memory accesses
  - Execution behavior and branch prediction uncertainties
- T-SGX
  - Attacks based on monitoring flags are possible

Analysis

- Déjà vu
  - Sneaky page monitoring attacks still effective
  - Only works on AEX based attacks
- Bottom line
  - Transaction based defenses usually come with high overload and low utilization

Analysis

- SGX-Shield
  - No live randomization ⇨ observe and monitor random patterns
- Shinde et al.
  - Cache and TLB based attacks possible

Analysis

- Other methods
  - Attack detection methods ⇨ Unreliable
  - Shuffling memory ⇨ expensive
  - ORAM (make addresses input-independent) ⇨ expensive
- The perfect solution?
  - Remove all branches and conditional code
  - Pin data/code to cache and TLB

Conclusion

- We studied multiple attacks and defenses
- Still no robust defense
- Attack are emerging
- Open to research

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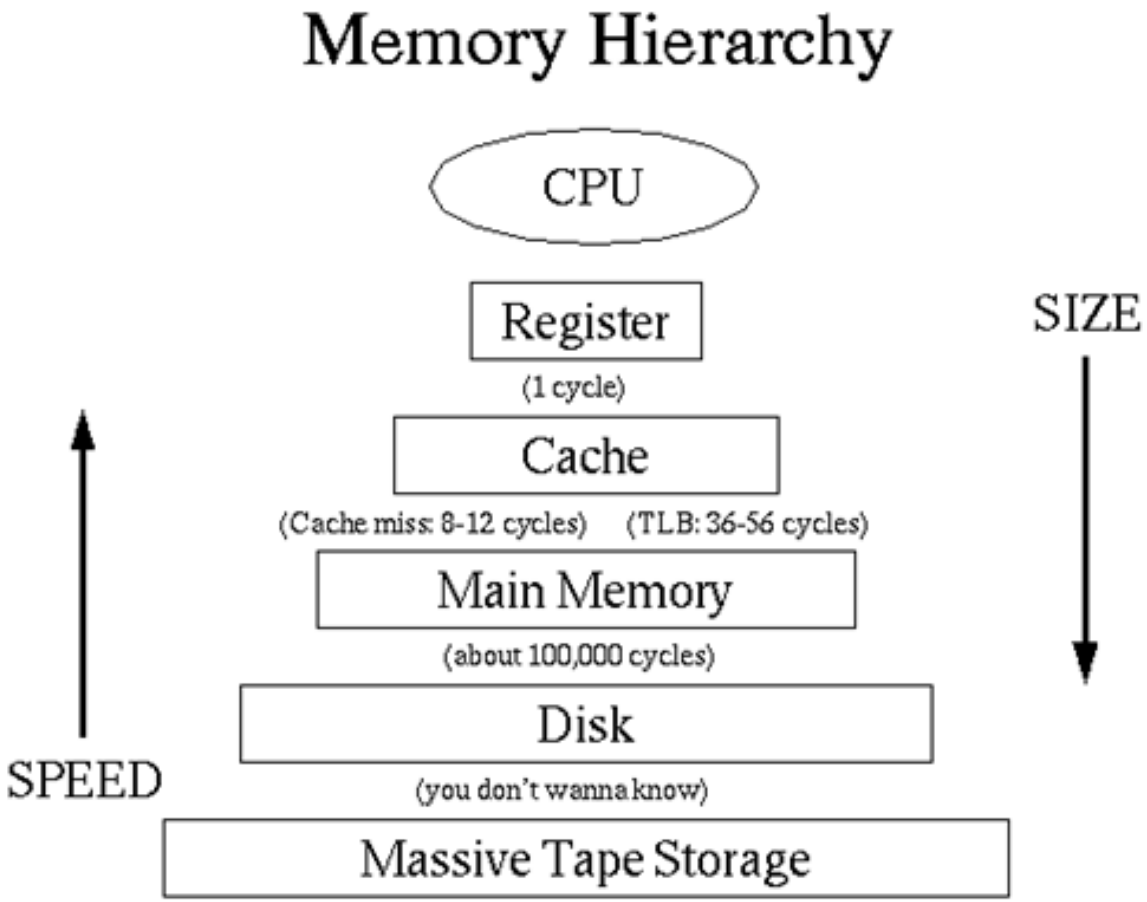
Introduction



Defenses

- SGX-Shield
  - Address space layout randomization
- ORAM+SGX
- Data shuffling