Microprocessors' Internal Architectures

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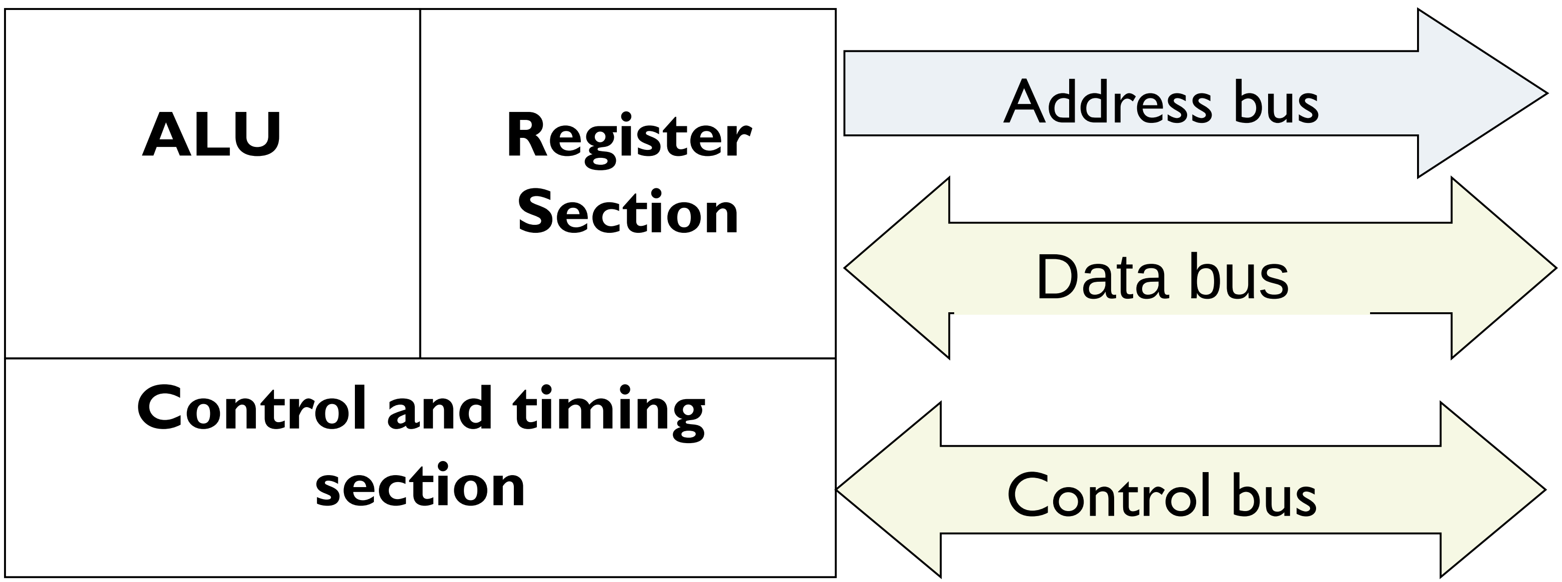
Course Title: Microprocessor and Assembly Language

Lecture References:

- **Book:**
  - *Microprocessor, architecture, programming & application with the 8085, Chapter # 2,* **Author:** Gaonkar
  - *Microprocessors and Interfacing: Programming and Hardware, Chapter # 2,* **Author:** Douglas V. Hall

- **Lecture Materials:**
  - *IBM PC Organization,* CAP/IT221

Internal Structure of a Microprocessor

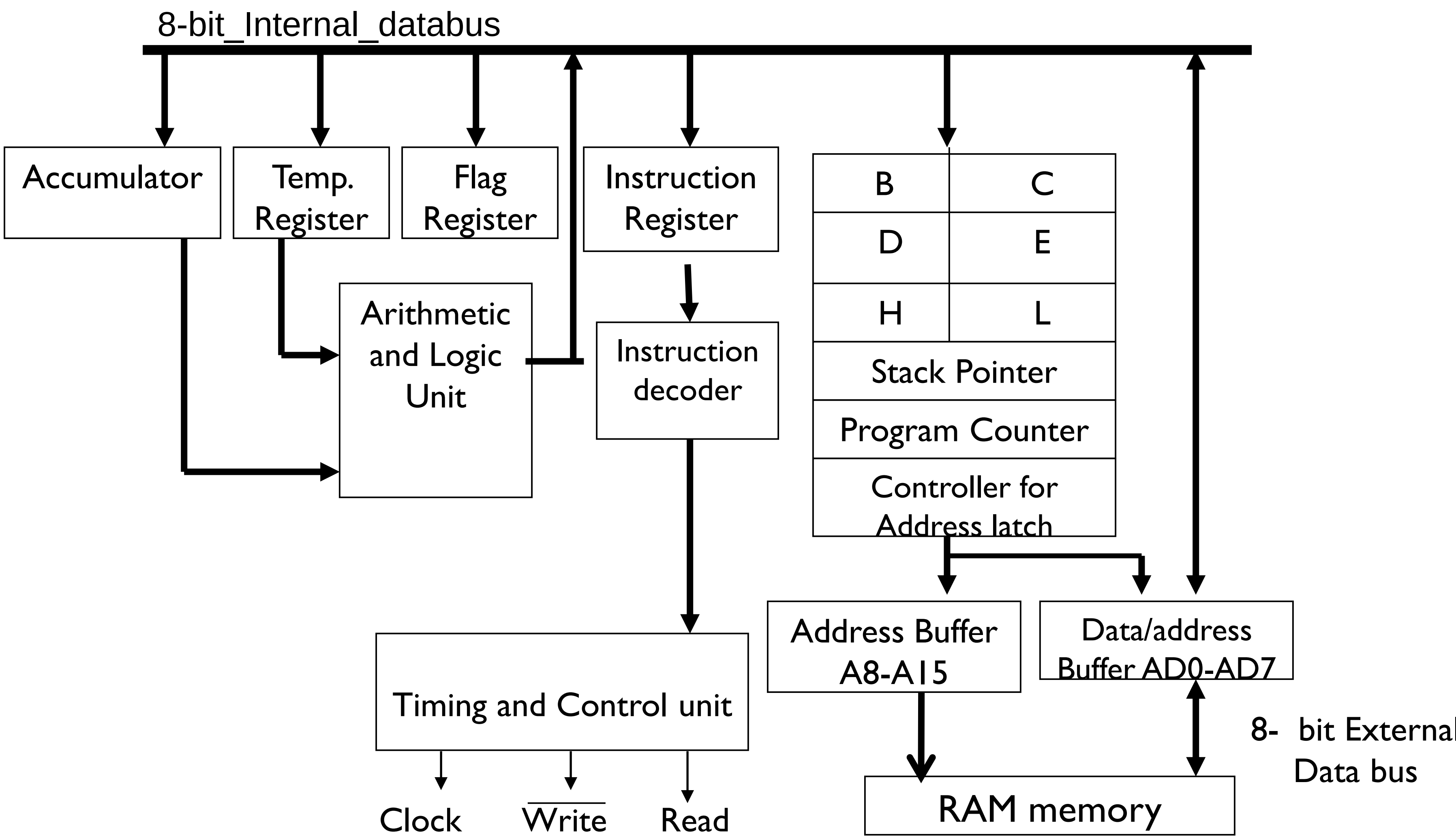


Block Diagram of a Microprocessor

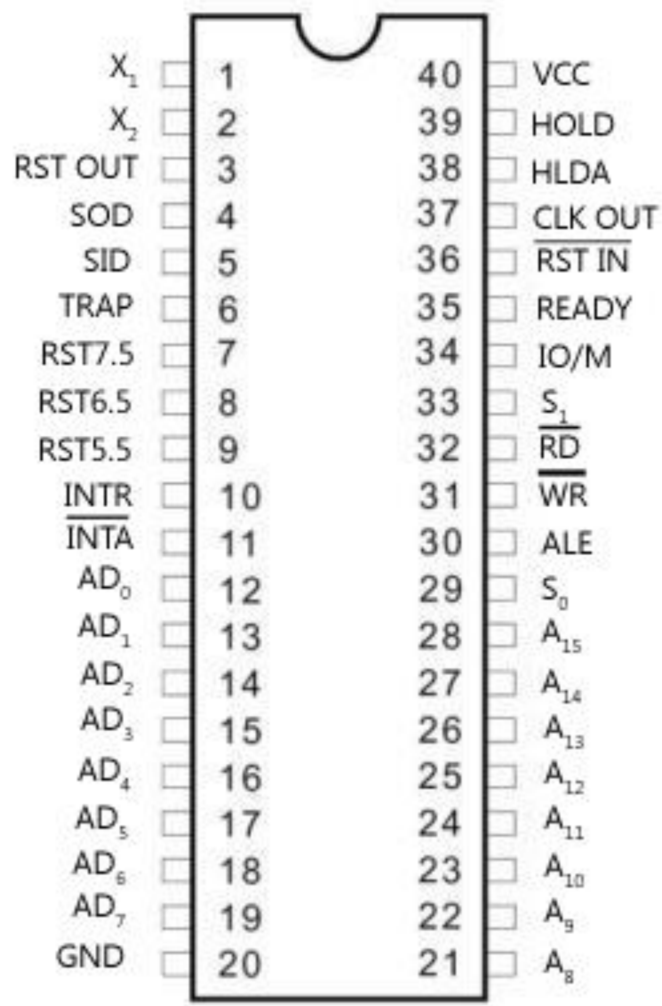
8085 Microprocessor

- **Intel 8085**
  - The 8085 microprocessor was introduced by Intel in the year 1976.
  - 8-bit microprocessor with 16-bit address bus and 8-bit data bus.
  - This microprocessor is an update of 8080 microprocessor.
  - It is an 8-bit microprocessor with a 40 pin Dual in Line Package (DIP)
  - Total 74 operation codes in assembly language and those can generate 246 instructions.

8-Bit 8085 Intel Processor Architecture



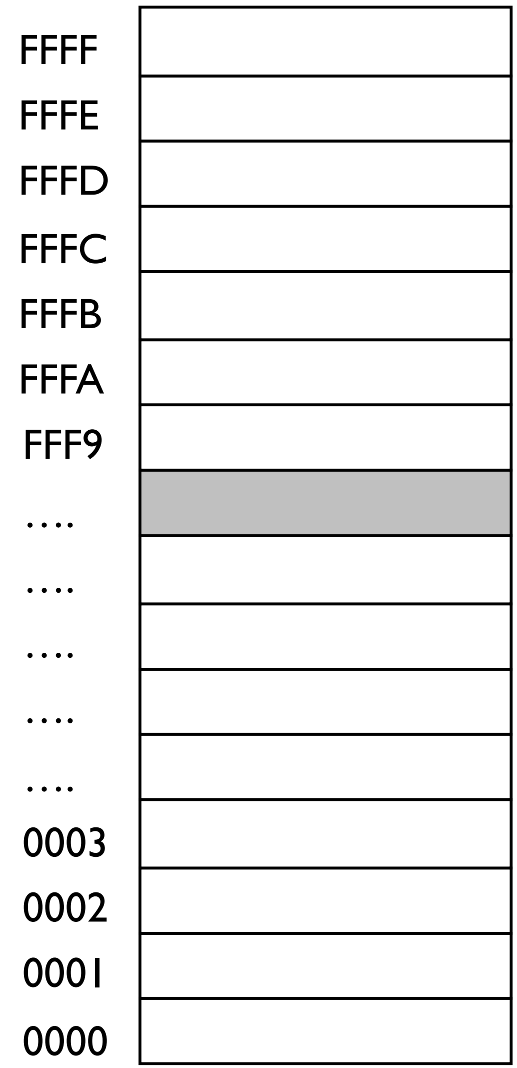
8-Bit 8085 Intel Processor (Pin Diagram)



8085 Registers and Memory

- **Registers:**
  - Total 11 registers and 1 temporary register
  - Information is stored in registers
  - Registers are classified according to the functions they perform

- 64 Kbytes of memory and 65536 memory locations.



8085 Register Categories

- **Accumulator** – 8 bit register which holds the latest result from ALU
- **B, C, D, E, H** and **L** are general purpose registers
- **HL** pair can be used for indirect addressing as well
- **Program counter** – 16 bit register which holds the address of the next instruction to be executed
- **Instruction Register** – It holds the instruction that is currently being processed.
- **Stack Pointer** is used during subroutine calling and execution.
- **Address Latch** – It increments/ decrements the address before sent to the address buffer

8085 Register Categories

- **<u>Flag Register</u>**

- **Sign Flag**: If the result of the latest arithmetic operation is having MSB (most- significant byte) ‘1’ (meaning it is a negative number), then the sign flag is set to ‘1’. Otherwise, it is reset to ‘0’ which means it is a positive number.

- **Zero Flag**: If the result of the latest operation is zero, then zero flag will be set to ‘1’; otherwise it be reset to ‘0’.

- **Auxiliary Carry Flag**: This flag is not accessible to programmer. This flag will be used by the system during BCD (binary-coded decimal) operations.

- **Parity Flag**: If the result of the latest operation is having even number of ‘1’s, then this flag will be set to ‘1’ Otherwise this will be reset to ‘0’. This is used for error checking.

- **Carry Flag**: If the result of the latest operations exceeds 8-bits then this flag will be set to ‘1’. Otherwise it be reset to ‘0’.

Simple Assembly Program in 8085

MVI A, 32H
MVI B , 48H
ADD B
OUT 01H
HLT

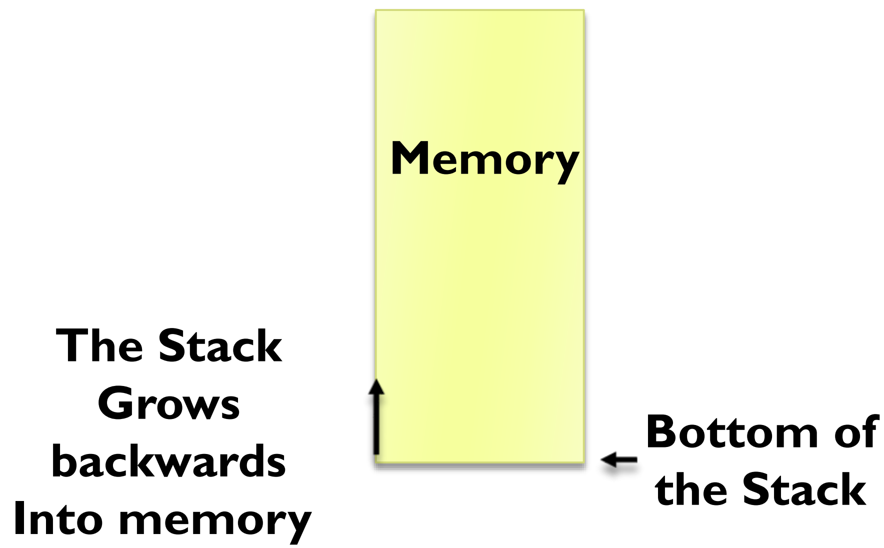
Memory Address	Contents (Binary)	Contents (Hex)	Operation
2000h	0011 1110	3E	Load Reg. Acc.
2001h	0011 0010	32	Value is 32h
2002h	0000 0110	06	Load Reg. B
2003h	0100 1000	48	Value is 48h
2004h	1000 0000	80	Add B with A & Store in A
2005h	1101 0011	D3	Display
2006h	0000 0001	01	Port Id 01h
2007h	0111 1100	76	End

Task:

- Derive the flag values

Stack Pointer and Stack Memory

- The stack is an area of memory identified by the programmer for temporary storage of information.
- The stack is a LIFO structure.
- The stack normally grows backwards into memory.
  - Programmer can defines the bottom of the stack (**SP**) and the stack grows up into reducing address range.



Stack Memory

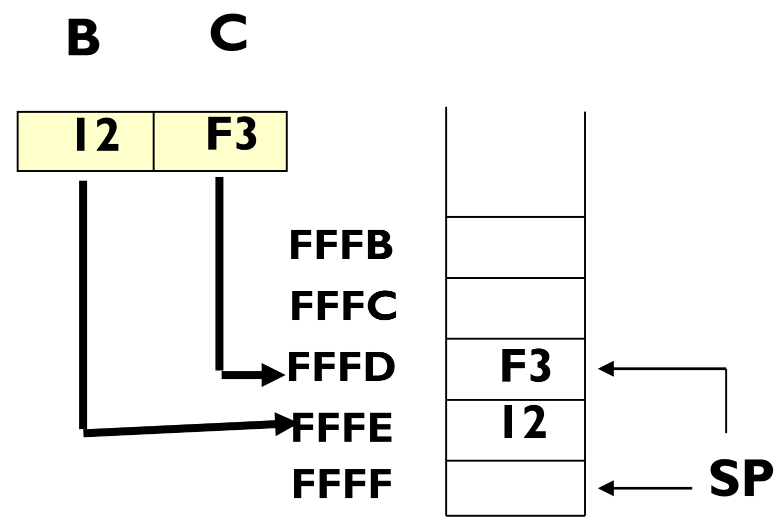
- Grows backwards into memory
- Better to place the bottom of the stack at the end of memory
- To keep it as far away from user programs as possible.
- Stack is defined by setting the SP (Stack Pointer) register.

LXI SP, FFFFh ; Load 16-bit number in a register

- This sets SP to location FFFFh (end of memory for 8085).

Saving Information in Stack

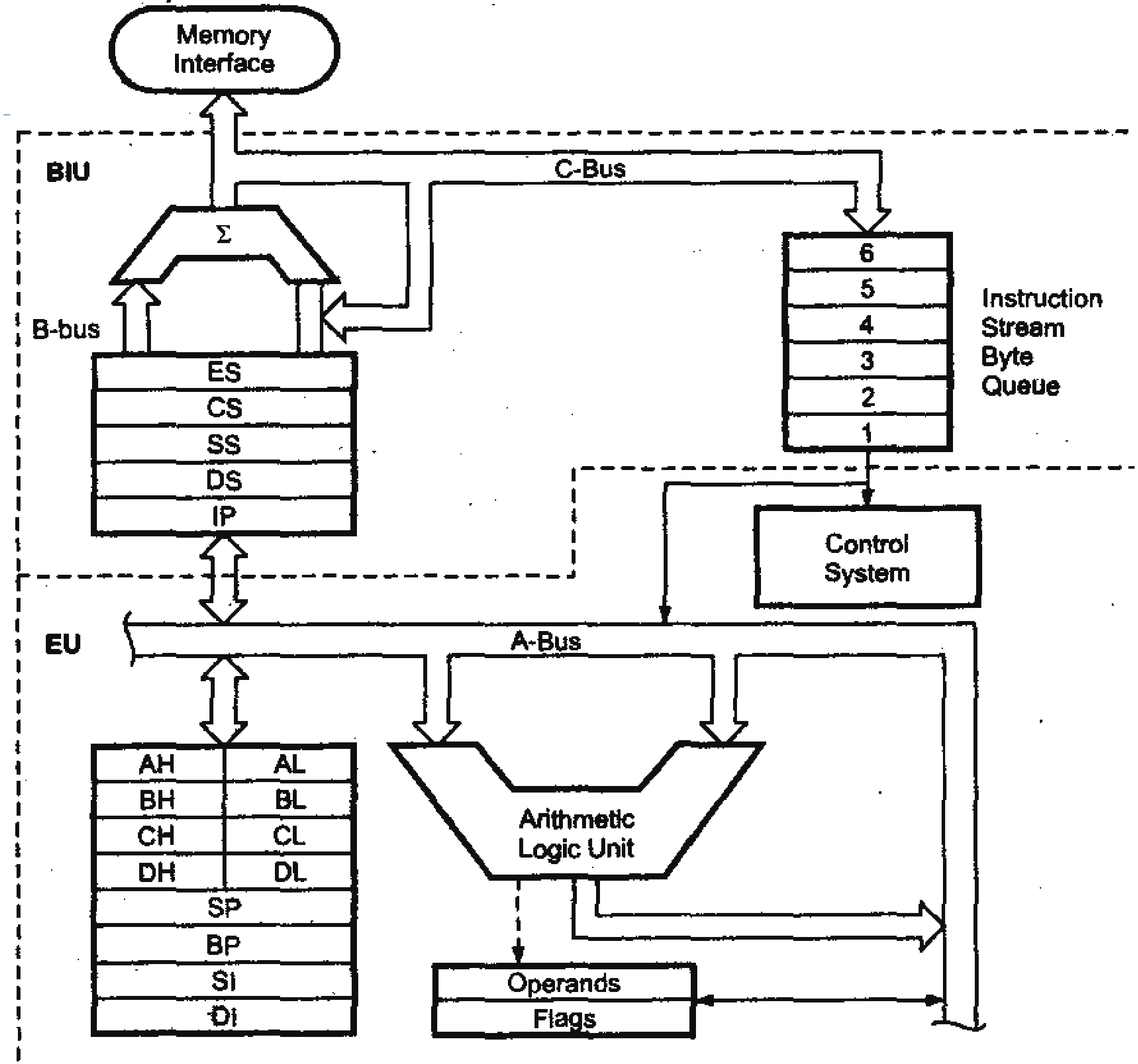
- Save information by PUSHing onto STACK
- Retrieved from STACK by POPing it off.
- PUSH and POP work with register pairs only.
- Example "PUSH B"
  - Decrement SP, Copy B to 0(SP)
  - Decrement SP, Copy C tp 0(SP)
- Example "POP B"
  - Copy SP to C, Increment SP
  - Copy SP to B, Increment SP



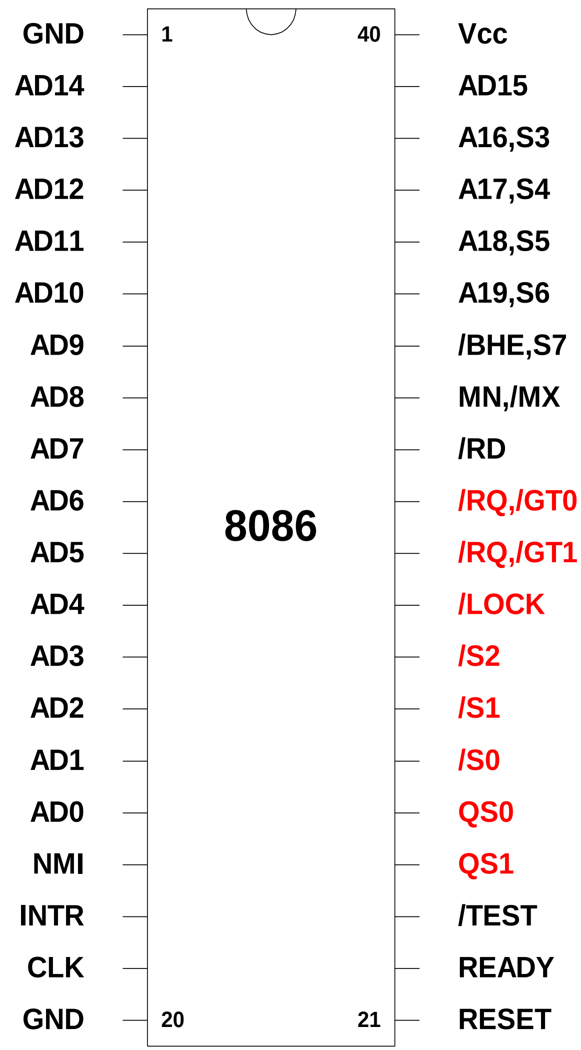
8086/8088 Microprocessor

- **Intel 8086**
  - The microprocessor 8086 can be considered to be the basic processor for the Intel X86 family from 1978.
  - It has a 20-bit address bus along with 16-bit data bus.
  - With the knowledge of 8086 16-bit processor, one can study the further versions of this processor 80286, 80406 and Pentium.
- **Intel 8088**
  - The Intel 8088 have 20-bit address bus with 8-bit data bus (allowing the use of cheaper and fewer supporting logic chips).
  - 8086/8088 have the same instruction set, it forms the basic set of instructions for other Intel families.

16-Bit 8088/8086 Intel Processor Architecture



16-Bit 8086 Intel Processor (Pin Diagram)



Organization of the 8088/8086

- 2 main components:
  1. **Execution Unit (EU)**
  2. **Bus Interface Unit (BIU)**

- **EU:** ALU + Registers (AX, BX, CX, DX, SI, DI, BP, and SP) + FLAGS register.
  - **ALU:** performs arithmetic & logic operations.
  - **Registers:** store data
  - **FLAGS Register:** Individual bits reflect the result of a computation.

Organization of the 8088/8086

- **BIU:** facilitates communication between the EU & the memory or I/O circuits.
  - Responsible for transmitting addresses, data, and control signals on the buses.
  - **Registers** (CS, DS, ES, SS, and IP) hold addresses of memory locations.
  - **IP** (instruction pointer) contain the address of the next instruction to be executed by the EU.

8086 Registers and Memory

Number of Registers: 14, each of that16-bit registers

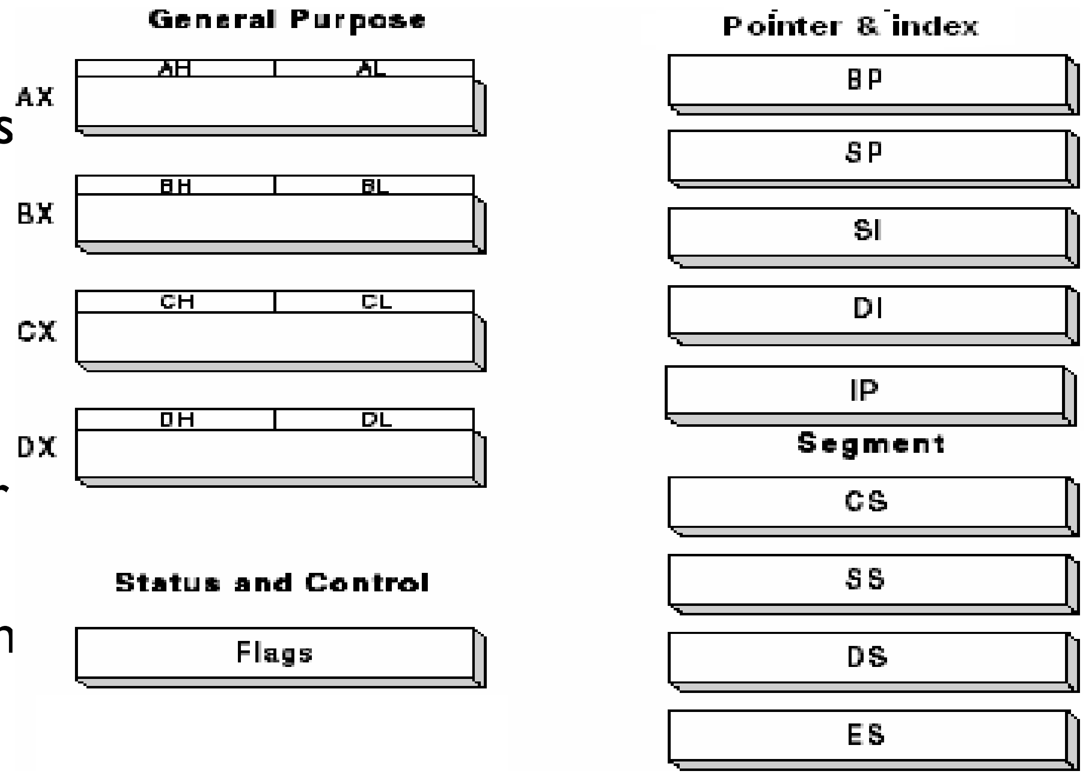
Memory Size: 1M Bytes

Registers of the 8086/80286 by Category

Category	Bits	Register Names
General	16	AX,BX,CX,DX
	8	AH,AL,BH,BL,CH,CL,DH,DL
Pointer	16	SP (Stack Pointer), Base Pointer (BP)
Index	16	SI (Source Index), DI (Destination Index)
Segment	16	CS(Code Segment) DS (Data Segment) SS (Stack Segment) ES (Extra Segment)
Instruction	16	IP (Instruction Pointer)
Flag	16	FR (Flag Register)

8086 Register Categories

- **Data registers (4)**: General data registers hold data for an operation (AX, BX, CX, DX).
- **Address registers (9)**: (Segment, Pointer and Index registers) hold the address of an instruction or data.
- **Status register (1)**: FLAG register keeps the current states of the processor.



General Data Registers

- These are 16-bit registers and can also be used as two 8 bit registers: ***low and high bytes*** can be accessed separately
- **AX (Accumulator)**
  - Most efficient register for arithmetic, logic operations and data transfer: the use of AX generates the shortest machine code.
  - In multiplication and division operations, one of the numbers involved must be in AL or AX
- **BX (Base)**
  - The base address register (offset)
- **CX (Counter)**
  - Counter for looping operations: loop counter, in REP instruction, and in the shift and rotate bits
- **DX (Data)**
  - Used in multiply and divide, also used in I/O operations

Memory Segment and Offset Concept

- The 8086 processor assign a 20-bit physical address to its memory locations.

  $2^{20} \rightarrow$ **1 Mbyte**

  20 bits $\rightarrow$ 5 hex digits

  First addresses: 00000, 00001,…,0000A,…FFFFF.

  But Registers are 16-bits and can address only 2^{16} = **64 KBytes.**

- **Partition the memory into segments**
  - One way four (4) 64 Kbytes segments might be positioned within the 1 Mbyte address space of an 8086 processor.

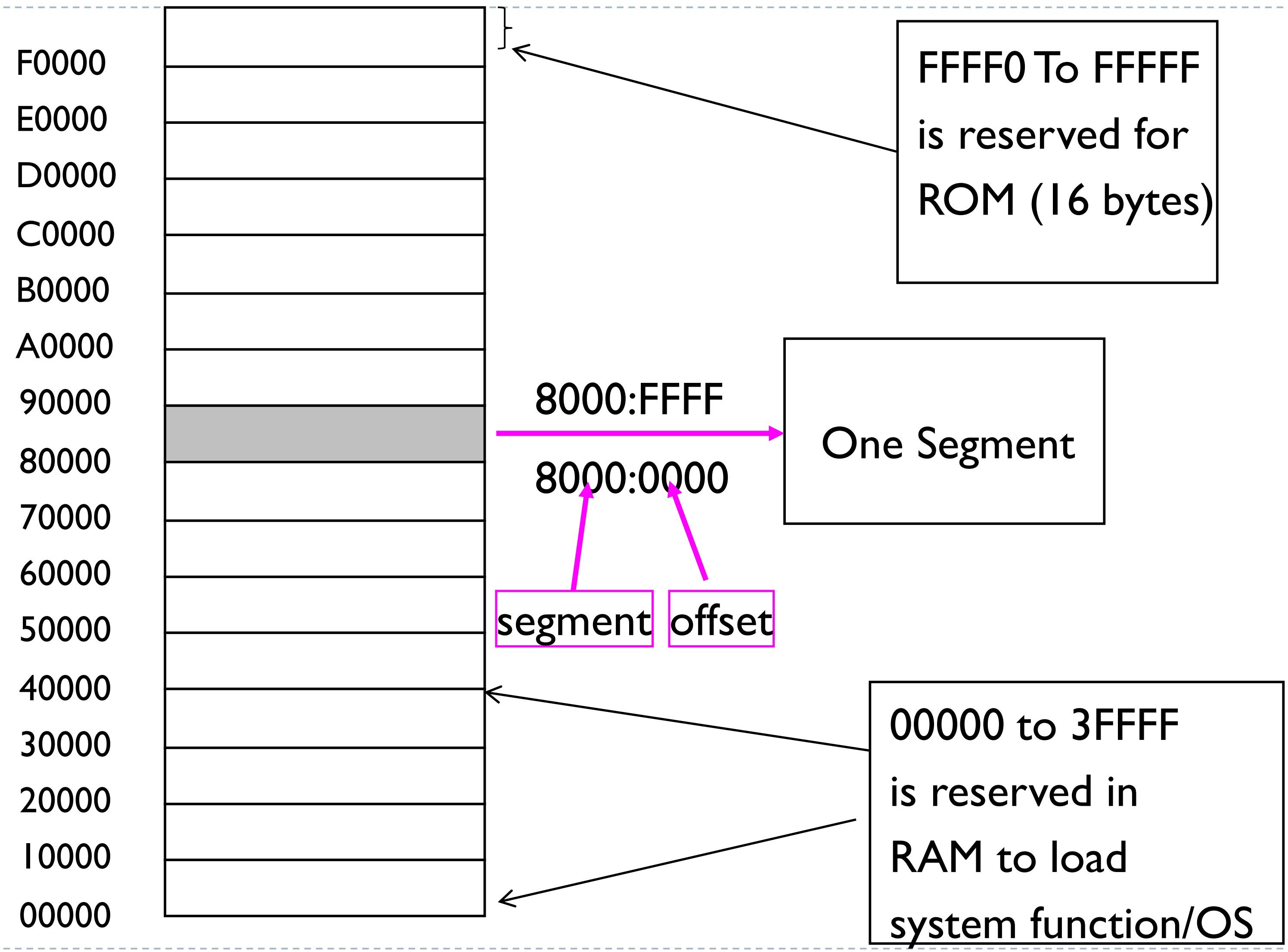
Memory Segment and Offset Concept

- ***Memory segment*** is a block of 2^{16} (64) KBytes consecutive memory bytes.

- Each segment is identified by a 16-bit number called **segment number**, starting with 0000 up to FFFFh. Segment registers hold segment number.

- Within a segment, a memory location is specified by giving an **offset** (16-bit) = It is the number of bytes from the beginning of the segment (0$\rightarrow$ FFFFh).

Memory Segment and Offset Concept



Memory Segment and Offset Concept

- A memory location may be specified by a ***segment number*** and ***offset*** (logical address).

  Example :

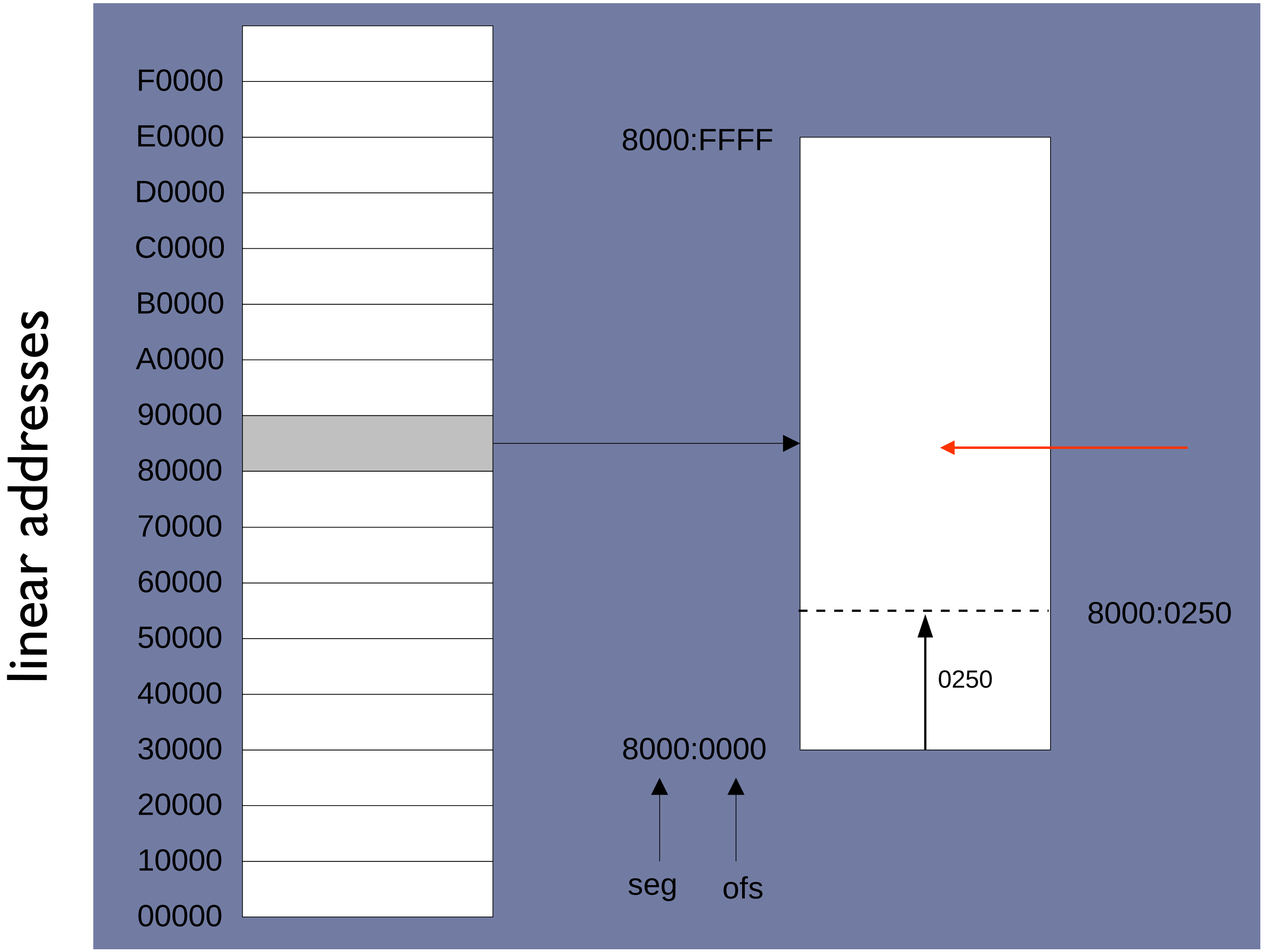
  A4FB : 4872 h

  Segment　　Offset

- **Offset:** is the distance from the beginning to a particular location in the **segment.**

- **Segment Number:** defines the starting of the segment within the memory space.

Memory Segment and Offset Concept



one segment

Memory Segment and Offset Concept

- **<u>Segmented Memory Address:</u>**
- Start location of the segment must be 20 bits → the absolute address is obtained by appending a hexadecimal zero to the segment number, i.e. , **multiplying by 16(10_h).**
  - Adds 4 Nibble bits at the lower portion of each 16-bit address.
- So, the **Physical Memory Address** is equal to:

Physical Address = Segment number X 10_h + Offset

- Physical **Address** for **A4FB : 4872**

A4FB0 h
+ 4872 h
A9822 h (20 Bits)

Physical Location of Segments

- **Segment 0**
  - **starts** at address 0000:0000 → 00000 h
  - **ends** at address 0000:FFFF → 0FFFF h
- **Segment 1**
  - **starts** at address 0001:0000 → 00010 h
  - **ends** at address 0001:FFFF → 1000F h
- Overlap occurs between the Segment 0 and 1 having varying size.
  - **Advantage:** Utilization of memory would be higher.

Physical Location of Segments

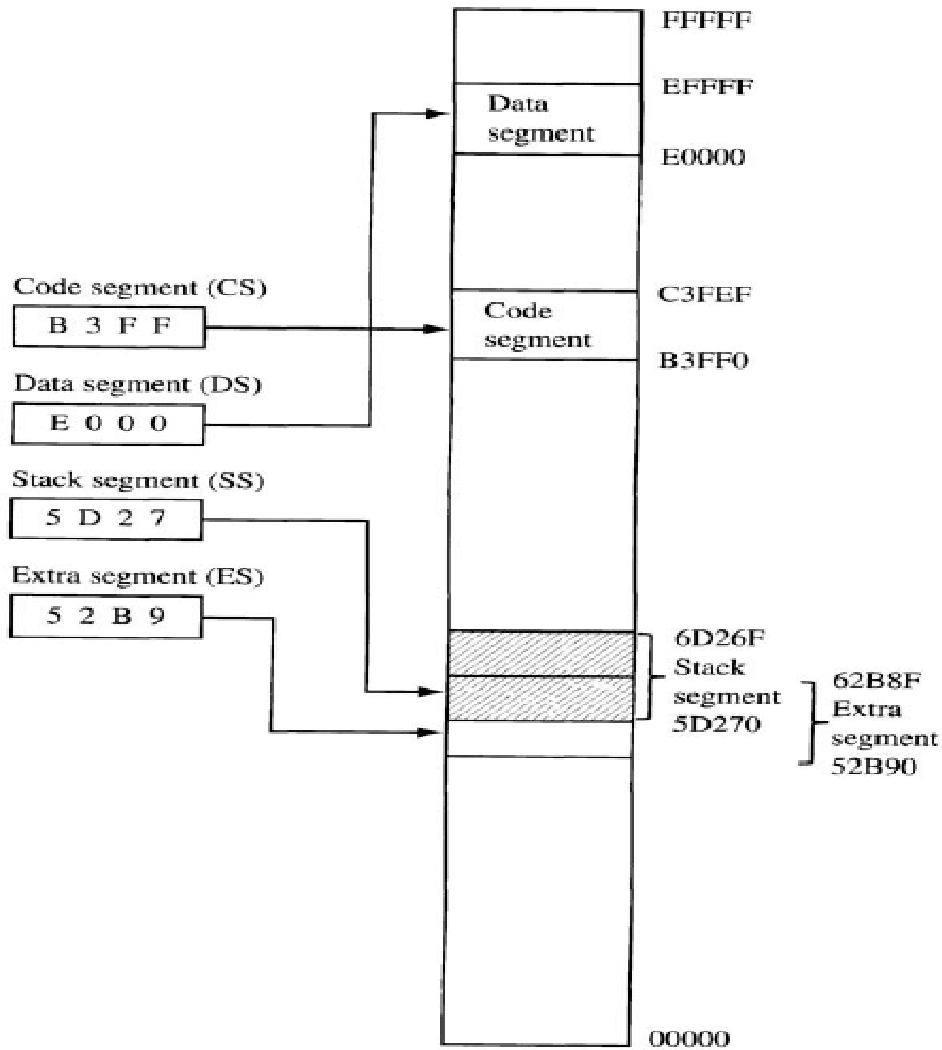
Segment	Physical Address (hex)
	...
	10021
	10020
End of Segment 2	1001F
	1001E
	...
	10010
End of Segment 1	1000F
	1000E
	...
	10000
End of Segment 0	0FFFF
	0FFFE
	...
	00021
Start of Segment 2	00020
	0001F
	...
	00011
Start of Segment 1	00010
	0000F
	...
	00003
	00002
	00001
Start of Segment 0	00000

Segment Registers

- Four Segment Registers in the BIU are used to hold the upper 16-bits of the starting addresses of four memory segments, namely
  - **Code segment CS**: holds segment address of the code segment.
  - **Data Segment DS:** holds segment address of the data segment.
  - **Extra Segment ES:** extra segment : holds alternate segment address of the data segment.
  - **Stack Segment SS:** holds segment address of the stack segment and used when sub-program executes.
- Codes , data , and stack are loaded into different memory segments (registers).

Memory Segment and Segment Registers

Segment Registers



Instruction Pointer (IP) and Code Segment Register

- **IP (Instruction pointer):**
  - Points to the next instruction.
  - Offset address relative to CS
- **Code segment CS**: holds segment address of the code segment.

- Suppose, CS = B3FFh and IP = 4214h

- Physical **Address** of the next instruction:

$$
\begin{array}{r}
\textbf{B3FF0 h} \\
\underline{\textbf{+ 4214 h}} \\
\textbf{B8204 h}
\end{array}
\text{ (20 Bits)}
$$

Stack Pointer and Index Registers

- Used for offset of data, often used as pointers. Unlike segment registers, they can be used in arithmetic and other operations.
- **SP (Stack Pointer)**:
  - Used with SS for accessing the stack segment.
  - Holds **Offset** address relative to SS
  - Always points to word (byte at even address)
  - An empty stack will had SP = FFFEh
- **BP (Base Pointer)**:
  - Used with SS to access data on the stack. However, unlike SP, BP can be used to access data in other segments.
  - Primarily used to access parameters passed via the stack
  - Holds **Offset** address relative to SS

Stack Pointer and Stack Segment Register

- Suppose, SS = 5D27h and SP = FFE0h

- Physical **Address** of the Top of Stack (ToS) information/data:

$$
\begin{array}{r}
\textbf{5D270 h} \\
\underline{\textbf{+ FFE0 h}} \\
\textbf{6D250 h} \text{ (20 Bits)}
\end{array}
$$

Data Pointer and Index Registers

- **SI (Source Index):**
  - Source of string operations. Used with DS (or ES).
  - Can be used for pointer addressing of data with effective address (EA)
  - Used as source in some string processing instructions
  - Offset address relative to DS
- **DI (Destination Index):**
  - Destination of string operation. Used with ES (or DS).
  - Can be used for pointer addressing of data
  - Used as destination in some string processing instructions
  - Offset address relative to ES

Source Index and Data Segment Register

- Suppose, DS = E000h and SI (EA) = 437Ah

- Physical **Address** of the data:

$$\begin{array}{r} \textbf{E0000 h} \\ \underline{+\ \textbf{437A h}} \\ \textbf{E437A h}\ \text{(20 Bits)} \end{array}$$

Flag Register

- **Flags Register:** A 16-Bits register specify status of CPU and information about the results of the arithmetic operations.
- Flags Register determines the current state of the processor.
- It is modified automatically by CPU after mathematical operations, this allows to determine the type of the result, and to determine conditions to transfer control to other parts of the program.
- Generally you cannot access these registers directly.

Bit Position

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	O	D	I	T	S	Z	x	A	x	P	x	C

O = Overflow	S = Sign
D = Direction	Z = Zero
I = Interrupt	A = Auxiliary Carry
T = Trap	P = Parity
x = undefined	C = Carry

Flag Register

- **Carry Flag (CF)** - this flag is set to '1' when there is an unsigned overflow. For example when you add bytes 255 + 1 (result is not in range 0...255). When there is no overflow this flag is reset to 0.
- **Parity Flag (PF)** - this flag is set to '1' when there is even number of one bits in result, and reset to '0' when there is odd number of one bits.
- **Auxiliary Flag (AF)** - set to '1' when there is an unsigned overflow for low nibble (4 bits).
- **Zero Flag (ZF)** - set to '1' when result is zero. For non-zero result this flag is reset to '0'.

Flag Register

- **Sign Flag (SF)** - set to ’1’ when result is negative. When result is positive it is reset to ‘0’. (This flag takes the value of the most significant bit).
- **Trap Flag (TF)** - Used for on-chip single-step debugging.
- **Interrupt enable Flag (IF)** - when this flag is set to ’1’ CPU reacts to interrupts from external devices.
- **Direction Flag (DF)** - this flag is used by some instructions to process data chains, when this flag is set to ’0’ - the processing is done forward, when this flag is set to ‘1’ the processing is done backward.
- **Overflow Flag (OF)** - set to ’1’ when there is a signed overflow. For example, when you add bytes 100 + 50.

Flag Register (Example)

Flag (Status) Register

15				Flags$_H$								Flags$_L$			0
X	X	X	X	OF	DF	IF	TF	SF	ZF	X	AF	X	PF	X	CF

- Six of the flags are status indicators reflecting properties of the last arithmetic or logical instruction.
- For example, if register AL = 7Fh and the instruction ADD AL,1 is executed then the following happen
  - AL = 80h
  - CF = 0; there is no carry out of bit 7
  - PF = 0; 80h has an odd number of ones
  - AF = 1; there is a carry out of bit 3 into bit 4
  - ZF = 0; the result is not zero
  - SF = 1; bit seven is one
  - OF = 1; the sign bit has changed
- Can be used to transfer program control to a new memory location

```
ADD AL,1
JNZ 0100h
```

Thank You !!