DCAE ELECTRONIC DEVICES, CIRCUITS AND ARCHITECTURES

Department of Electronic Devices, Circuits and Architectures

ASIC / FPGA Verification Course

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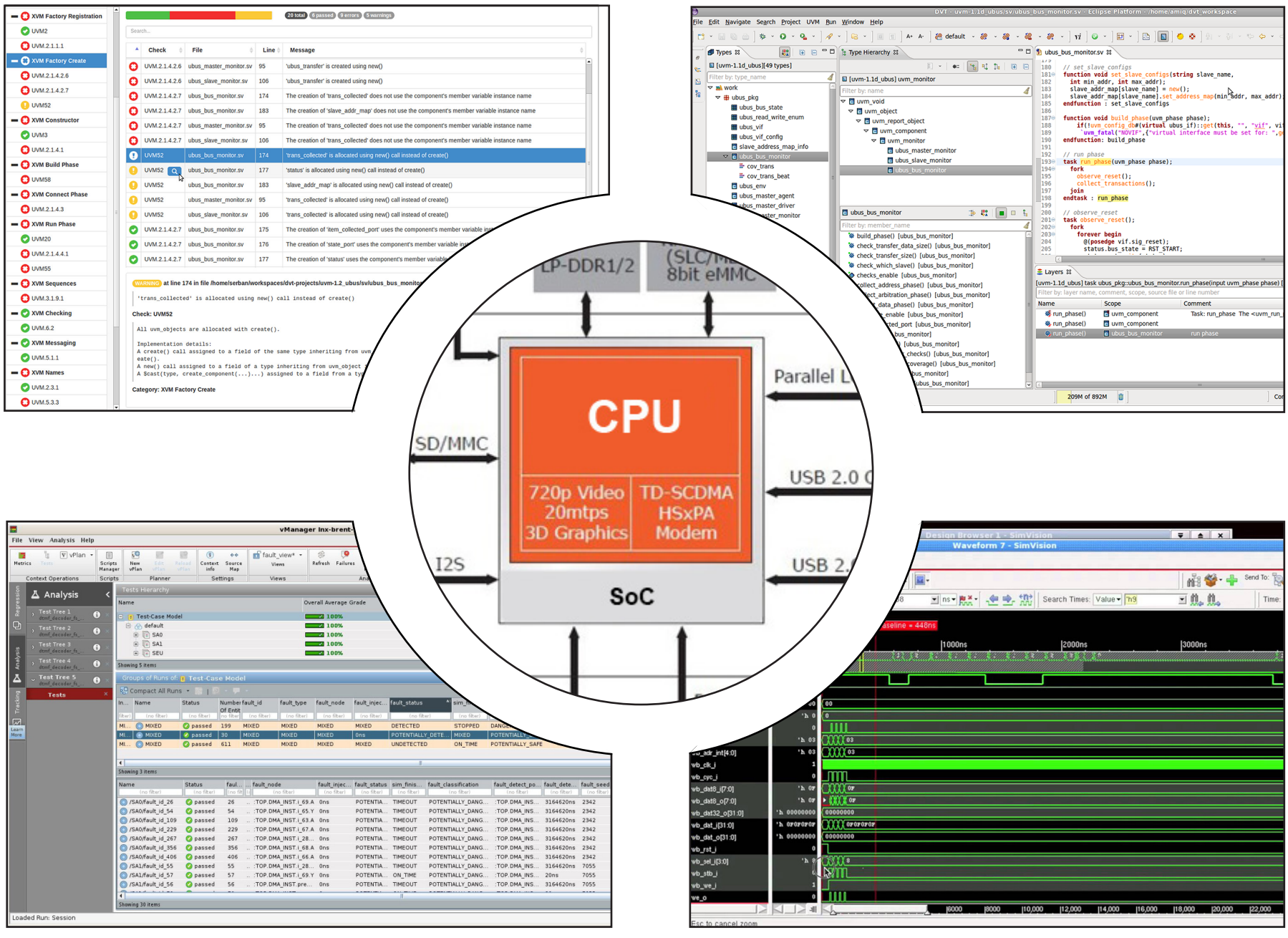
Starting November 2nd, 2015



Course Content

- Functional Verification Cycle
- Functional Verification Metrics
- Verification Planning
- Verification Environment Design
- Stimuli and Scenario Design
- Monitors and Checkers
- Verification Closure
- 100% Hands-On
- SystemVerilog, UVM
- SystemVerilog Assertions

Requirements

- Passion for technology
- Object Oriented Programming
- Digital Circuits Design (CID)
- Verilog / VHDL Knowledge

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