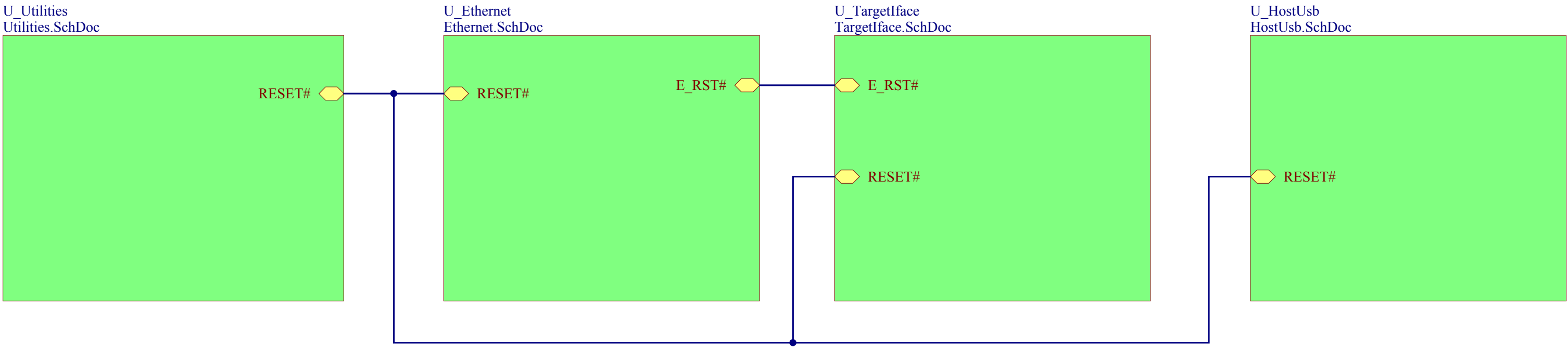


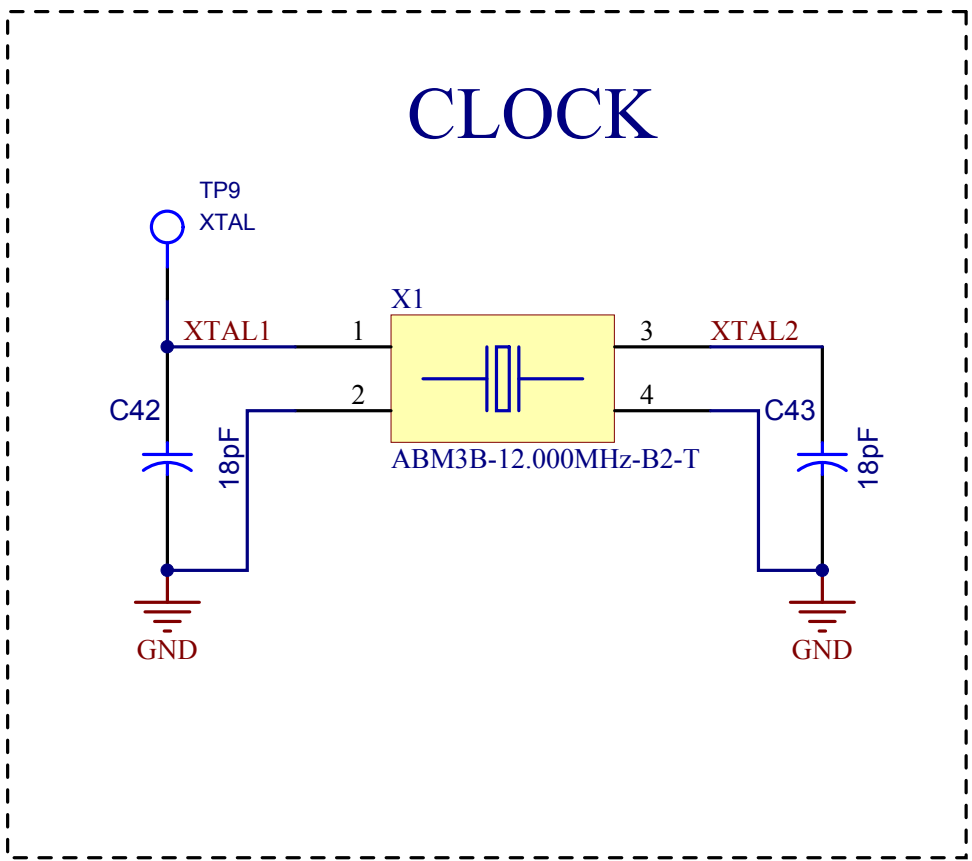
# High Resolution Circuit Diagrams for PE0003 August 2014



- CML  
Logo
- Serial Number  
& Mod 1-9  
Check Box
- Small  
6 Layer  
Box

## POWER SUPPLY

The diagram illustrates the power supply circuit for the LPC4330FBD144\_00003B. The circuit includes a power source (J11) connected to a diode (D7) for protection. The output of the diode is connected to a 5V regulator (U7, ZLDO1117G33TA). The regulator's input is connected to a 5V source (TP3) and its output is connected to a 3V3 source (TP4). The 3V3 source is connected to the VDDA and VSSA pins of the microcontroller (U1-6, LPC4330FBD144\_00003B). The microcontroller's VDDIO and VSSIO pins are connected to a 3V3 source. The microcontroller's XTAL1 and XTAL2 pins are connected to a 3V3 source. The circuit also includes several capacitors (C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41) and a resistor (R27, 330R) connected to the 3V3 source.



# BOOT

The diagram shows the BOOT pin configuration. The BOOT pin is connected to a 3V3 supply through a network of resistors (R29, R30, R31, R32) and capacitors (n/f). The BOOT pin is also connected to a network of resistors (R36, R37, R38, R39) and capacitors (10K) connected to GND. The BOOT pin is also connected to four other pins: BOOT\_M0, BOOT\_M1, BOOT\_M2, and BOOT\_M3.

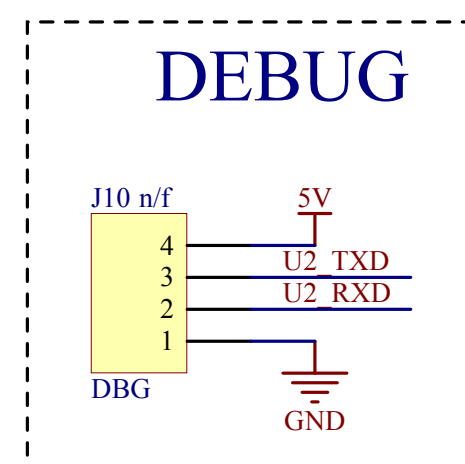
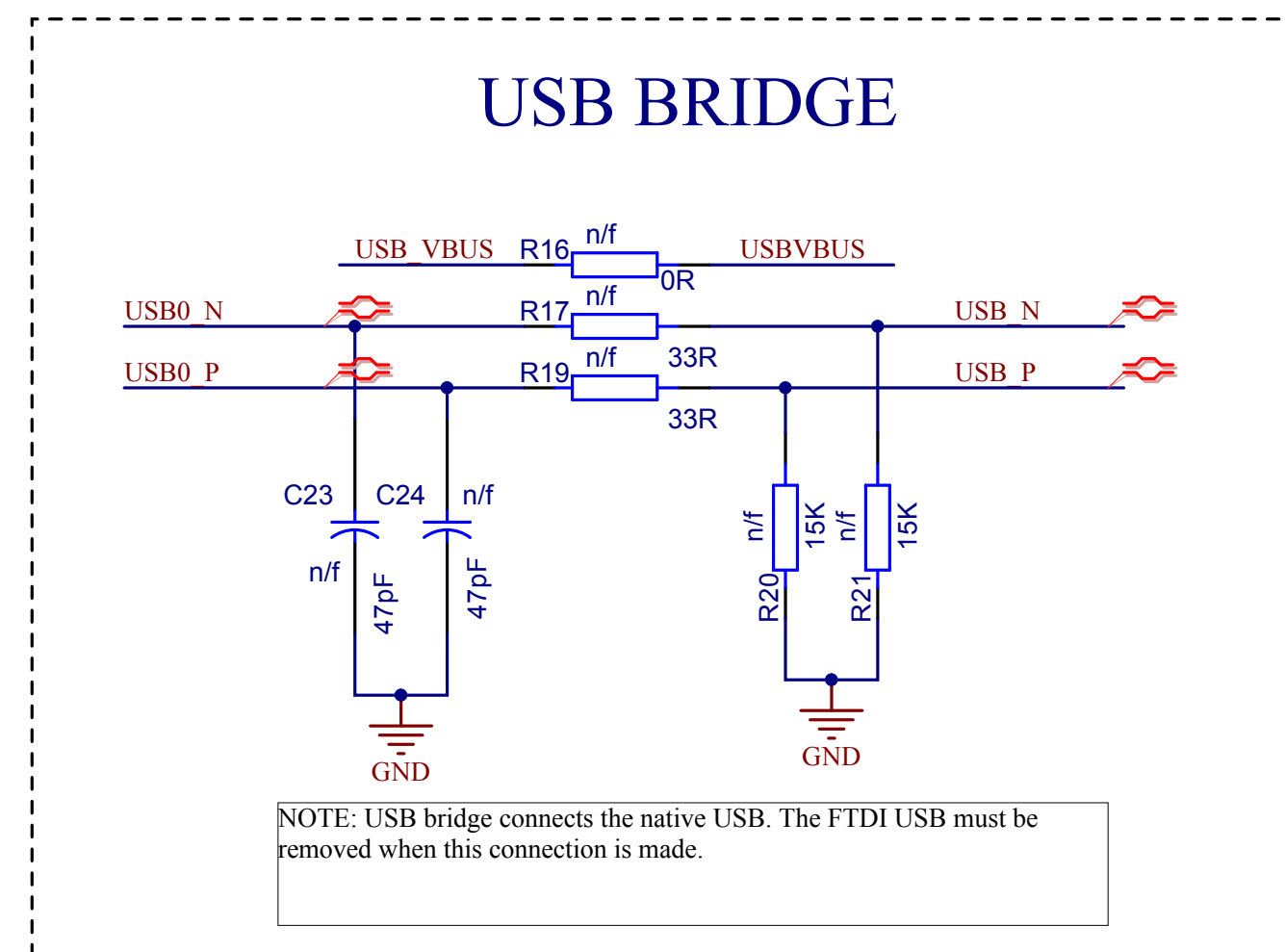
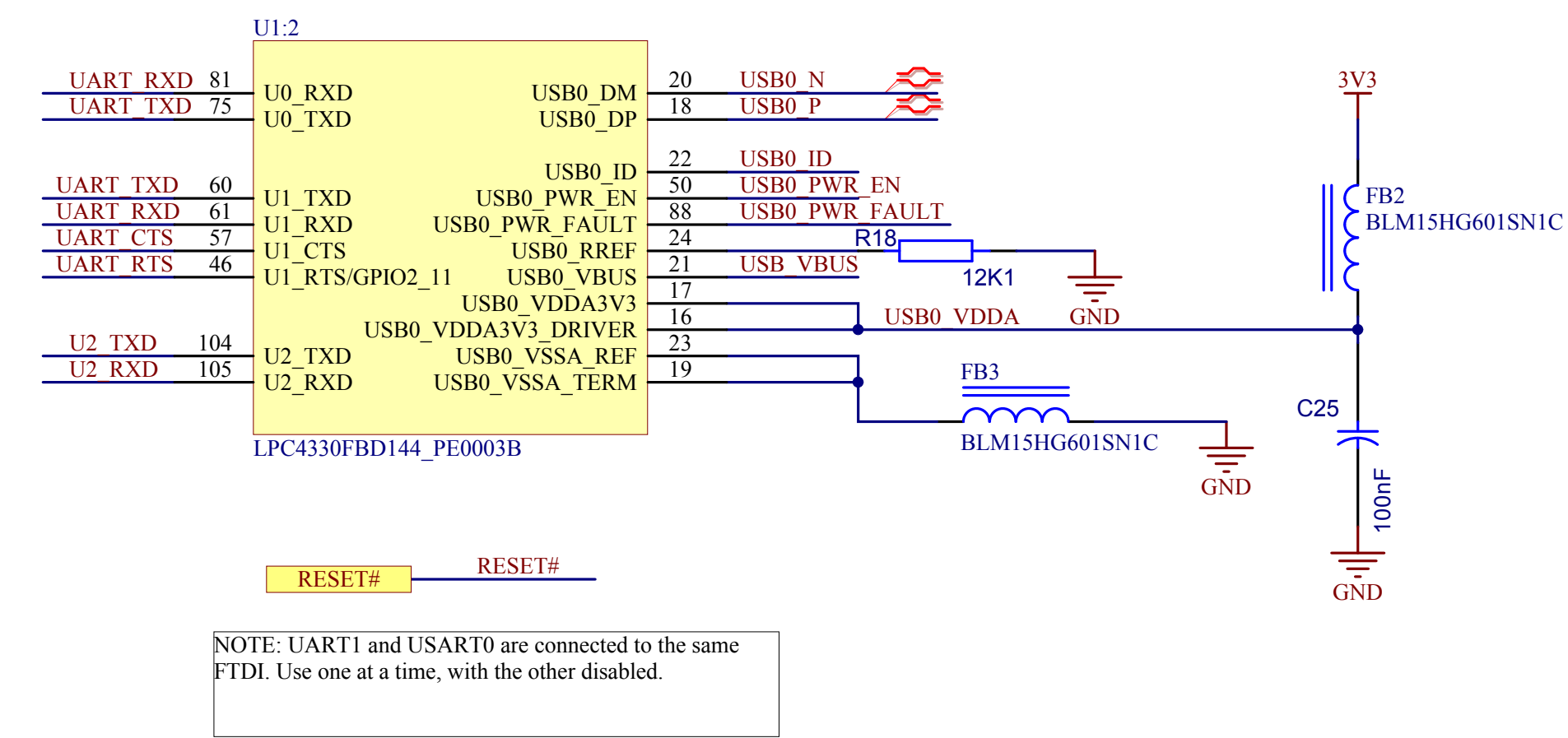
The diagram shows a JTAG connection setup. A 3V3 power supply is connected to pin 1 of the J13 connector. Pin 2 is connected to SWIO/TMS. Pin 3 is connected to SWDCLK/TCLK. Pin 4 is connected to SWO/TDO. Pin 5 is connected to NC/TDI. Pin 6 is connected to RESET#. Pin 7 is connected to GND. Pin 8 is connected to GND. Pin 9 is connected to GND. Pin 10 is connected to GND.

## SD CARD

The diagram illustrates the electrical connections for an SD card interface. The microcontroller's pins are connected to the SD card's pins as follows:

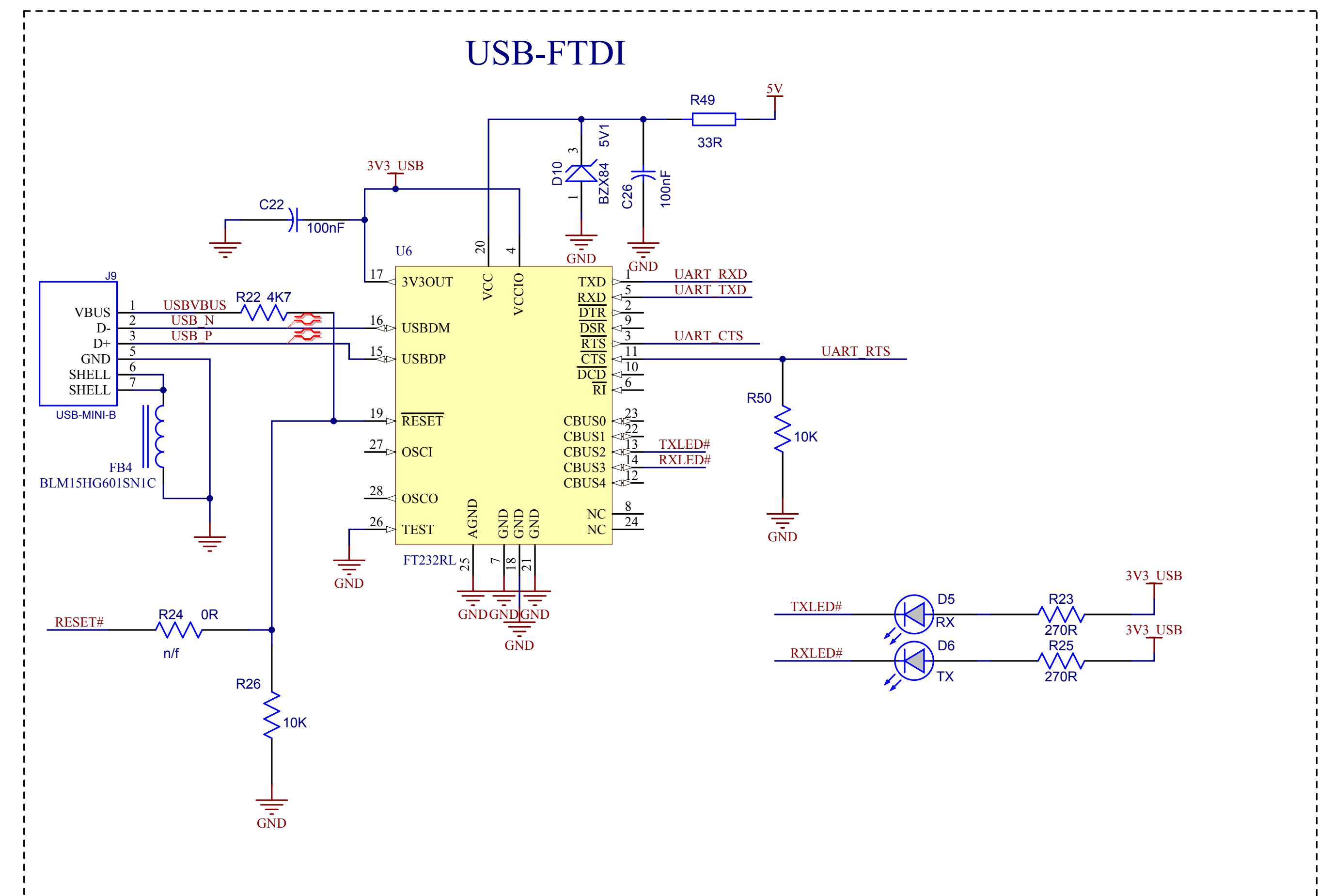
- SD\_DAT2 (pin 1) to DAT2
- SD\_DAT3 (pin 2) to CD/DAT3
- SD\_CMD (pin 3) to CMD
- SD\_CLK (pin 4) to VDD
- SD\_DAT0 (pin 5) to CLK
- SD\_DAT1 (pin 6) to VSS
- SD\_DAT0 (pin 7) to DAT0
- SD\_DAT1 (pin 8) to DAT1

The microcontroller's SHLD1 and SHLD2 pins (pins 9 and 10) are connected to GND. The circuit also includes a 3V3 supply, a 47µF 6.3V capacitor (C44) connected to GND, and a 10K pull-up resistor (R41) connected to 3V3.

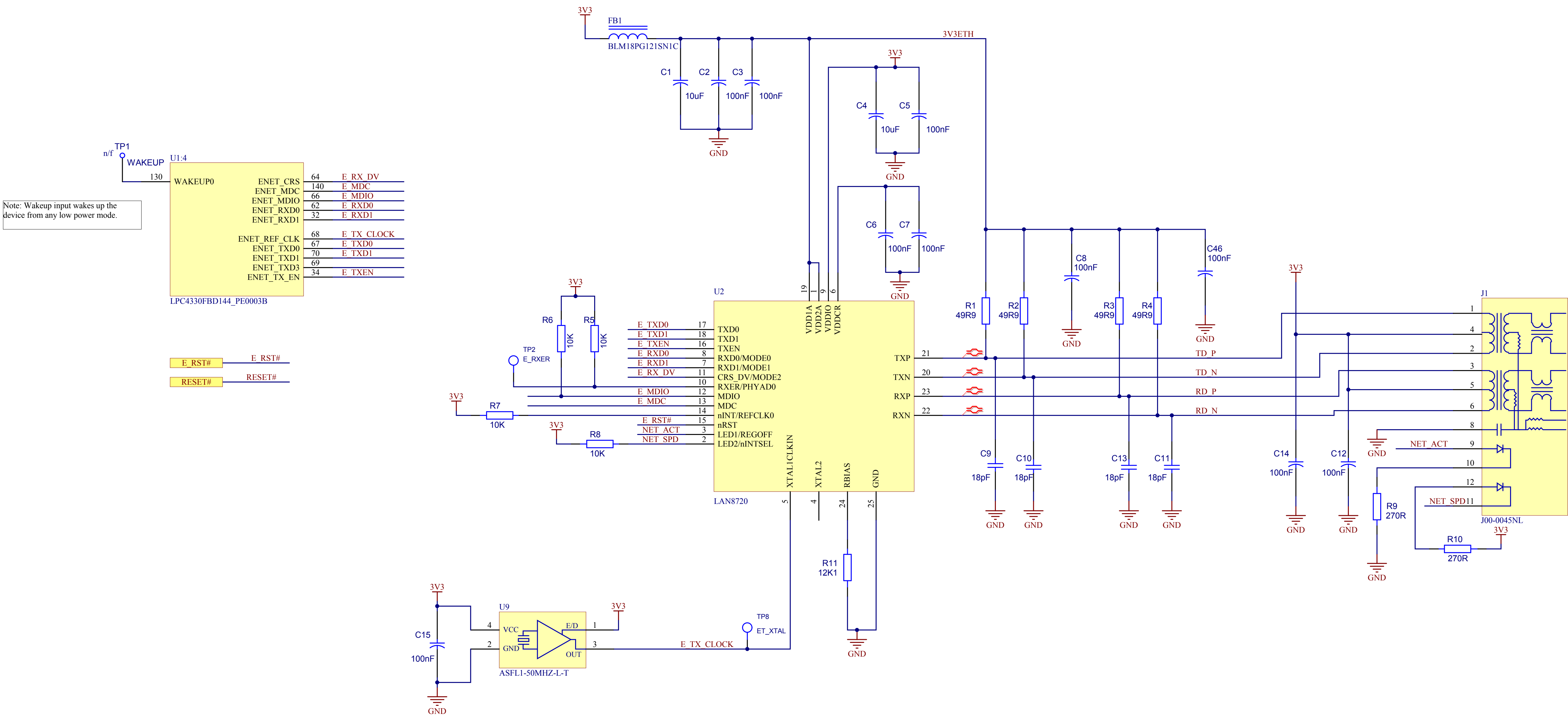


USB ROUTING GUIDELINES

- ⇒Route USB trace pairs together [ DM & DP].
- ⇒Do not route USB traces under crystals, oscillators,magnetic devices or ICs that use and/or duplicate clocks.
- ⇒Route high-speed USB signals using a minimum of vias and corners.
- ⇒Use 0.5mm minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality.



ETHERNET



ROUTING GUIDELINES

- => Keep trace length difference between TX+ and TX- (or RX+ and RX-) in 700 mils.
- => Keep RX+/- signal on the top layer, the RX+/- signal should avoid any vias, if possible. Avoid right angle signal trace.
- =>The crystal/oscillator clock and the switching noise from digital signals should be far away from TX+/-, RX+/- pairs.
- =>Keep TX, RX differential signals running symmetric, equal length, and closely. The trace spacing between TX+ and TXor between RX+ and RX- pair should be 8 to 10 mils.

The better spacing between TX+/- and RX+/- pairs should be larger than 200 mils

- =>The trace length from LAN8720 to the transformer should not be longer than 5 inches, keep the trace as straight as possible, and keep it parallel for differential pairs.
- =>The termination resistors 49.9Ohm and capacitors of TX± and RX± pairs should be placed near the transformer side and should be shorter than 400 mils.



