Al Azhar University
Faculty of Engineering (G)
Comp & Sys Department
Final Exam 2021/2022

Course: Computer Aided Design
Grade: 4th Year
Allowed Time:3 hour
Total Marks: 70

The Examination consists of five questions in two pages

Q1. Answer the following questions (10 degree)

1. **Define the terms:**

   CAD **CAM** **EDA** **PCB**

2. **Differentiate between the terms SSI, MSI, LSI and VLSI? And when CAD started evolving?**

Q2. Illustrate with a diagram only (10 degree)

a. **IC design & manufacturing process.**

b. **The design flow in VLSI.**

Q3. Design a 1-bit half adder circuit by completing these steps (20 degree):

1. **Design the circuit truth table with two inputs a, b and two outputs sum, carry.**
2. **Draw the Circuit Schematic?**
3. **Write the Boolean Expression?**
4. **Write the circuit Verilog HDL code module with three different Levels of design abstraction?**

(The rest of questions in the next page)

Q4. **A one-hot decoder is a circuit that has n inputs and 2n outputs.** **Each output will assert for one and only one input code. Since there are 2n outputs, there will always be one and only one output asserted at any given time. shows how to model a 2-to-4 one-hot decoder in Verilog with continuous assignment and logic operators.**

Illustrate the following (20 degree):

-The system block diagram and truth table.

-Output logic expression.

-Verilog modeling using logical operators.

Q5. Given the following Verilog code find (10 degree):

1. **The truth table.**
2. **Minimized output logic expression using the k-map.**

```
module SystemX (output wire F,
                input  wire A, B, C);

   assign F = ( !C && (!A || B) ) ? 1'b1 : 1'b0;

endmodule
```

The end of the questions

Best regards

Dr. Maha Medhat