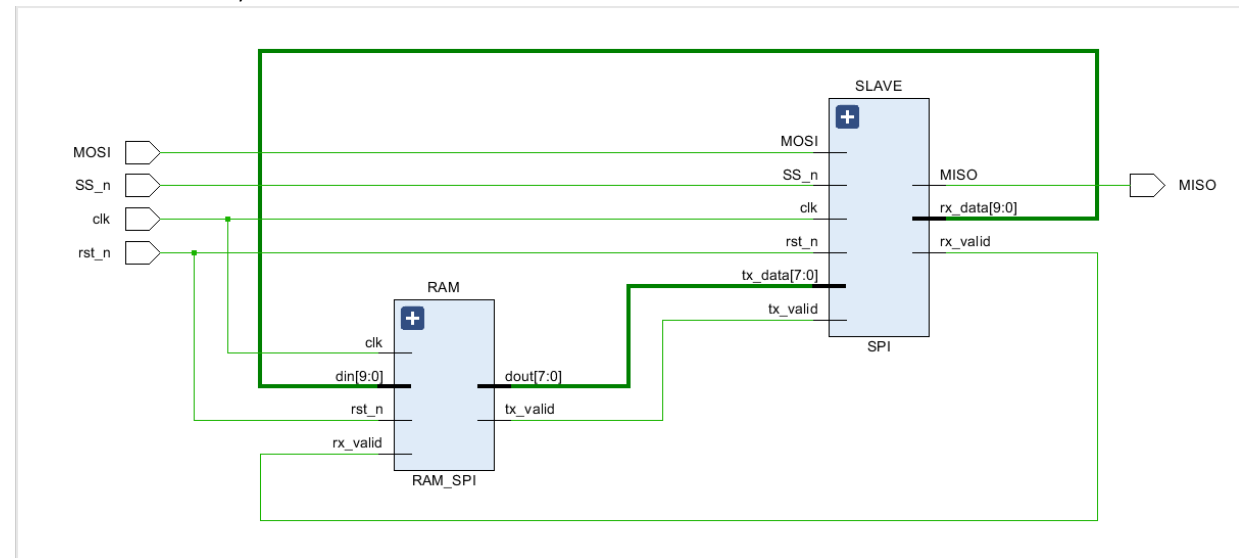


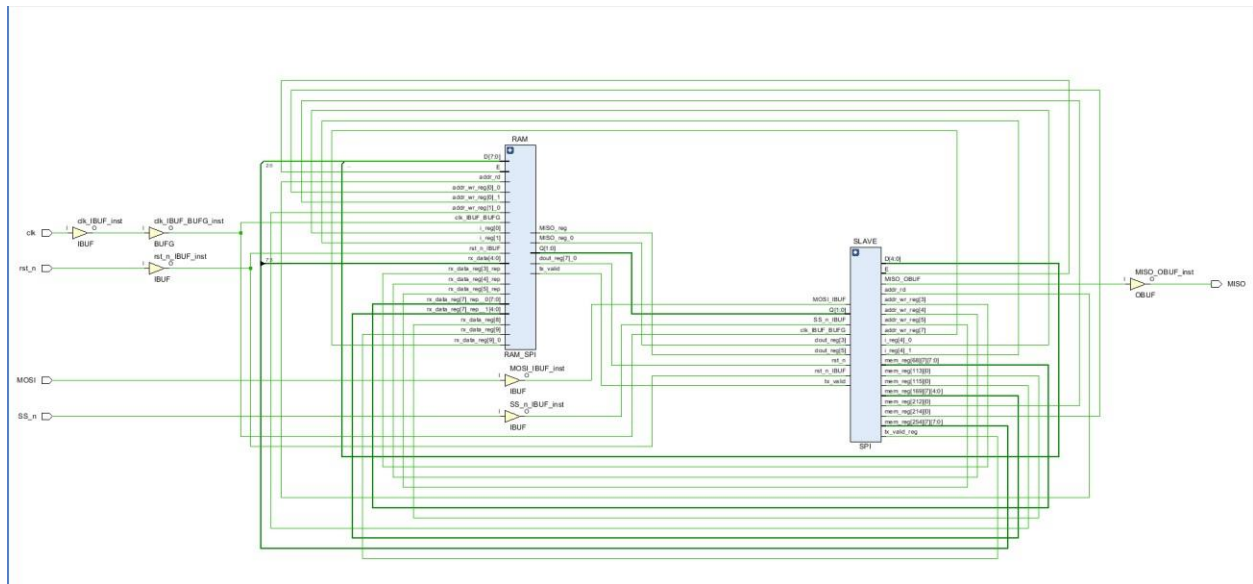
**Project**  
**SPI Slave with Single Port RAM**

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## Elaboration and Synthesis Schematics





# Synthesis Report

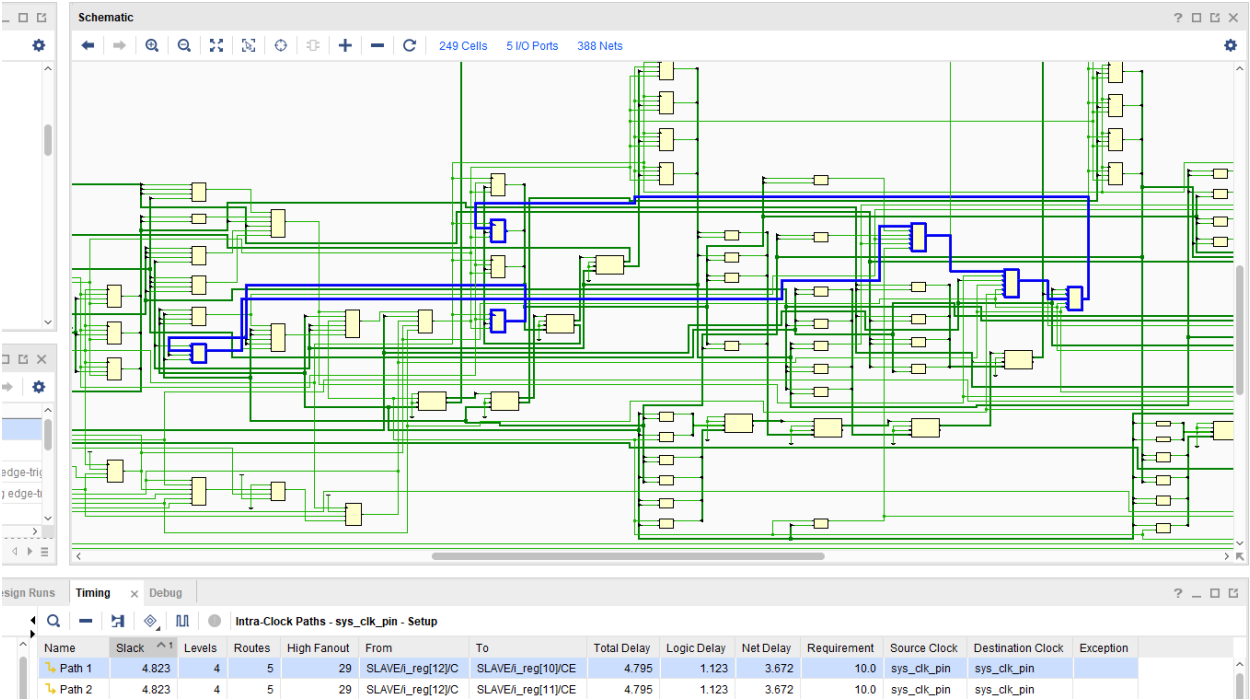
State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

INFO: [Synth 8-3354] encoded FSM with state register 'cs\_reg' using encoding 'sequential' in module 'SPI'

# Timing Report Snippet

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.823 ns	Worst Hold Slack (WHS): 0.145 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4333	Total Number of Endpoints: 4333	Total Number of Endpoints: 2179
All user specified timing constraints are met.		

Critical Path Snippet

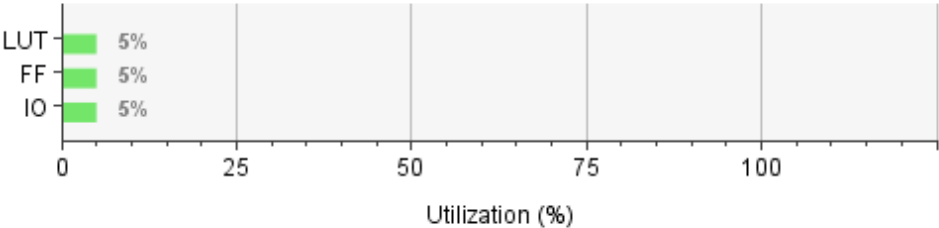


Implementation

Utilization Report

Summary

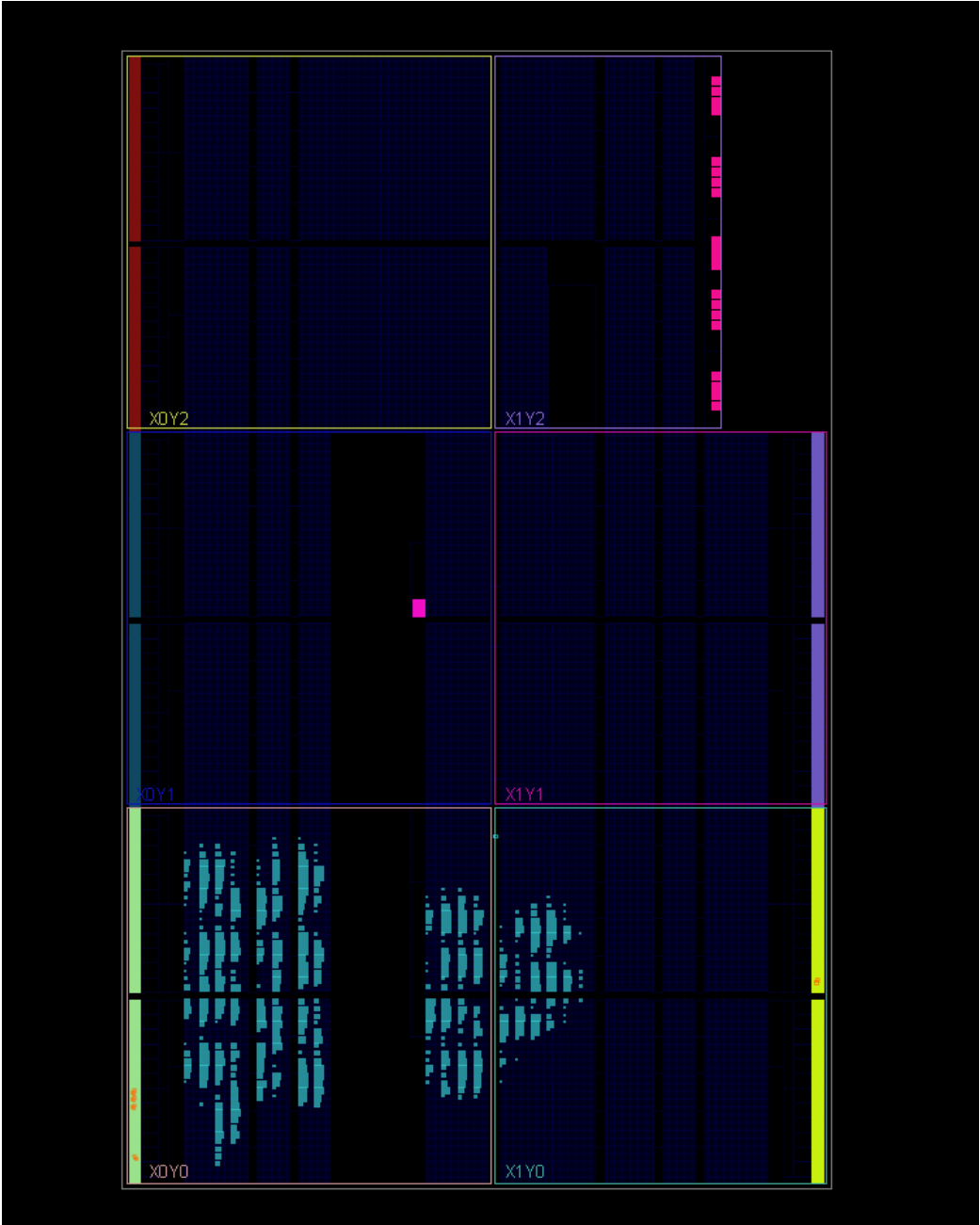
Resource	Utilization	Available	Utilization %
LUT	945	20800	4.54
FF	2182	41600	5.25
IO	5	106	4.72



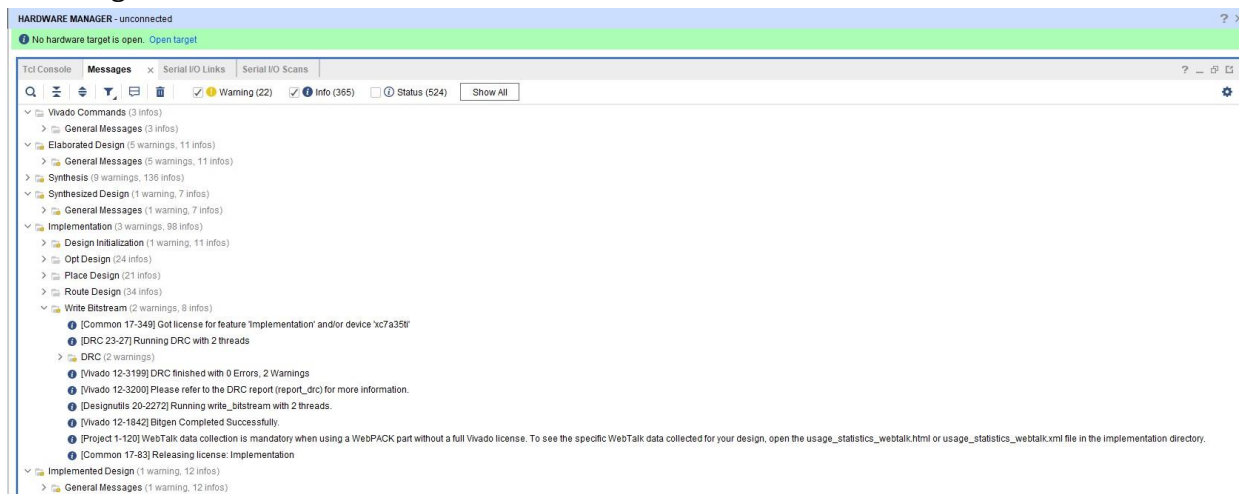
Timing Report Snippet

Runs	Timing	Utilization
Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1.545 ns	Worst Hold Slack (WHS): 0.197 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4333	Total Number of Endpoints: 4333	Total Number of Endpoints: 2179
All user specified timing constraints are met.		

FPGA Device Snippet



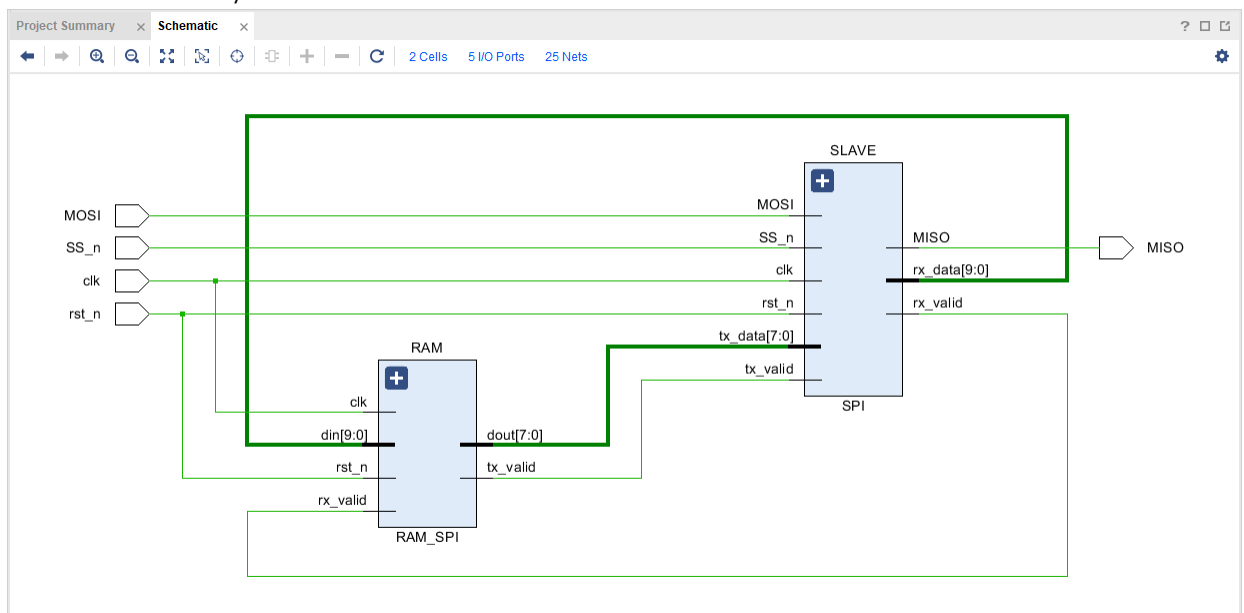
## “Messages” Tab

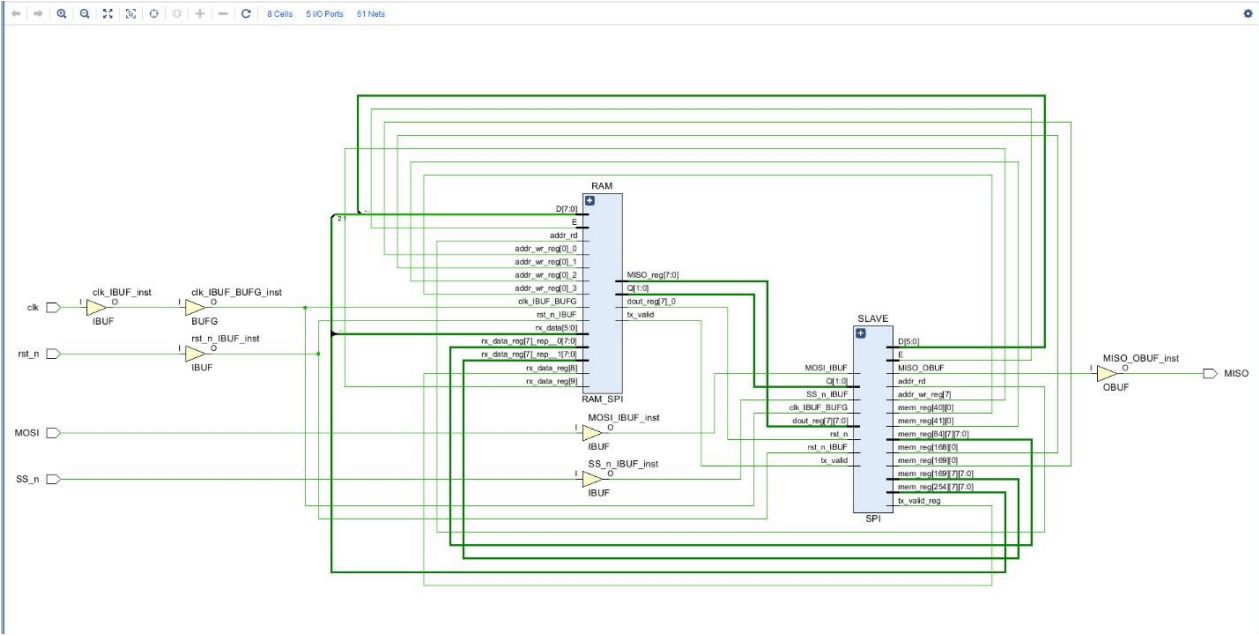


## Gray Encoding

### Synthesis

### Elaboration and Synthesis Schematics





Synthesis Report

State		New Encoding		Previous Encoding
IDLE		000		000
CHK_CMD		001		001
WRITE		011		010
READ_ADD		010		011
READ_DATA		111		100

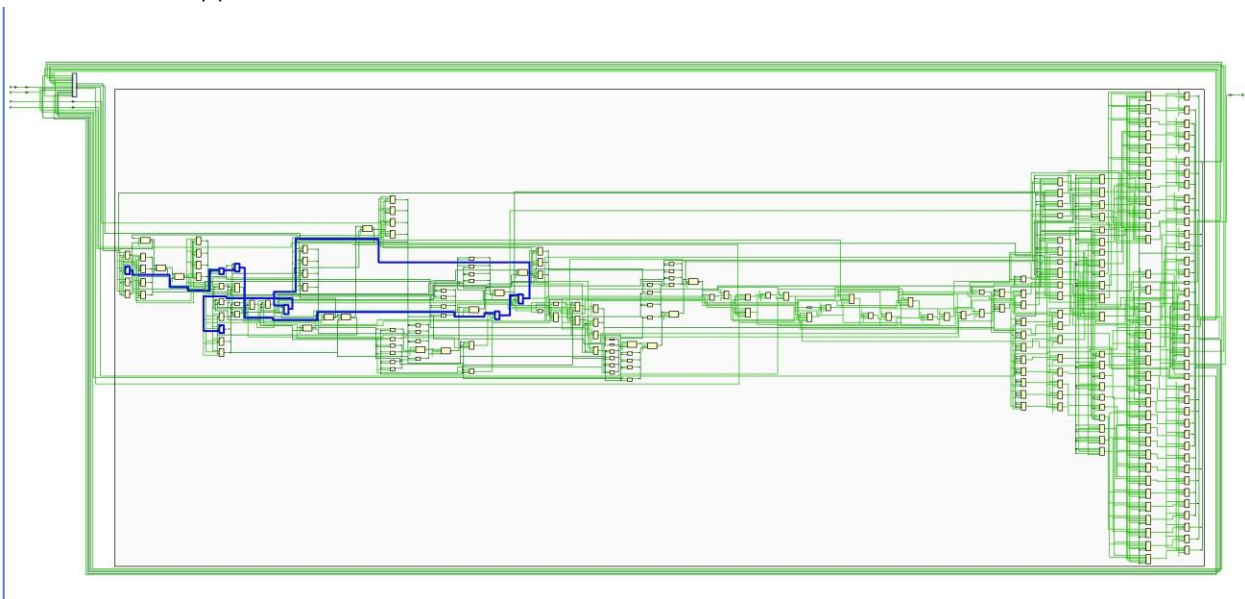
F0: [Synth 8-3354] encoded FSM with state register 'cs\_reg' using encoding 'gray' in module 'SPI'

Timing Report Snippet

Timing			
Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 3.764 ns	Worst Hold Slack (WHS): 0.145 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 4334	Total Number of Endpoints: 4334	Total Number of Endpoints: 2180	
All user specified timing constraints are met.			



Critical Path Snippet



Implementation

Utilization Report

Design Runs

Timing

Utilization ×

Summary

Resource	Utilization	Available	Utilization %
LUT	942	20800	4.53
FF	2183	41600	5.25
IO	5	106	4.72

LUT

FF

IO

5%

5%

5%

0

25

50

75

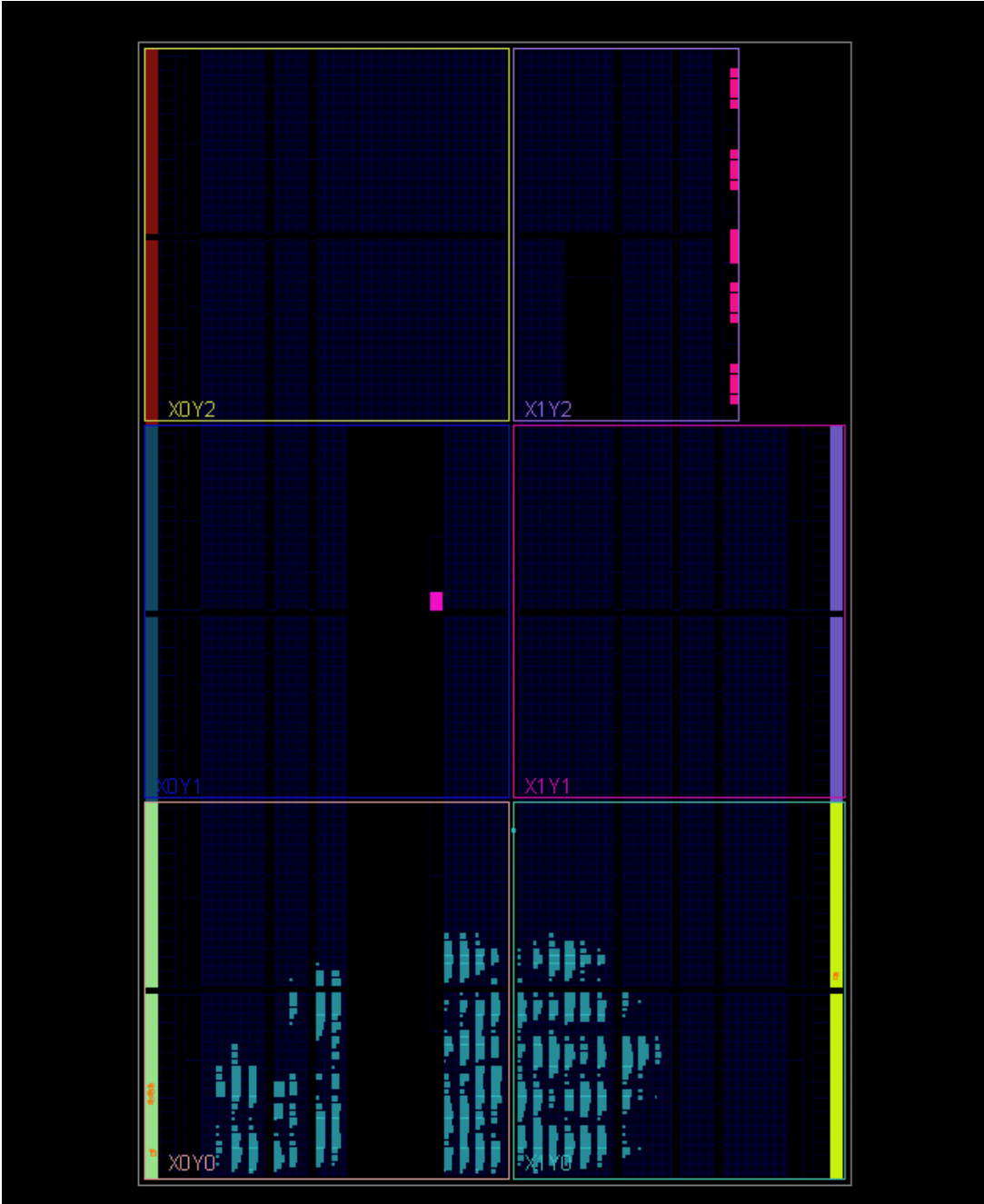
100

Utilization (%)

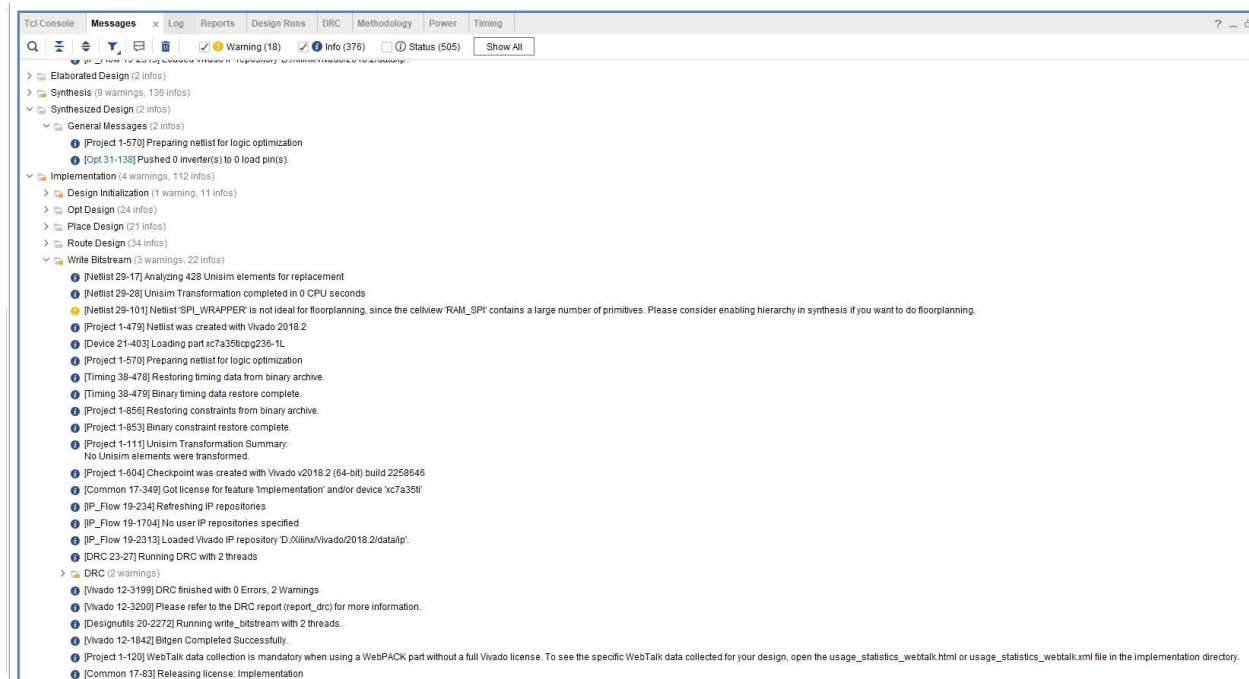
Timing Report Snippet

Timing			Utilization
Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 2.748 ns	Worst Hold Slack (WHS): 0.202 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 4334	Total Number of Endpoints: 4334	Total Number of Endpoints: 2180	
All user specified timing constraints are met.			

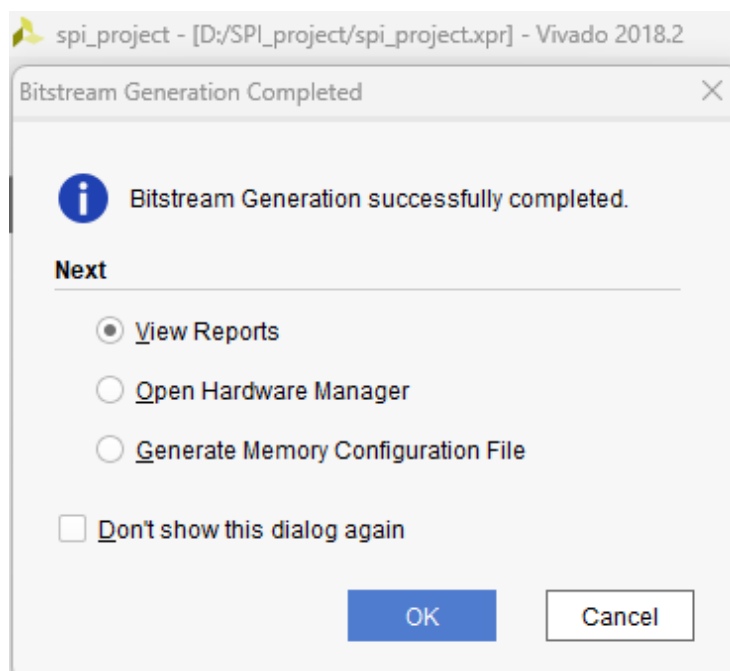
FPGA Device Snippet



## “Messages” Tab



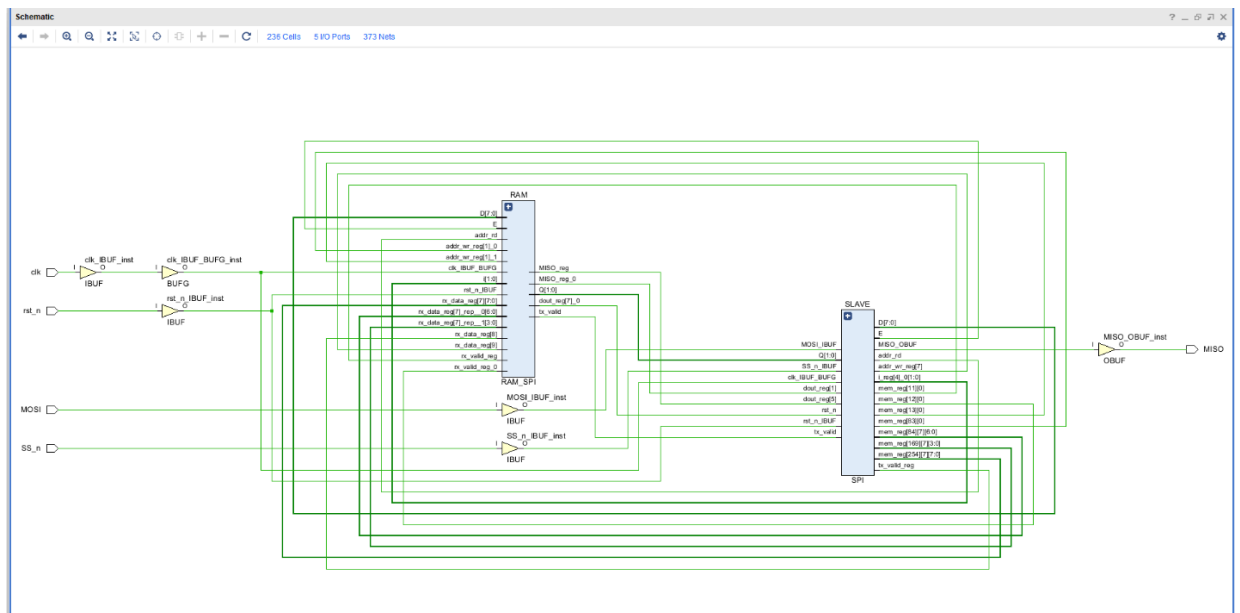
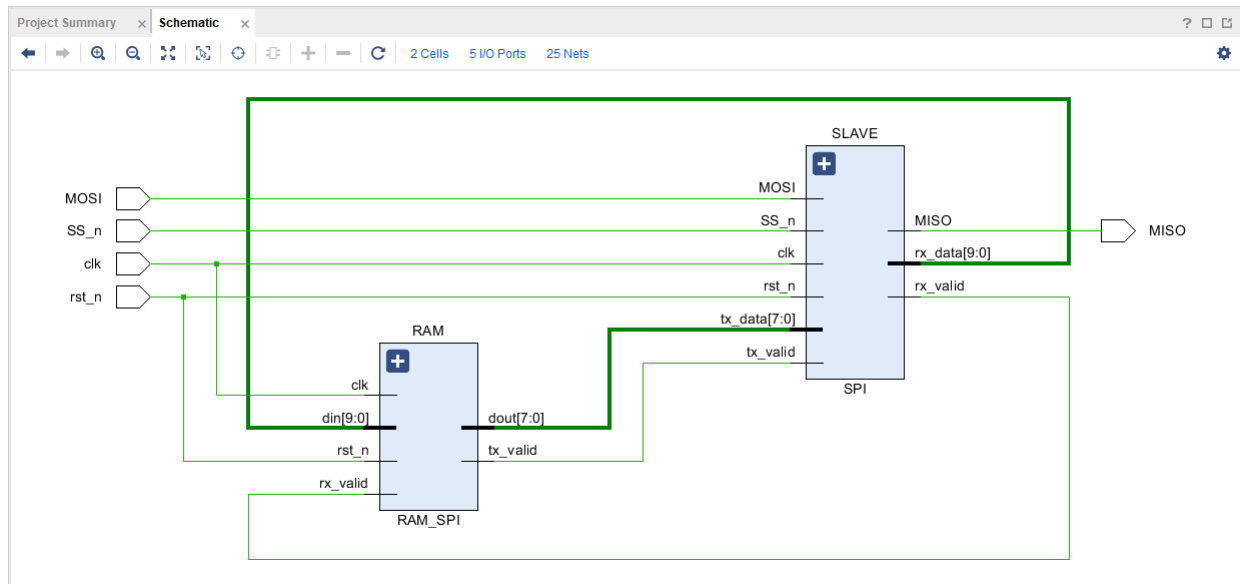
Note: since the gray encoding has the highest setup time slack, we performed the debug core on It and this the bitstream generation success.



# One\_Hot Encoding

## Synthesis

### Elaboration and Synthesis Schematics



Synthesis Report

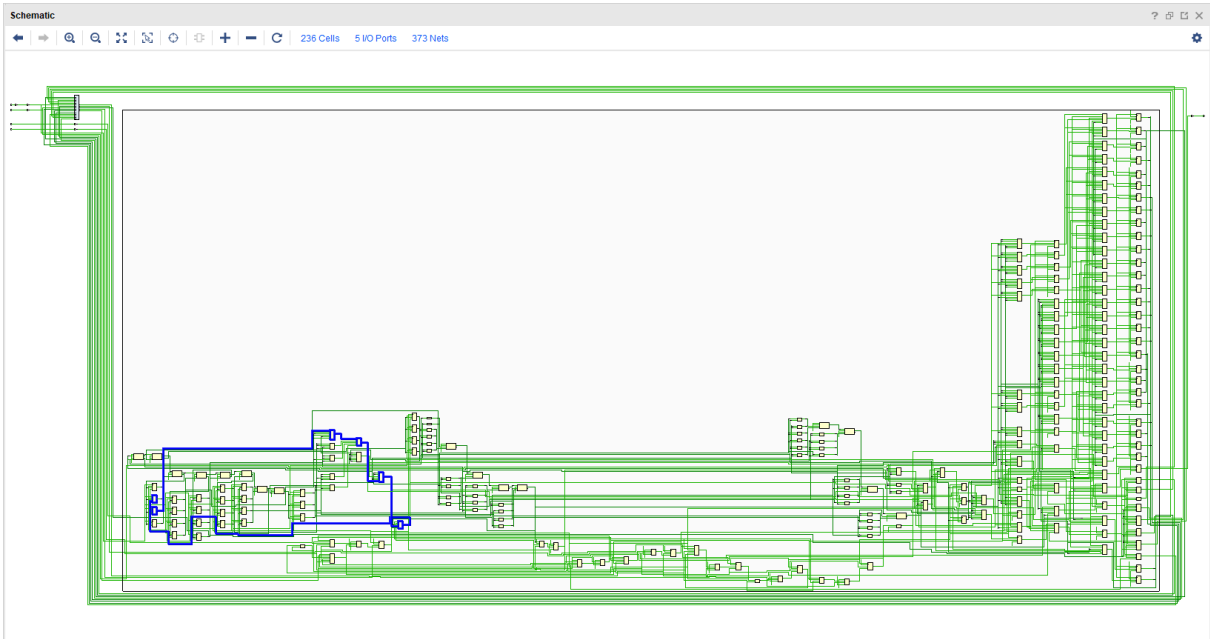
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

FO: [Synth 8-3354] encoded FSM with state register 'cs\_reg' using encoding 'one-hot' in module 'SPI'

Timing Report Snippet

uns	Timing	Utilization	Debug
Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 4.405 ns	Worst Hold Slack (WHS): 0.145 ns	Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 4315	Total Number of Endpoints: 4315	Total Number of Endpoints: 2171	
All user specified timing constraints are met.			

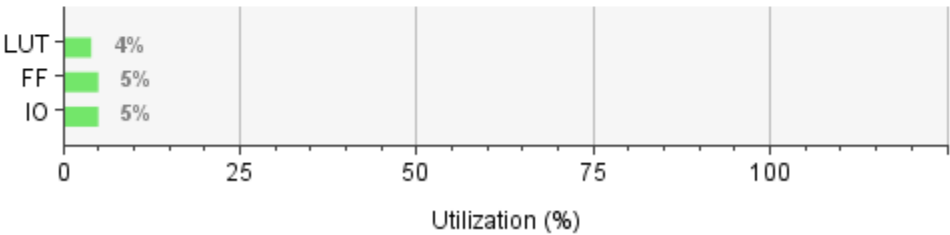
Critical Path Snippet



Implementation  
Utilization Report

Summary

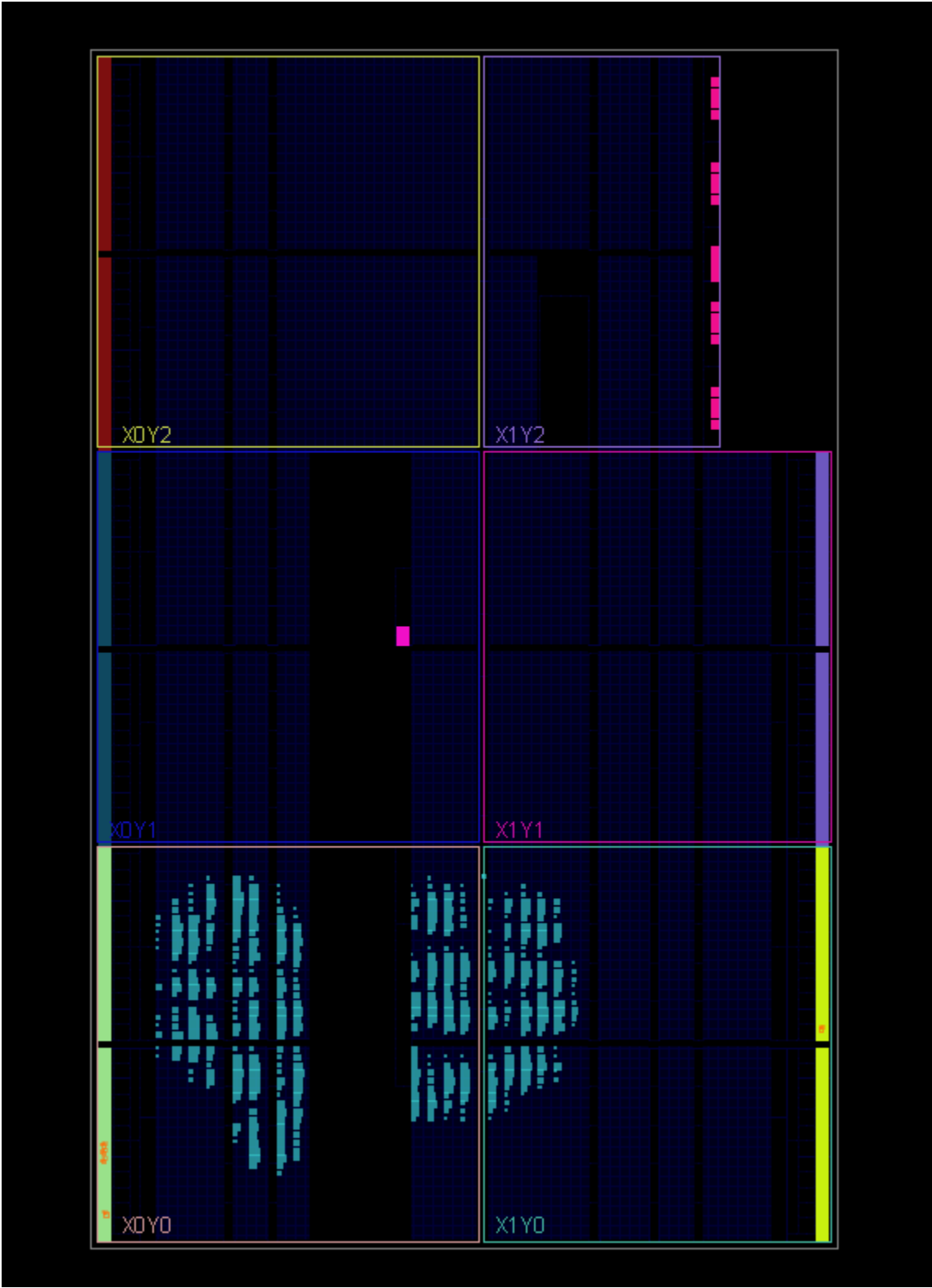
Resource	Utilization	Available	Utilization %
LUT	933	20800	4.49
FF	2176	41600	5.23
IO	5	106	4.72



Timing Report Snippet

ts	Design Runs	Timing	×
Design Timing Summary			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 2.079 ns		Worst Hold Slack (WHS): 0.210 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4315		Total Number of Endpoints: 4315	Total Number of Endpoints: 2171
All user specified timing constraints are met.			

FPGA Device Snippet



## “Messages” Tab

The screenshot displays the Vivado Messages tab, which is part of the IDE's interface. The top bar shows tabs for Utilization, Tcl Console, Messages (active), Log, Reports, Design Runs, and Timing. Below the tabs, there's a search bar and filters for Warning (16), Info (349), and Status (483). A 'Show All' button is also present. The main area lists messages grouped by category:

- Vivado Commands** (3 infos)
  - General Messages** (3 infos)
    - [IP\_Flow 19-234] Refreshing IP repositories
    - [IP\_Flow 19-1704] No user IP repositories specified
    - [IP\_Flow 19-2313] Loaded Vivado IP repository 'D:/xilinx/Vivado/2018.2\data/ip/.'
- Synthesis** (0 warnings, 136 infos)
- Implementation** (3 warnings, 98 infos)
  - Design Initialization** (1 warning, 11 infos)
  - Opt Design** (24 infos)
  - Place Design** (21 infos)
  - Route Design** (34 infos)
  - Write Bitstream** (2 warnings, 8 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
    - [DRC 23-27] Running DRC with 2 threads
    - DRC** (2 warnings)
      - [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings
      - [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.
      - [Designutils 20-2272] Running write\_bitstream with 2 threads.
      - [Vivado 12-1842] Bitgen Completed Successfully.
      - [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.
      - [Common 17-83] Releasing license: Implementation
- Implemented Design** (1 warning, 14 infos)
  - General Messages** (1 warning, 14 infos)