Project

SPI Slave with Single Port RAM

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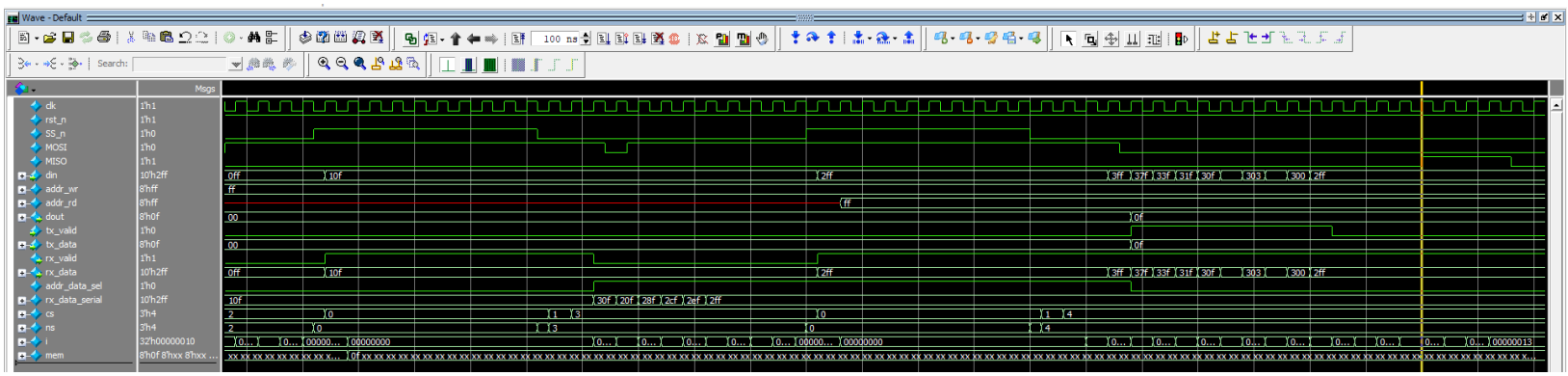
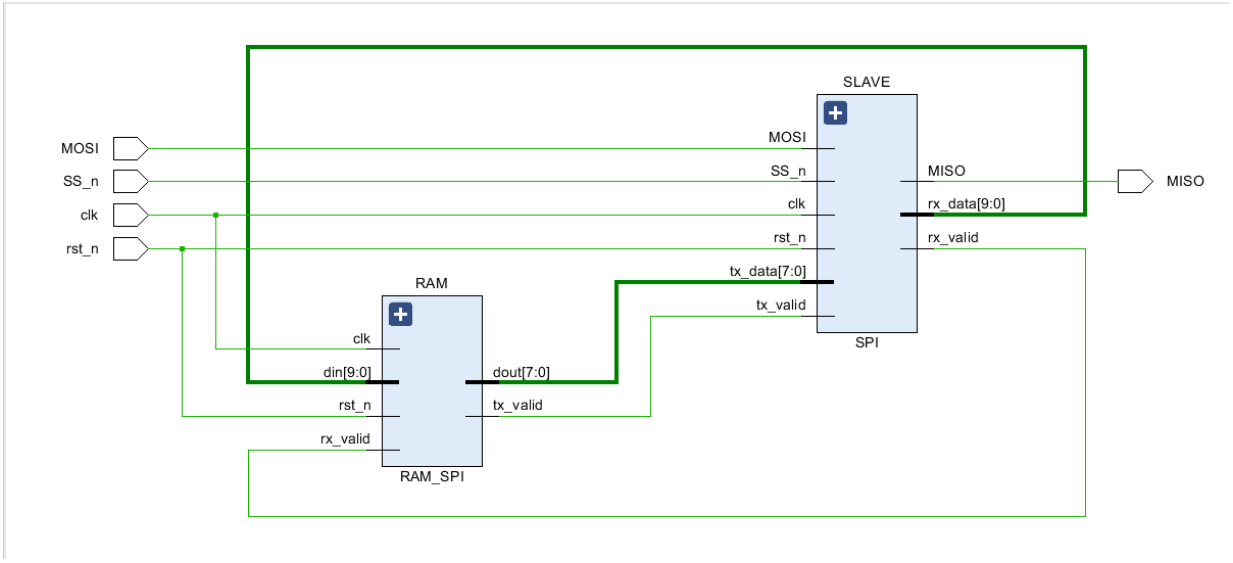
QuestaSim Snippets

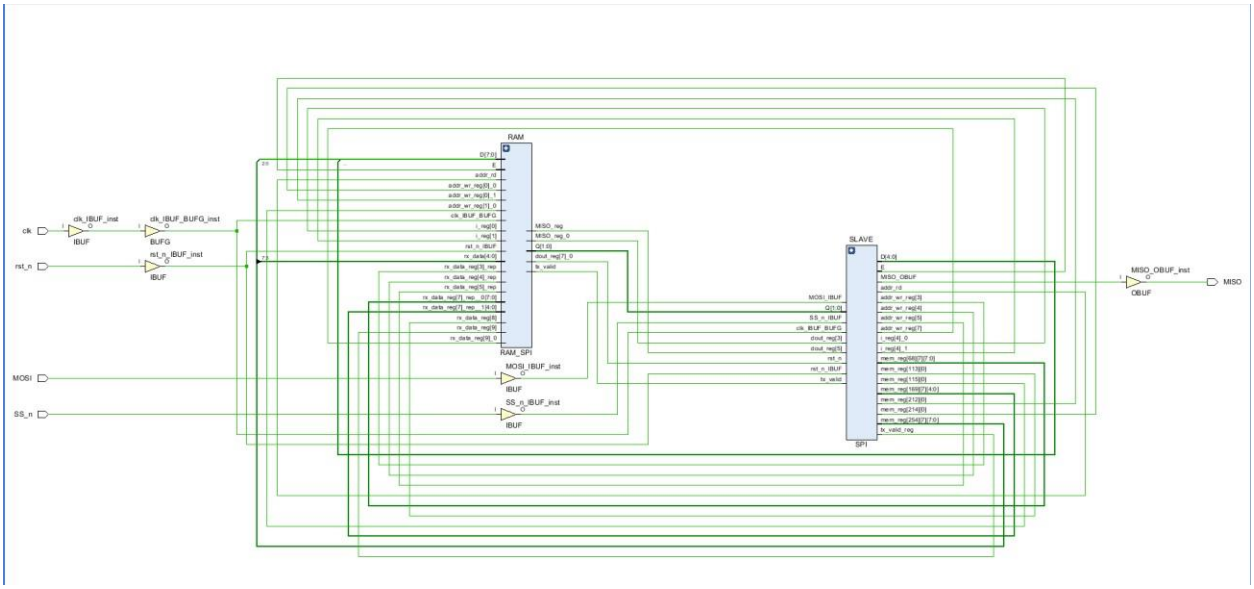


Sequential Encoding

Synthesis

Elaboration and Synthesis Schematics





Synthesis Report

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'
```

Timing Report Snippet

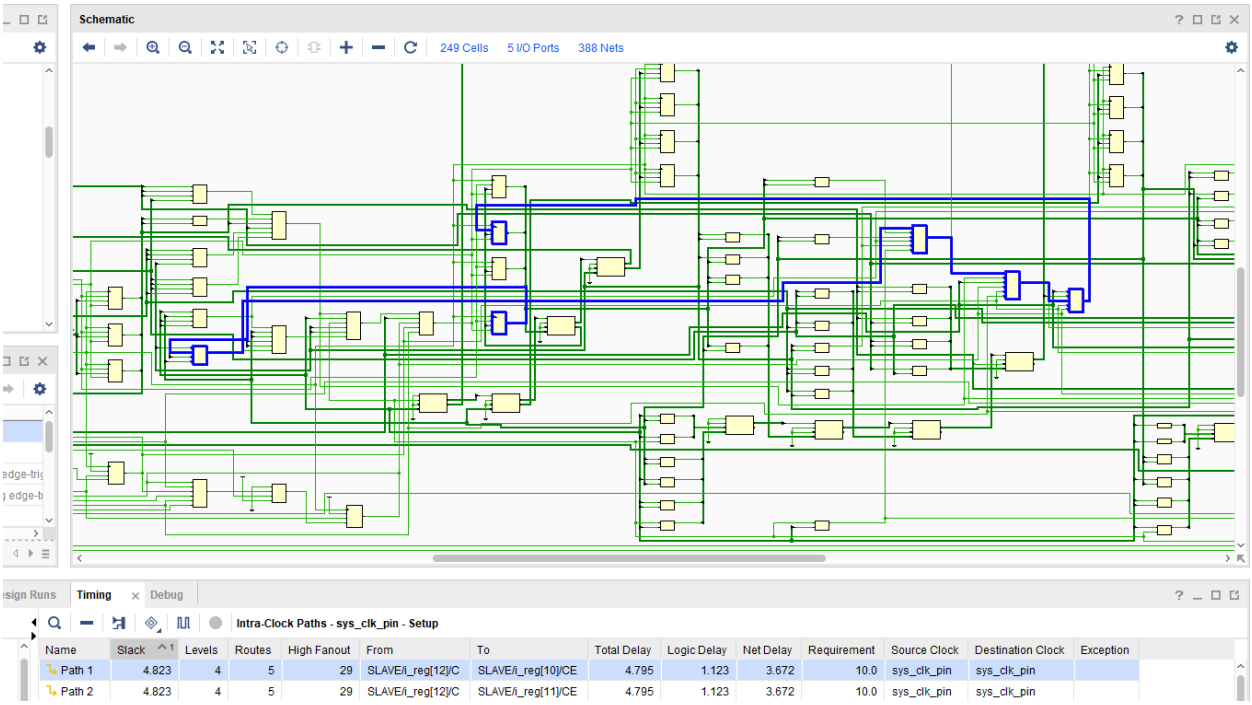
Runs | Timing | Utilization | Debug

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.823 ns	Worst Hold Slack (WHS):	0.145 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4333	Total Number of Endpoints:	4333	Total Number of Endpoints:	2179

All user specified timing constraints are met.

Critical Path Snippet

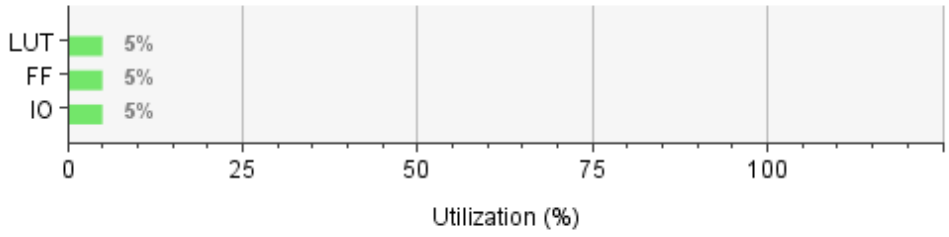


Implementation

Utilization Report

Summary

Resource	Utilization	Available	Utilization %
LUT	945	20800	4.54
FF	2182	41600	5.25
IO	5	106	4.72



Timing Report Snippet

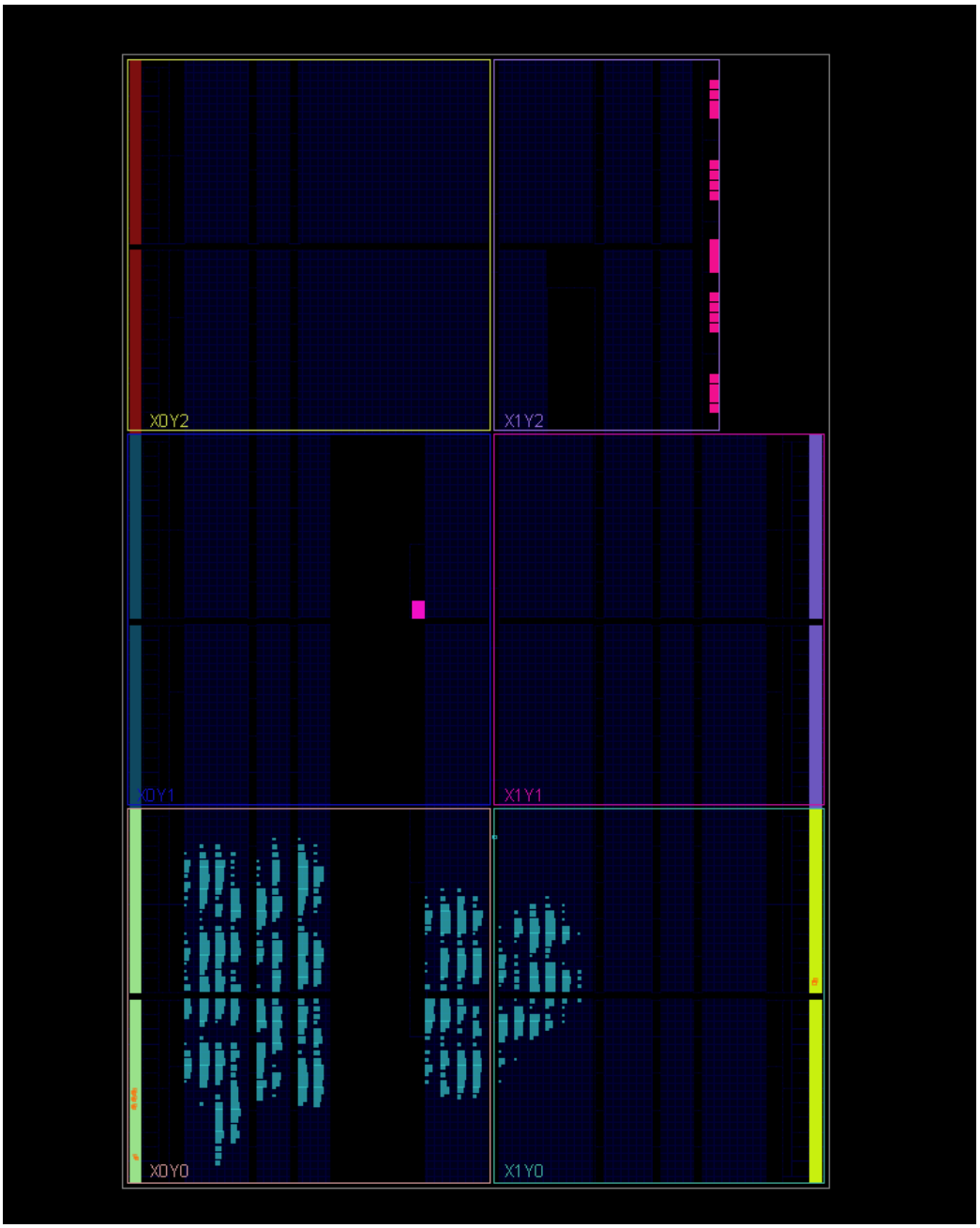
Runs | Timing | Utilization

Design Timing Summary

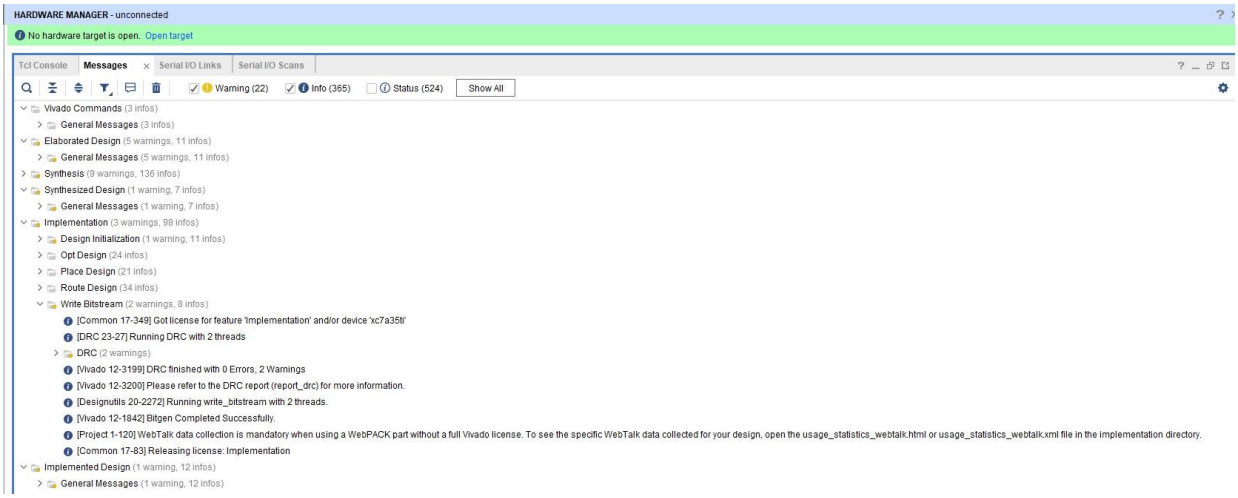
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.545 ns	Worst Hold Slack (WHS):	0.197 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4333	Total Number of Endpoints:	4333	Total Number of Endpoints:	2179

All user specified timing constraints are met.

FPGA Device Snippet



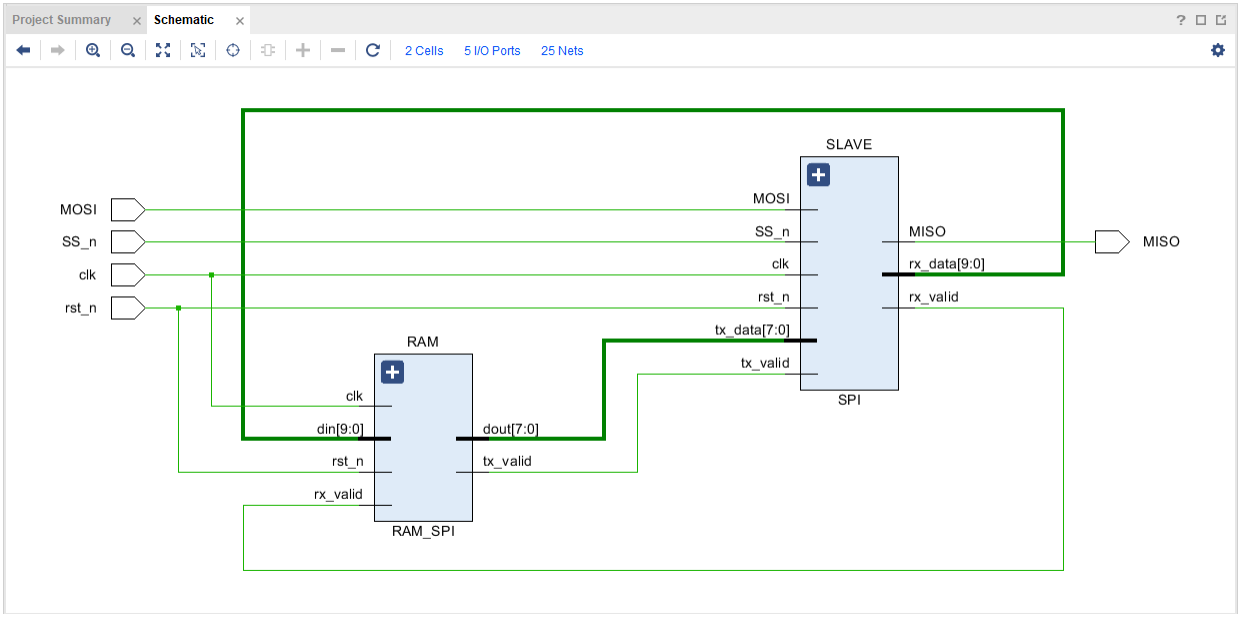
“Messages” Tab

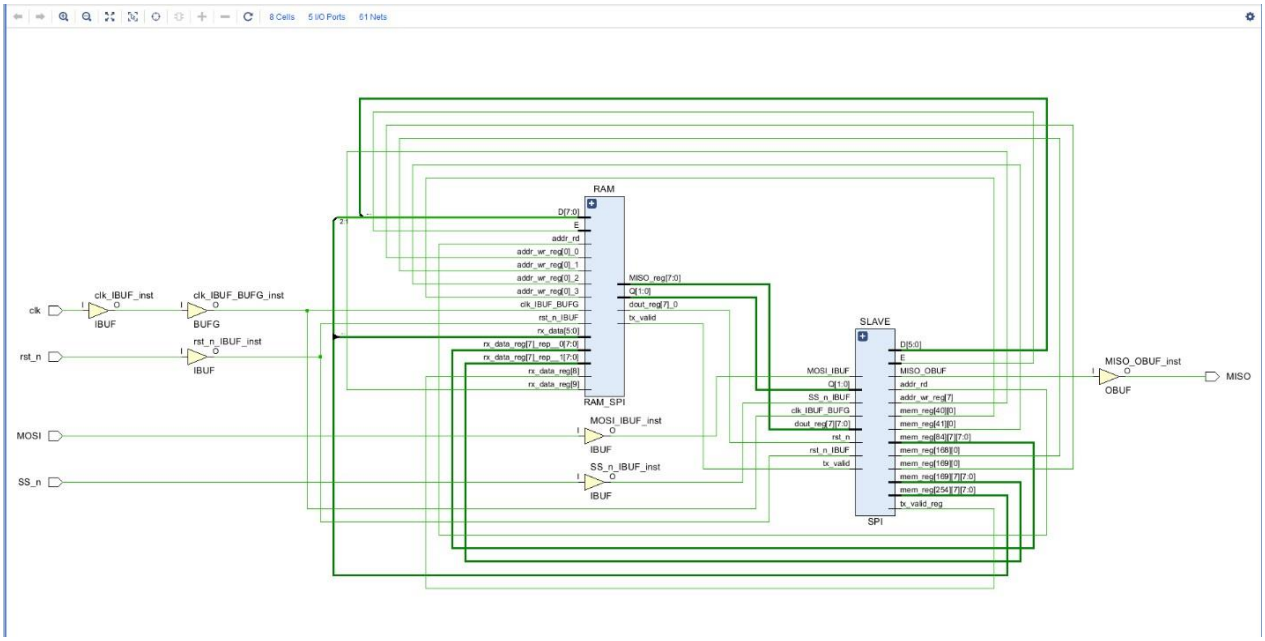


Gray Encoding

Synthesis

Elaboration and Synthesis Schematics





Synthesis Report

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

FO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'

Timing Report Snippet

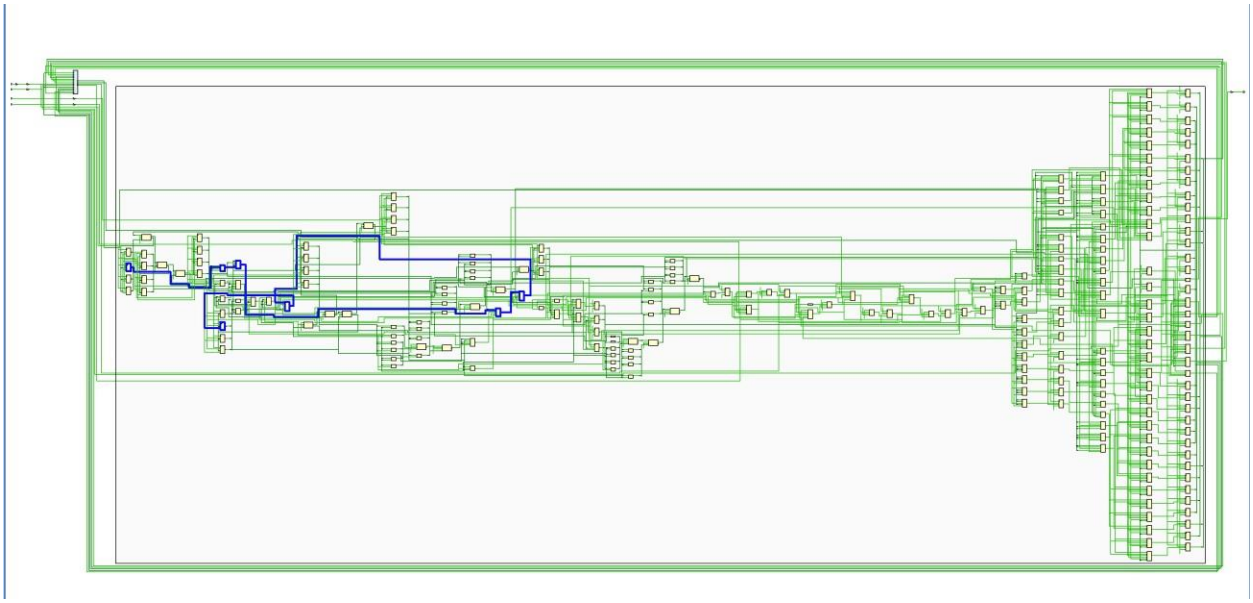
uns | Timing | Utilization | Debug

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.764 ns	Worst Hold Slack (WHS):	0.145 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4334	Total Number of Endpoints:	4334	Total Number of Endpoints:	2180

All user specified timing constraints are met.

Critical Path Snippet



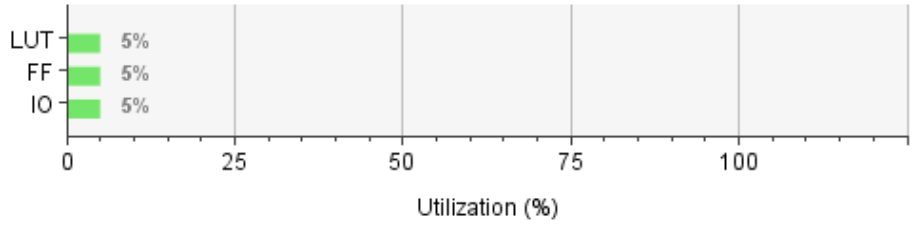
Implementation

Utilization Report

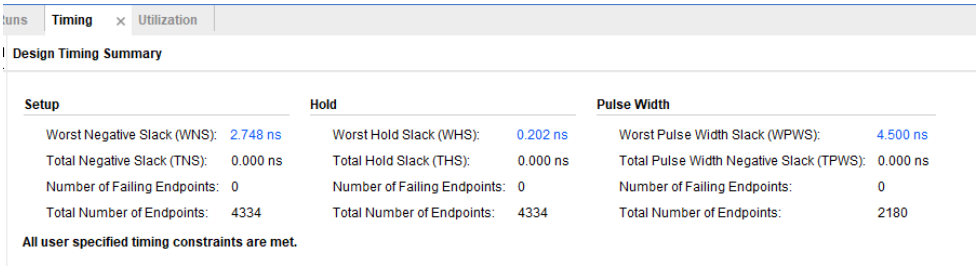
Design Runs | Timing | **Utilization** ×

Summary

Resource	Utilization	Available	Utilization %
LUT	942	20800	4.53
FF	2183	41600	5.25
IO	5	106	4.72



Timing Report Snippet



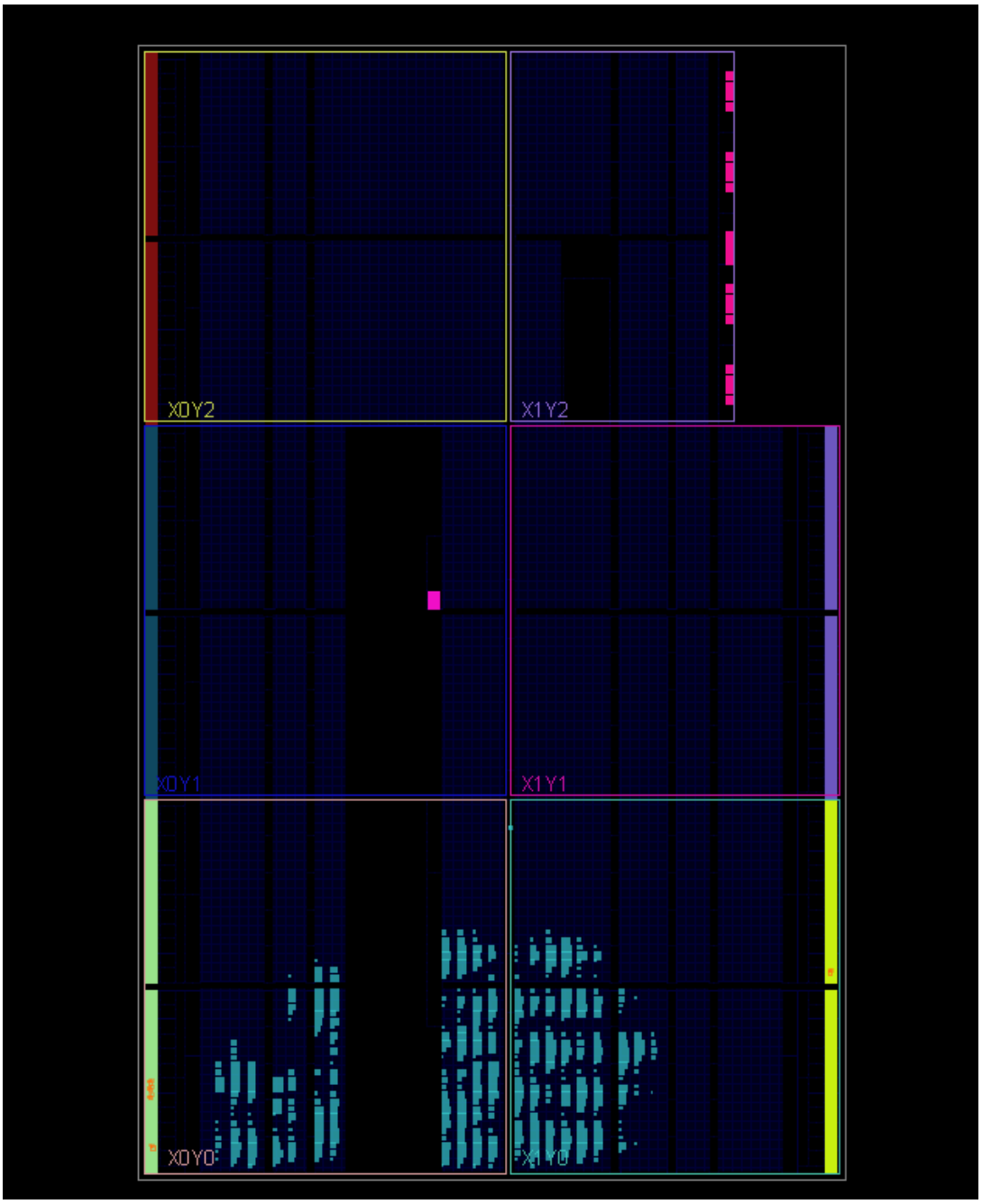
Timing | Utilization

Design Timing Summary

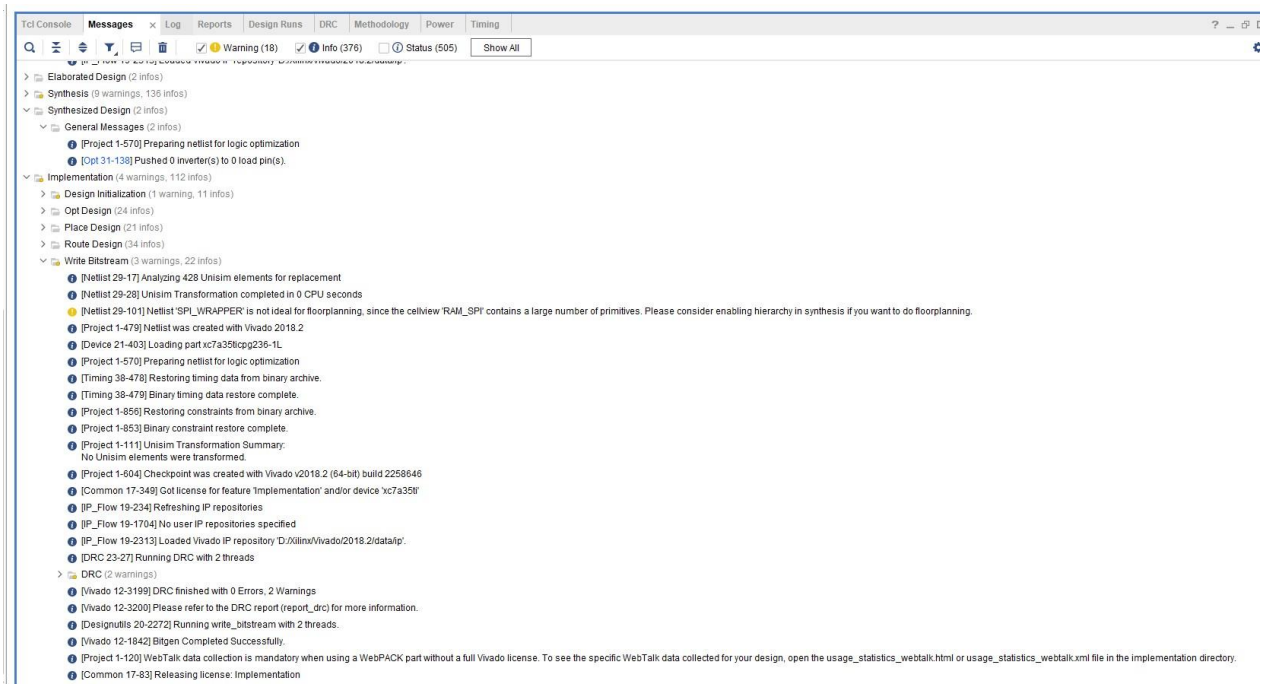
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.748 ns	Worst Hold Slack (WHS):	0.202 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4334	Total Number of Endpoints:	4334	Total Number of Endpoints:	2180

All user specified timing constraints are met.

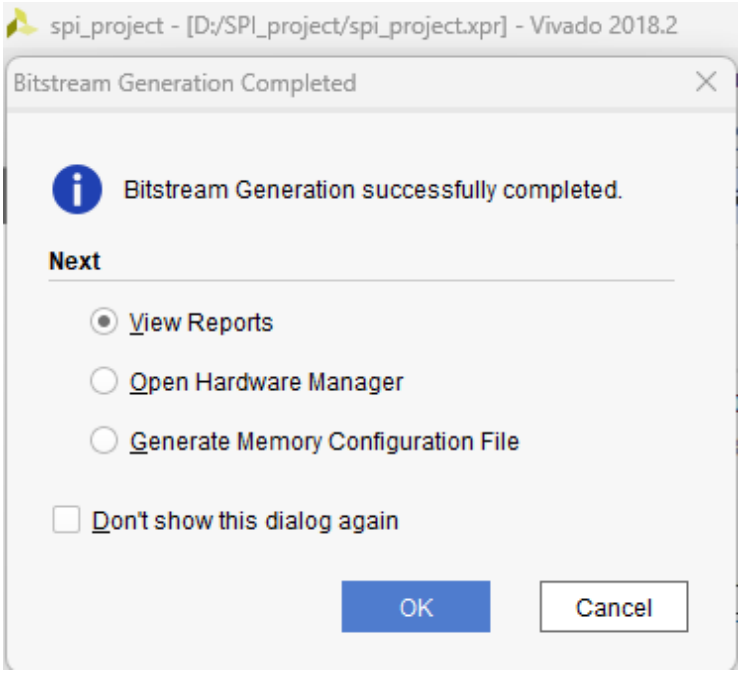
FPGA Device Snippet



“Messages” Tab



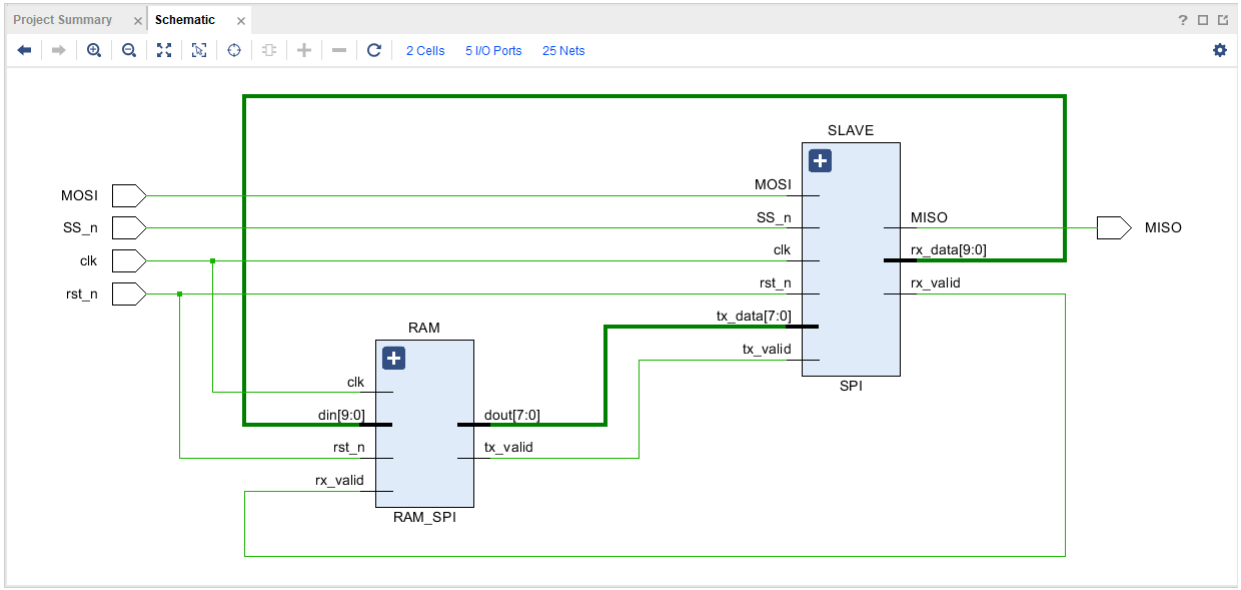
Note: since the gray encoding has the highest setup time slack, we performed the debug core on It and this the bitstream generation success.

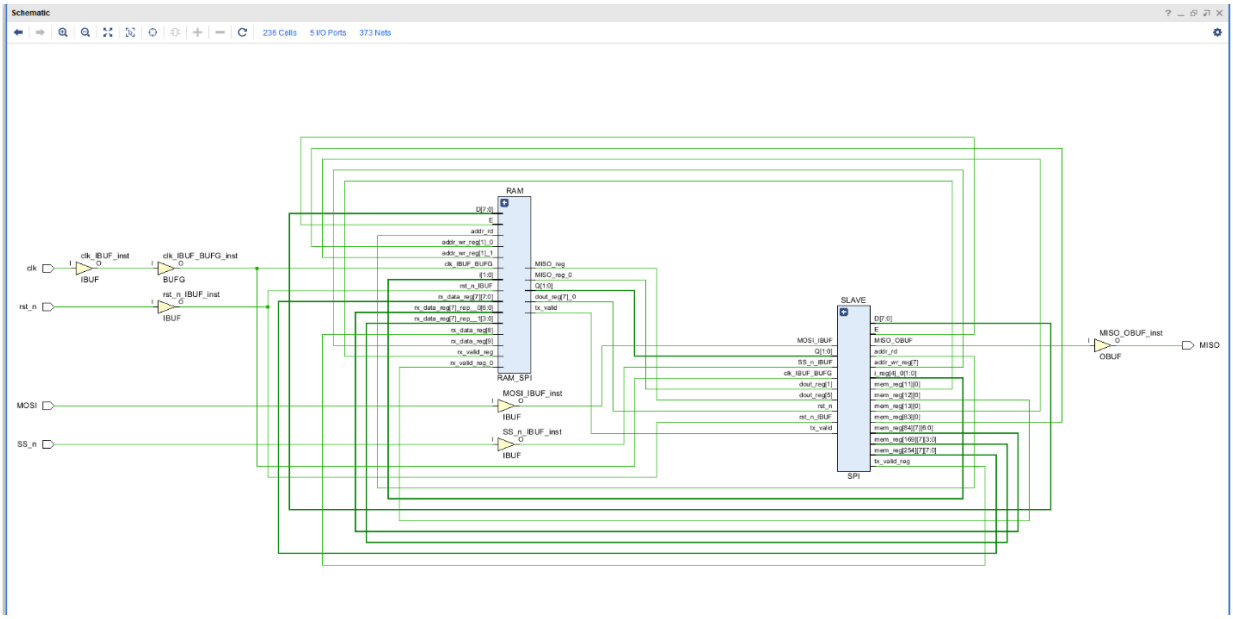


One_Hot Encoding

Synthesis

Elaboration and Synthesis Schematics



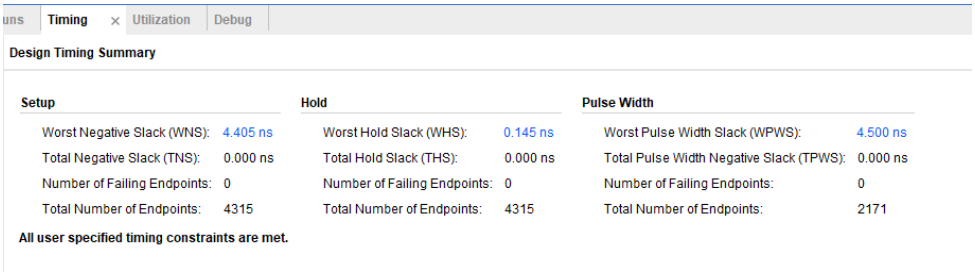


Synthesis Report

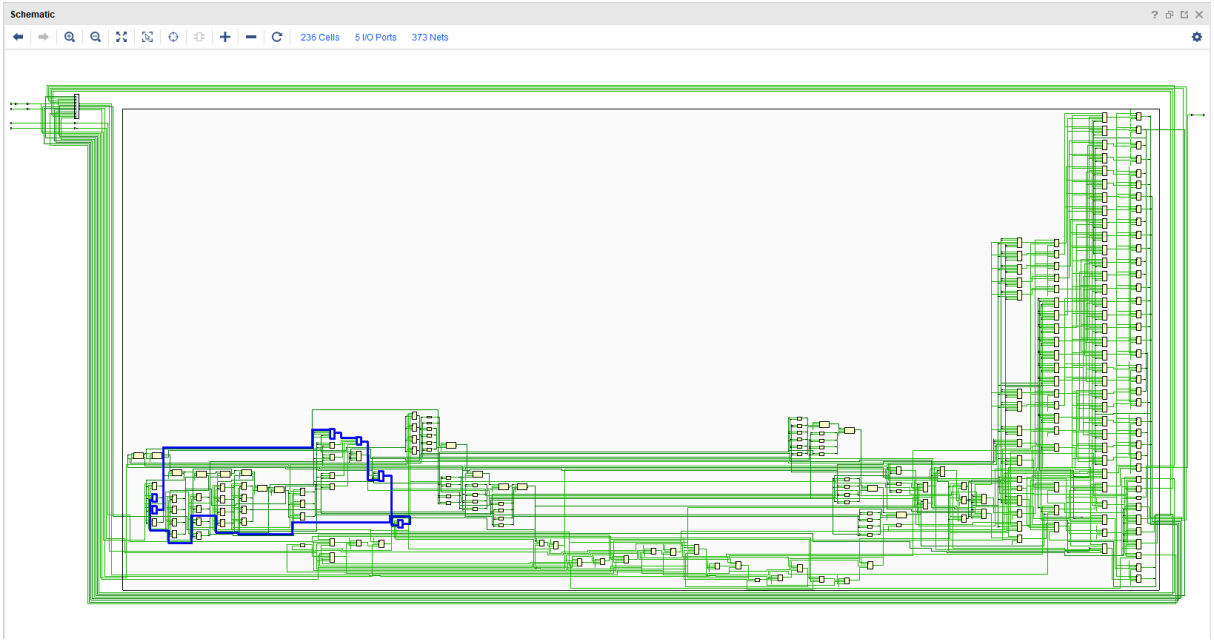
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

FO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'

Timing Report Snippet



Critical Path Snippet

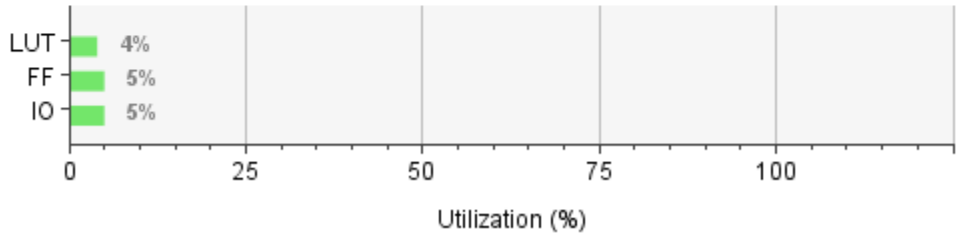


Implementation

Utilization Report

Summary

Resource	Utilization	Available	Utilization %
LUT	933	20800	4.49
FF	2176	41600	5.23
IO	5	106	4.72



Timing Report Snippet

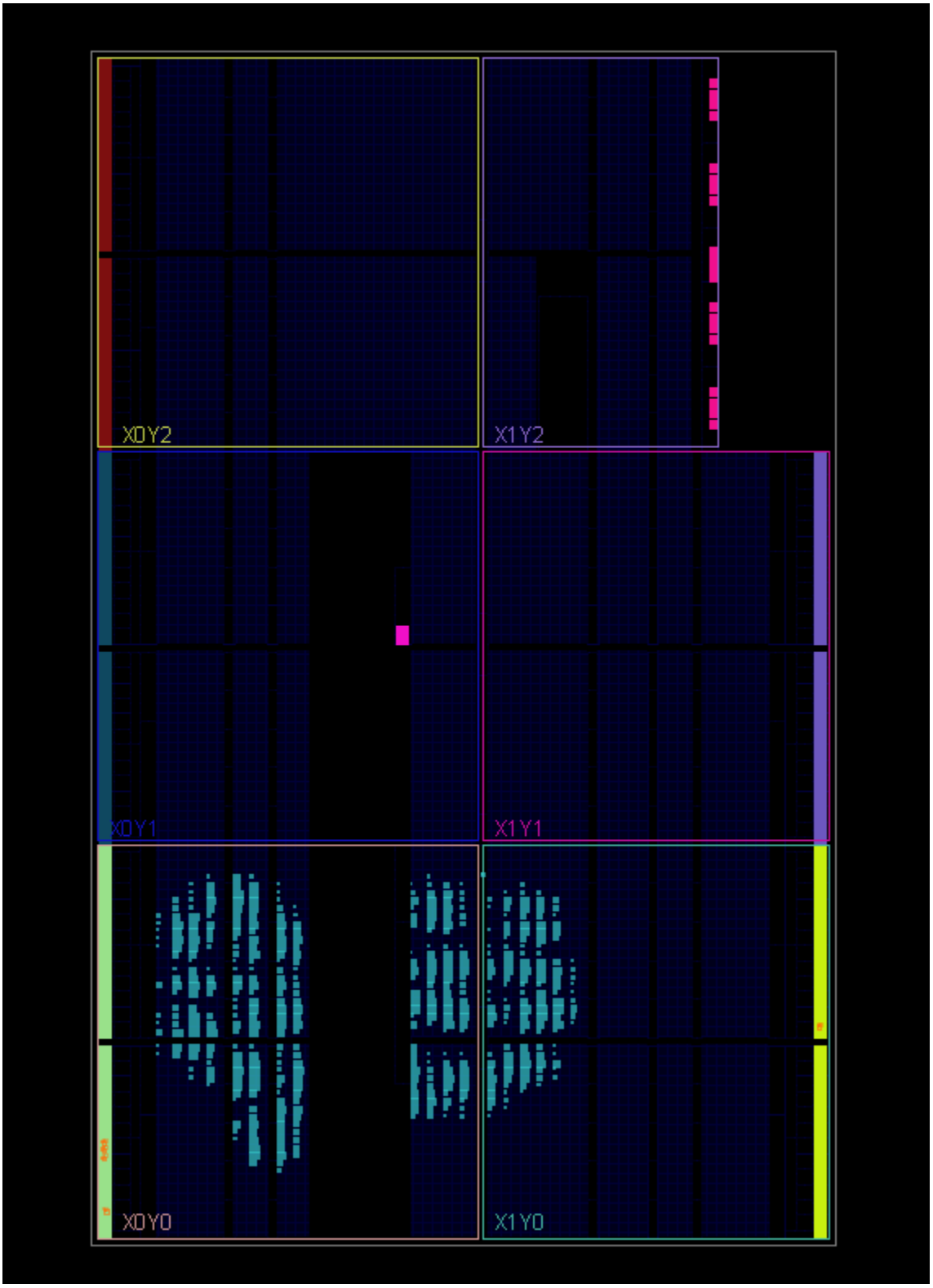
Design Runs | Timing

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.079 ns	Worst Hold Slack (WHS):	0.210 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4315	Total Number of Endpoints:	4315	Total Number of Endpoints:	2171

All user specified timing constraints are met.

FPGA Device Snippet



“Messages” Tab