# Project

# Spartan6 - DSP48A1

# Table of Contents

## *RTL Code*

```
module Spartan6_DSP48A1(A, B, C, D, CLK, CARRYIN, OPMODE, BCIN,
                        RSTA, RSTB, RSTC, RSTD, RSTM, RSTP, RSTCARRYIN, RSTOPMODE,
                        CEA, CEB, CEC, CED, CEM, CEP, CECARRYIN, CEOPMODE, PCIN,
                        BCOUT, PCOUT, M, P,CARRYOUT, CARRYOUTF);

    parameter A0REG=1'b0, A1REG=1'b1, B0REG=1'b0, B1REG=1'b1, CREG=1'b1, DREG=1'b1, MREG=1'b1, PREG=1'b1,
        CARRYINREG=1'b1, CARRYOUTREG=1'b1, OPMODEREG=1'b1, CARRYINSEL="OPMODE5", B_INPUT="DIRECT", RSTTYPE="SYNC";

    input [17:0] A, B, D, BCIN;
    input [47:0] C, PCIN;
    input [7:0] OPMODE;
    input CLK, CARRYIN, RSTA, RSTB, RSTC, RSTD, RSTM,
          RSTP, RSTCARRYIN, RSTOPMODE, CEA, CEB, CEC, CED, CEM, CEP, CECARRYIN, CEOPMODE;
    output [47:0] P, PCOUT;
    output [17:0] BCOUT;
    output [35:0] M;
    output CARRYOUT, CARRYOUTF;

    wire [7:0] OPMODE_MUX;
    wire [17:0] D_MUX, B_MUX0, A_MUX0, Pre_AdderMUX, Pre_AdderOUT, B_IN, A_MUX1, B_MUX1;
    wire [47:0] C_MUX, X_MUX, Z_MUX,M_MUX_extended, Post_AdderOUT, P_MUX;
    wire [35:0] MULT_OUT, M_MUX;
    wire CarryCascade_MUX, CYI_MUX, carryout, CYO_MUX;

    REG_MUX #(18, DREG , RSTTYPE) D_REG(D, CLK, RSTD, CED, D_MUX);
    REG_MUX #(8, OPMODEREG , RSTTYPE) OPMODE_REG(OPMODE, CLK, RSTOPMODE, CEOPMODE, OPMODE_MUX);
    generate
        if (B_INPUT=="DIRECT")
            assign B_IN = B;
        else if(B_INPUT=="CASCADE")
            assign B_IN = BCIN;
        else
            assign B_IN ='b0;
    endgenerate

    REG_MUX #(18, B0REG, RSTTYPE) B0_REG(B_IN, CLK, RSTB, CEB, B_MUX0);
    REG_MUX #(18, A0REG, RSTTYPE) A0_REG(A, CLK, RSTA, CEA, A_MUX0);
    REG_MUX #(48, CREG, RSTTYPE) C_REG(C, CLK, RSTC, CEC, C_MUX);
    MUX2x1 Adder1MUX(B_MUX0, Pre_AdderOUT, OPMODE_MUX[4], Pre_AdderMUX);
    REG_MUX #(18, B1REG, RSTTYPE) B1_REG(Pre_AdderMUX, CLK, RSTB, CEB, B_MUX1);
    REG_MUX #(18, A1REG, RSTTYPE) A1_REG(A_MUX0, CLK, RSTA, CEA, A_MUX1);
    REG_MUX #(36, MREG, RSTTYPE) M_REG(MULT_OUT, CLK, RSTM, CEM, M_MUX);
    generate
        if (CARRYINSEL=="OPMODE5")
            assign CarryCascade_MUX= OPMODE_MUX[5];
        else if(CARRYINSEL=="CARRYIN")
            assign CarryCascade_MUX = CARRYIN;
        else
            assign CarryCascade_MUX ='b0;
    endgenerate
    REG_MUX #(1, CARRYINREG, RSTTYPE) CYI(CarryCascade_MUX, CLK, RSTCARRYIN, CECARRYIN, CYI_MUX);
    assign M_MUX_extended = { {12 {M_MUX[35]} }, M_MUX };
    MUX4x1 X('b0, M_MUX_extended, P_MUX, {D[11:0], A, B}, OPMODE_MUX[1:0], X_MUX);
    MUX4x1 Z('b0, PCIN, P_MUX, C_MUX, OPMODE_MUX[3:2], Z_MUX);
    REG_MUX #(48, PREG, RSTTYPE) P_REG(Post_AdderOUT, CLK, RSTP, CEP, P_MUX);
    REG_MUX #(1, CARRYOUTREG, RSTTYPE) CYO(carryout, CLK, RSTCARRYIN, CECARRYIN, CYO_MUX);

    adder_subtracter Pre_adder_sub (D_MUX,B_MUX0,0,OPMODE_MUX[6],Pre_AdderOUT);
    adder_subtracter #(48) Post_adder_sub (Z_MUX,X_MUX,CYI_MUX,OPMODE_MUX[7],Post_AdderOUT,carryout);

    assign MULT_OUT = A_MUX1 * B_MUX1;
    assign BCOUT = B_MUX1;
    assign M = M_MUX;
    assign CARRYOUT = CYO_MUX;
    assign CARRYOUTF = CYO_MUX;
    assign P = P_MUX;
    assign PCOUT = P_MUX;
    endmodule
```

```verilog
module adder_subtracter(A,B,cin,operation,result,carryout);
parameter DATA_WIDTH = 18;
input [DATA_WIDTH-1:0] A,B;
input cin,operation;
output [DATA_WIDTH-1:0] result;
output carryout;

assign {carryout,result} = (operation)? (A-(B+cin)) : (A+(B+cin))  ;

endmodule
```

```verilog
module MUX2x1(in0, in1, sel, out);
    parameter WIDTH = 18;
    input [WIDTH-1:0] in0, in1;
    input sel;
    output [WIDTH-1:0] out;
    assign out = (sel == 0)? in0 : in1;
endmodule
```

```verilog
module MUX4x1(in0, in1, in2, in3, sel, out);
    input [47:0] in0, in1, in2, in3;
    input [1:0] sel;
    output [47:0] out;
    assign out = (sel == 0)? in0 : (sel == 1)? in1 : (sel == 2)? in2 : in3;
endmodule
```

```verilog
module REG_MUX(in, clk, rst, en, out);
    parameter REG_WIDTH =18, REG_SEL=1, RST_TYPE="SYNC";
    input [REG_WIDTH-1:0] in;
    input rst, clk, en;
    output [REG_WIDTH-1:0] out;

    generate
        if (REG_SEL)
            Register #(.REG_WIDTH(REG_WIDTH), .RST_TYPE(RST_TYPE)) REG(in, rst, clk, en, out);
        else
            assign out = in;
    endgenerate
endmodule
```

```
module Register(in, rst, clk, en, out);
    parameter REG_WIDTH =18;
    parameter RST_TYPE ="SYNC";

    input [REG_WIDTH-1:0] in;
    input rst, clk, en;
    output reg [REG_WIDTH-1:0] out;

    generate
        if (RST_TYPE == "SYNC") begin
            always @(posedge clk ) begin
                if (rst) begin
                    out <= 'b0;
                end
                else if(en)
                    out <= in;
            end
        end
        else if(RST_TYPE == "ASYNC") begin
            always @(posedge clk or posedge rst) begin
                if (rst) begin
                    out <= 'b0;
                end
                else if(en)
                    out <= in;
            end
        end
    endgenerate
endmodule
```

## *Testbench Code*

```
module DSP_48A1_tb();

parameter A0REG=1'b0, A1REG=1'b1, B0REG=1'b0, B1REG=1'b1, CREG=1'b1, DREG=1'b1, MREG=1'b1, PREG=1'b1,
        CARRYINREG=1'b1, CARRYOUTREG=1'b1, OPMODEREG=1'b1, CARRYINSEL="OPMODE5", B_INPUT="DIRECT", RSTTYPE="SYNC";
reg [17:0] A,B,D,BCIN;
reg [47:0] C;
reg clk,RSTA,RSTB,RSTC,RSTD,RSTOPMODE,RSTM,RST_CARRYIN,RSTP;
reg CEA,CEB,CED,CEC,CE_OPMODE,CEM,CE_CARRYIN,CEP;
reg CARRYIN;
reg [47:0] PCIN;
reg [7:0] opmode;
wire [17:0] BCOUT;
wire [35:0] M;
wire [47:0] P,PCOUT;
wire CARRYOUT,CARRYOUTF;
Spartan6_DSP48A1 dut(A, B, C, D, clk, CARRYIN, opmode, BCIN,
                     RSTA, RSTB, RSTC, RSTD, RSTM, RSTP, RST_CARRYIN, RSTOPMODE,
                     CEA, CEB, CEC, CED, CEM, CEP, CE_CARRYIN, CE_OPMODE, PCIN,
                     BCOUT, PCOUT, M, P,CARRYOUT, CARRYOUTF);


initial begin
    clk=0;
    forever begin
        #2  clk=~clk;
    end
end
initial begin
    RSTB=1;
    RSTD=1;
    #50;
    repeat (20) begin
        D=$random;
        B=$random;
        @(negedge clk);
    end
    RSTB=0;
```

```
    RSTD=0;
    RSTA=0;
    RSTC=0;
    RSTOPMODE=0;
    RSTM=0;
    RST_CARRYIN=0;
    RSTP=0;
    CEB=1;
    CED=1;
    CEA=1;
    CEC=1;
    CE_OPMODE=1;
    CEM=1;
    CE_CARRYIN=1;
    CEP=1;
    #2;
    repeat (20) begin
        A=5;
        C=60;
        D=7;
        B=2;
        BCIN=11;
        opmode[6]=0;
        opmode[4]=1;
        CARRYIN=0;
        PCIN='b0;
        opmode[1:0]=2'b01;
        opmode[3:2]=2'b11;
        opmode[5]=1'b1;
        opmode[7]=1;
        @(negedge clk);
    end
    #2;
    RSTB=1;
    RSTD=1;
    RSTA=1;
    RSTC=1;
```

```
    RSTOPMODE=1;
    RSTM=1;
    RST_CARRYIN=1;
    RSTP=1;
    #2;
    RSTB=0;
    RSTD=0;
    RSTA=0;
    RSTC=0;
    RSTOPMODE=0;
    RSTM=0;
    RST_CARRYIN=0;
    RSTP=0;
    #2;
    repeat (20) begin
        A=5;
        C=3;
        D=7;
        B=2;
        BCIN=11;
        opmode[6]=1;
        opmode[4]=1;
        CARRYIN=0;
        PCIN=0;
        opmode[1:0]=2'b01;
        opmode[3:2]=2'b11;
        opmode[5]=1'b0;
        opmode[7]=0;
        @(negedge clk);
    end
    #2;
    RSTB=1;
    RSTD=1;
    RSTA=1;
    RSTC=1;
    RSTOPMODE=1;
    RSTM=1;
```

```
112     RST_CARRYIN=1;
113     RSTP=1;
114     #2;
115     RSTB=0;
116     RSTD=0;
117     RSTA=0;
118     RSTC=0;
119     RSTOPMODE=0;
120     RSTM=0;
121     RST_CARRYIN=0;
122     RSTP=0;
123     #2;
124     repeat (20) begin
125         A=5;
126         C=60;
127         D=7;
128         B=2;
129         BCIN=11;
130         opmode[6]=0;
131         opmode[4]=1;
132         CARRYIN=0;
133         PCIN=0;
134         opmode[1:0]=2'b01;
135         opmode[3:2]=2'b11;
136         opmode[5]=1'b1;
137         opmode[7]=0;
138         @(negedge clk);
139     end
140     #2;
141     RSTB=1;
142     RSTD=1;
143     RSTA=1;
144     RSTC=1;
145     RSTOPMODE=1;
146     RSTM=1;
147     RST_CARRYIN=1;
148     RSTP=1;
```

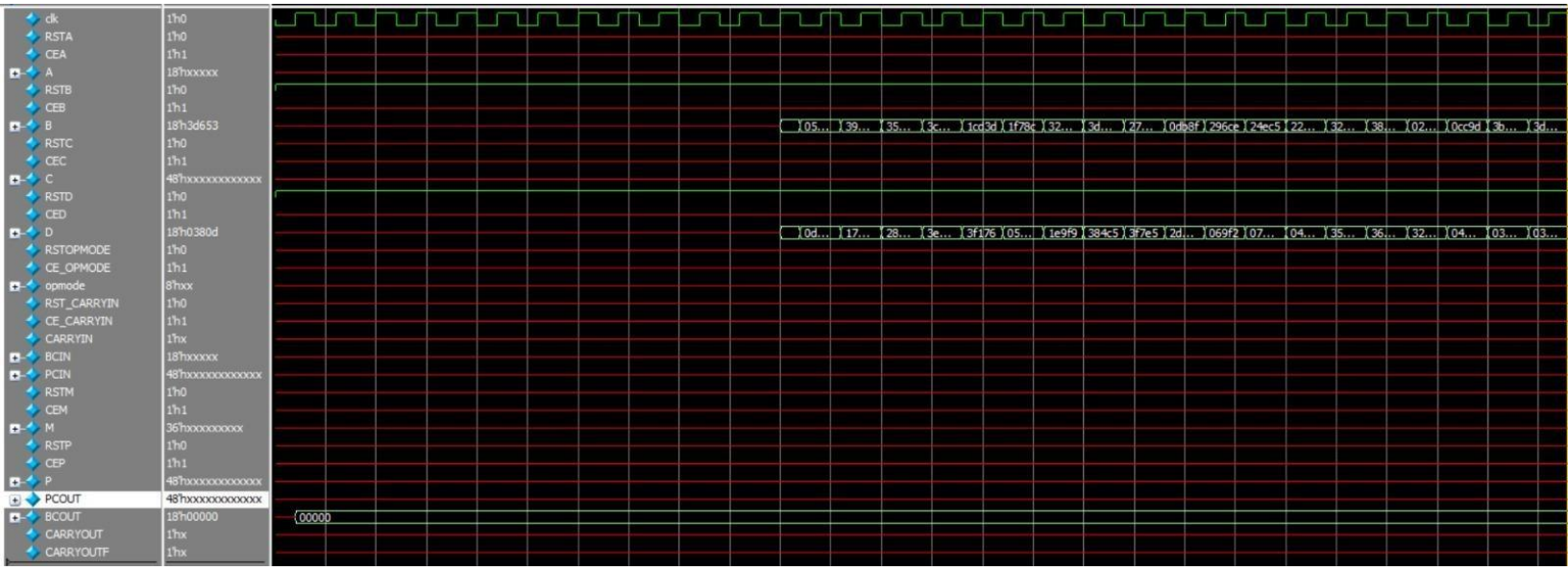
```
149     #2;
150     RSTB=0;
151     RSTD=0;
152     RSTA=0;
153     RSTC=0;
154     RSTOPMODE=0;
155     RSTM=0;
156     RST_CARRYIN=0;
157     RSTP=0;
158     #2;
159     repeat (20) begin
160         A=5;
161         C=60;
162         D=7;
163         B=2;
164         BCIN=11;
165         opmode[6]=1;
166         opmode[4]=1;
167         CARRYIN=0;
168         PCIN=0;
169         opmode[1:0]=2'b01;
170         opmode[3:2]=2'b11;
171         opmode[5]=1'b0;
172         opmode[7]=1;
173         @(negedge clk);
174     end
175     #2;
176     RSTB=1;
177     RSTD=1;
178     RSTA=1;
179     RSTC=1;
180     RSTOPMODE=1;
181     RSTM=1;
182     RST_CARRYIN=1;
183     RSTP=1;
184     #2;
185     RSTB=0;
```

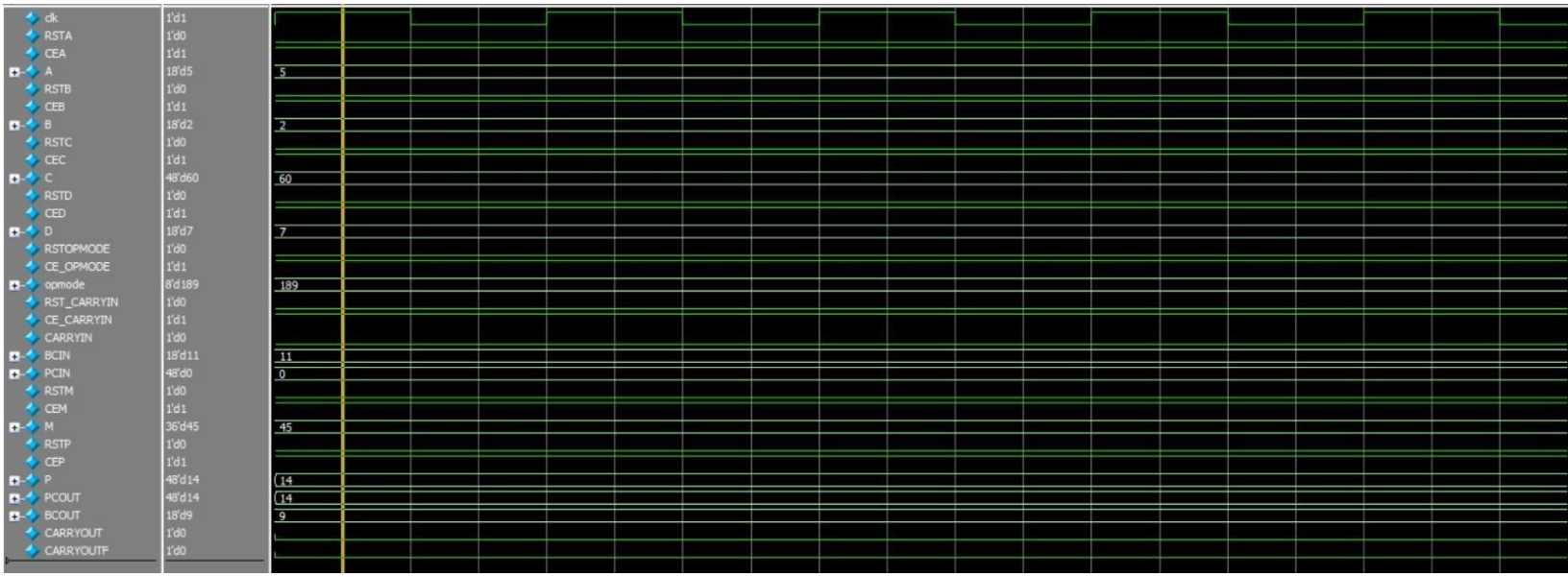
```
185         RSTB=0;
186         RSTD=0;
187         RSTA=0;
188         RSTC=0;
189         RSTOPMODE=0;
190         RSTM=0;
191         RST_CARRYIN=0;
192         RSTP=0;
193         #2;
194         repeat (30) begin
195             A=5;
196             C=60;
197             D=7;
198             B=2;
199             BCIN=11;
200             opmode[6]=1;
201             opmode[4]=0;
202             CARRYIN=0;
203             PCIN=0;
204             opmode[1:0]=$random;
205             opmode[3:2]=$urandom_range(0,2);
206             opmode[5]=1'b0;
207             opmode[7]=1;
208             @(negedge clk);
209         end
210         #2 $stop;
211     end
212     endmodule
```

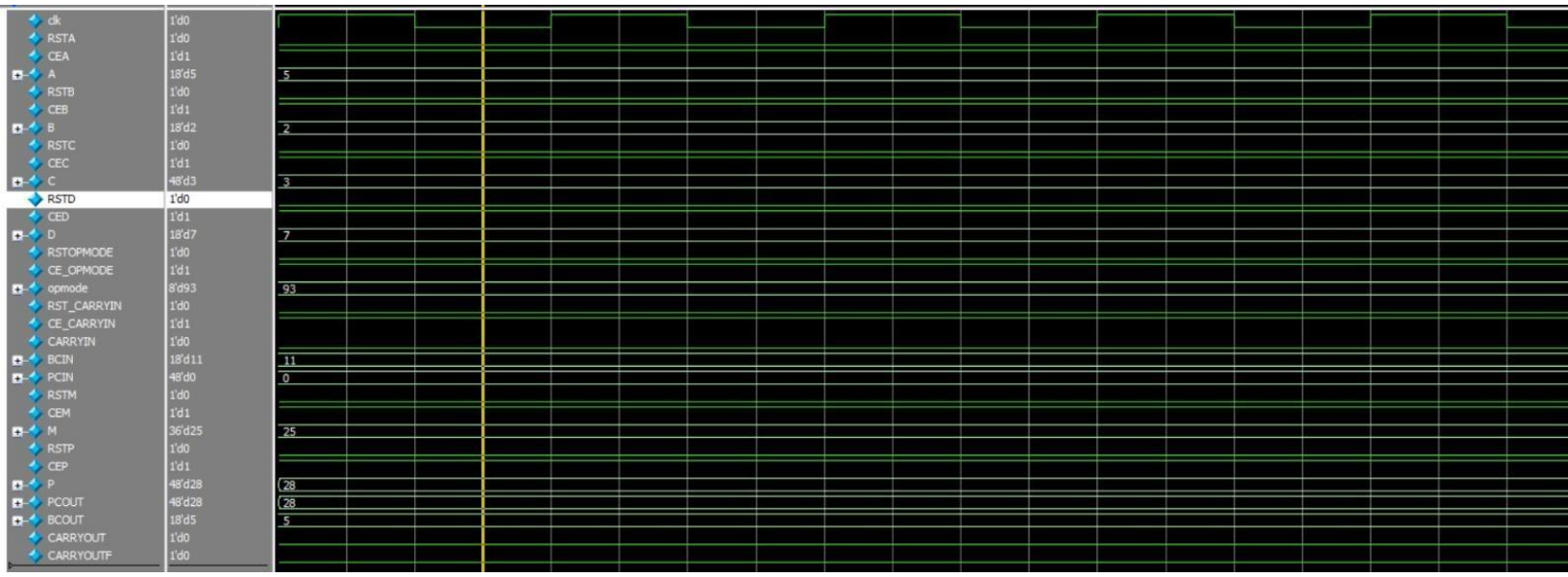
*Do File*

```
1 vlib work
2 vlog adder_sub.v REG_MUX.v Register.v MUX4x1.v MUX2x1.v Spartan6_DSP48A1.v DSP_48A1_tb.v
3 vsim -voptargs=+acc work.DSP_48A1_tb
4 add wave *
5 run -all
```

*QuestaSim Snippets*




clk 1'd0
RSTA 1'd0
CEA 1'd1
A 18'd5
RSTB 1'd0
CEB 1'd1
B 18'd2
RSTC 1'd0
CEC 1'd1
C 48'd3
RSTD 1'd0
CED 1'd1
D 18'd7
RSTOPMODE 1'd0
CE_OPMODE 1'd1
opmode 8'd93
RST_CARRYIN 1'd0
CE_CARRYIN 1'd1
CARRYIN 1'd0
BCIN 18'd11
PCIN 48'd0
RSTM 1'd0
CEM 1'd1
M 36'd25
RSTP 1'd0
CEP 1'd1
P 48'd28
PCOUT 48'd28
BCOUT 18'd5
CARRYOUT 1'd0
CARRYOUTF 1'd0
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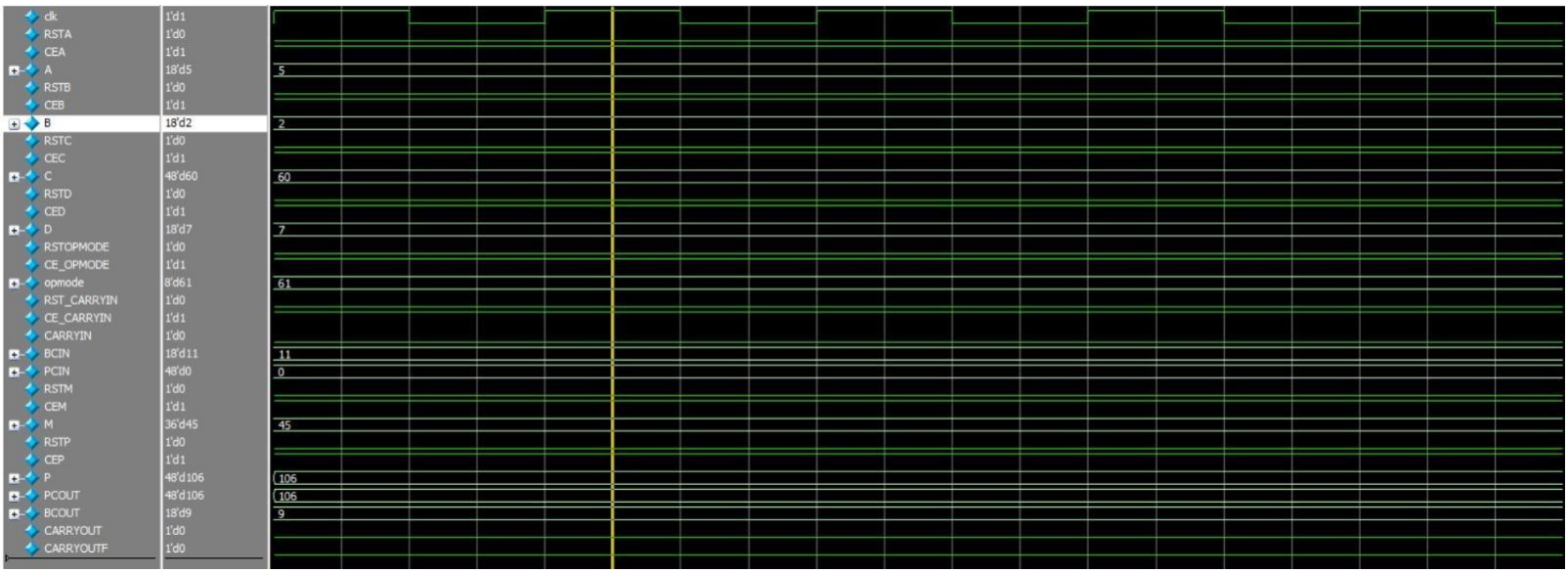
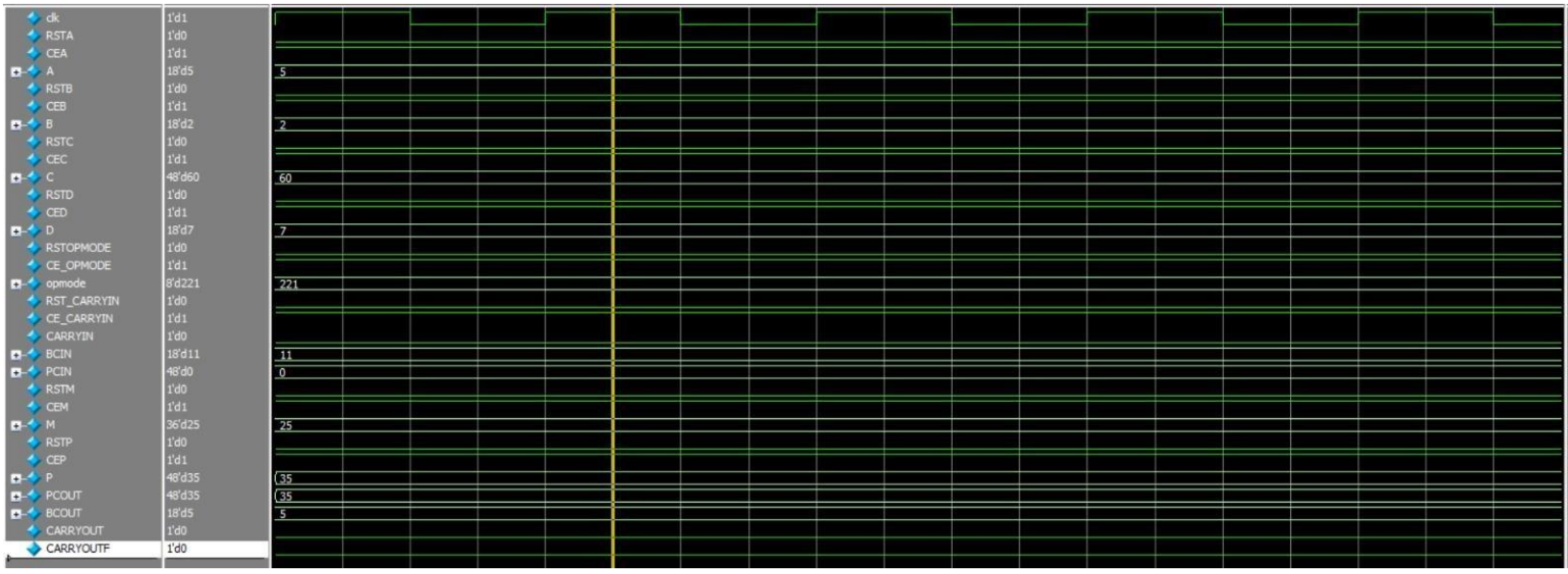
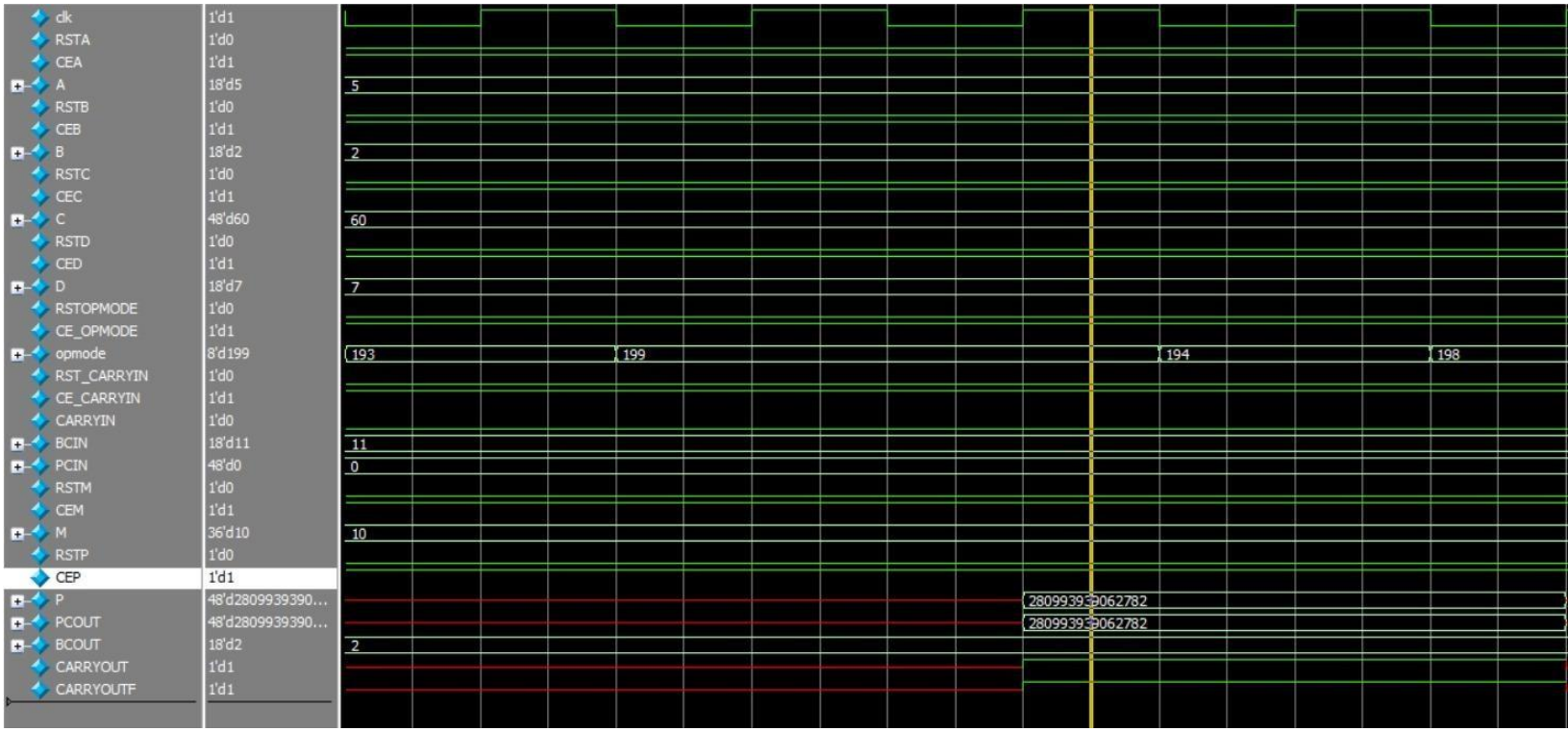
2
3
7
93
11
0
25
28
28
5

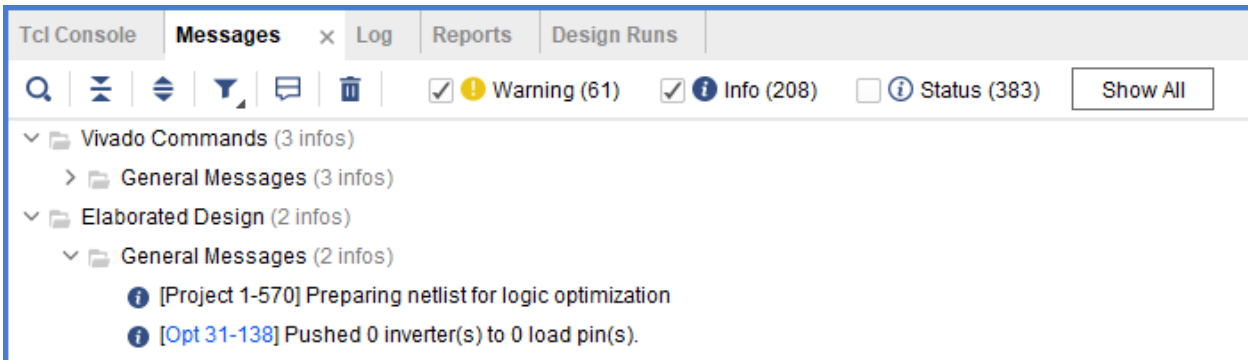

clk 1'd1
RSTA 1'd0
CEA 1'd1
A 18'd5
RSTB 1'd0
CEB 1'd1
B 18'd2
RSTC 1'd0
CEC 1'd1
C 48'd60
RSTD 1'd0
CED 1'd1
D 18'd7
RSTOPMODE 1'd0
CE_OPMODE 1'd1
opmode 8'd61
RST_CARRYIN 1'd0
CE_CARRYIN 1'd1
CARRYIN 1'd0
BCIN 18'd11
PCIN 48'd0
RSTM 1'd0
CEM 1'd1
M 36'd45
RSTP 1'd0
CEP 1'd1
P 48'd106
PCOUT 48'd106
BCOUT 18'd9
CARRYOUT 1'd0
CARRYOUTF 1'd0
5
2
60
7
61
11
0
45
106
106
9


clk 1'd1
RSTA 1'd0
CEA 1'd1
A 18'd5
RSTB 1'd0
CEB 1'd1
B 18'd2
RSTC 1'd0
CEC 1'd1
C 48'd60
RSTD 1'd0
CED 1'd1
D 18'd7
RSTOPMODE 1'd0
CE_OPMODE 1'd1
opmode 8'd221
RST_CARRYIN 1'd0
CE_CARRYIN 1'd1
CARRYIN 1'd0
BCIN 18'd11
PCIN 48'd0
RSTM 1'd0
CEM 1'd1
M 36'd25
RSTP 1'd0
CEP 1'd1
P 48'd35
PCOUT 48'd35
BCOUT 18'd5
CARRYOUT 1'd0
CARRYOUTF 1'd0

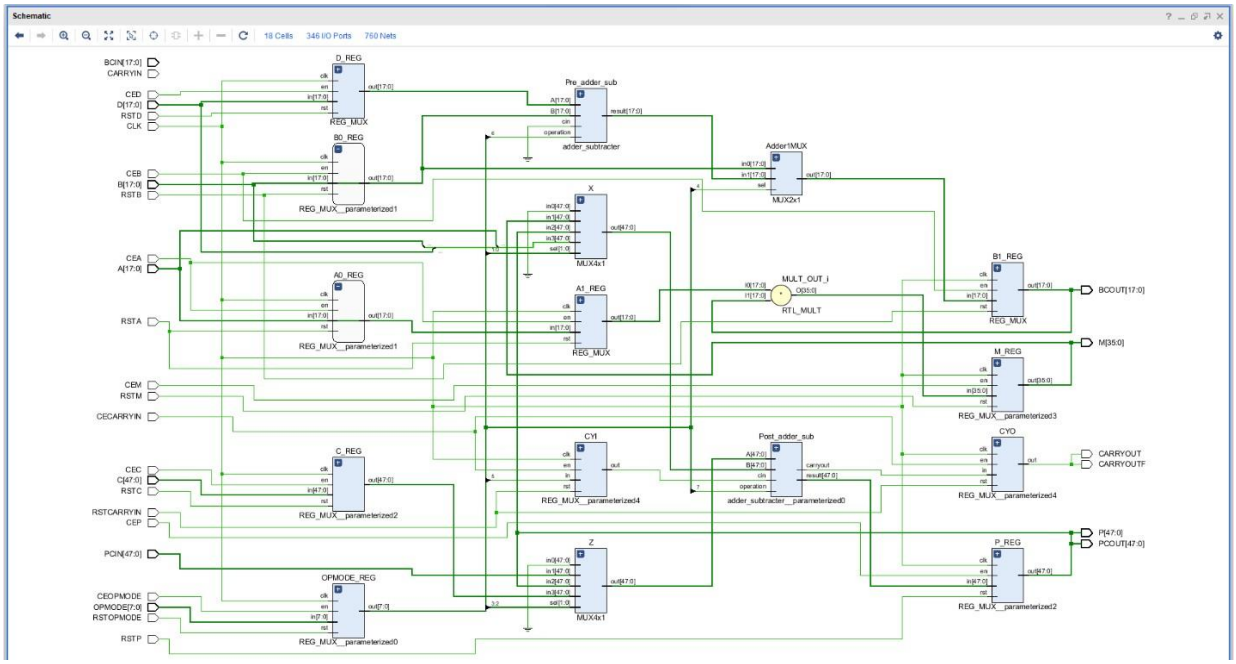

clk 1'd1
RSTA 1'd0
CEA 1'd1
A 18'd5
RSTB 1'd0
CEB 1'd1
B 18'd2
RSTC 1'd0
CEC 1'd1
C 48'd60
RSTD 1'd0
CED 1'd1
D 18'd7
RSTOPMODE 1'd0
CE_OPMODE 1'd1
opmode 8'd199
RST_CARRYIN 1'd0
CE_CARRYIN 1'd1
CARRYIN 1'd0
BCIN 18'd11
PCIN 48'd0
RSTM 1'd0
CEM 1'd1
M 36'd10
RSTP 1'd0
CEP 1'd1
P 48'd2809939390...
PCOUT 48'd2809939390...
BCOUT 18'd2
CARRYOUT 1'd1
CARRYOUTF 1'd1
193
199
194
198
2809939062782
2809939062782

## *Elaboration*

"Messages" tab

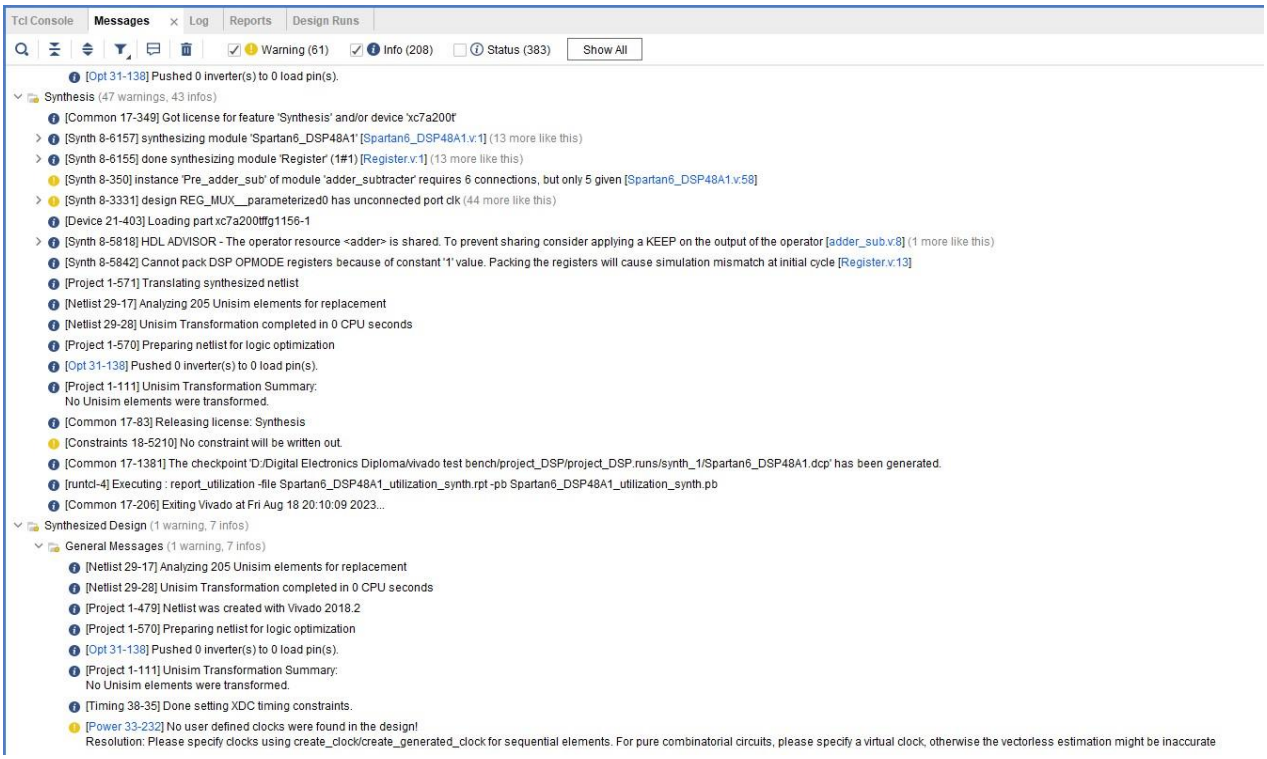



Schematic Snippets

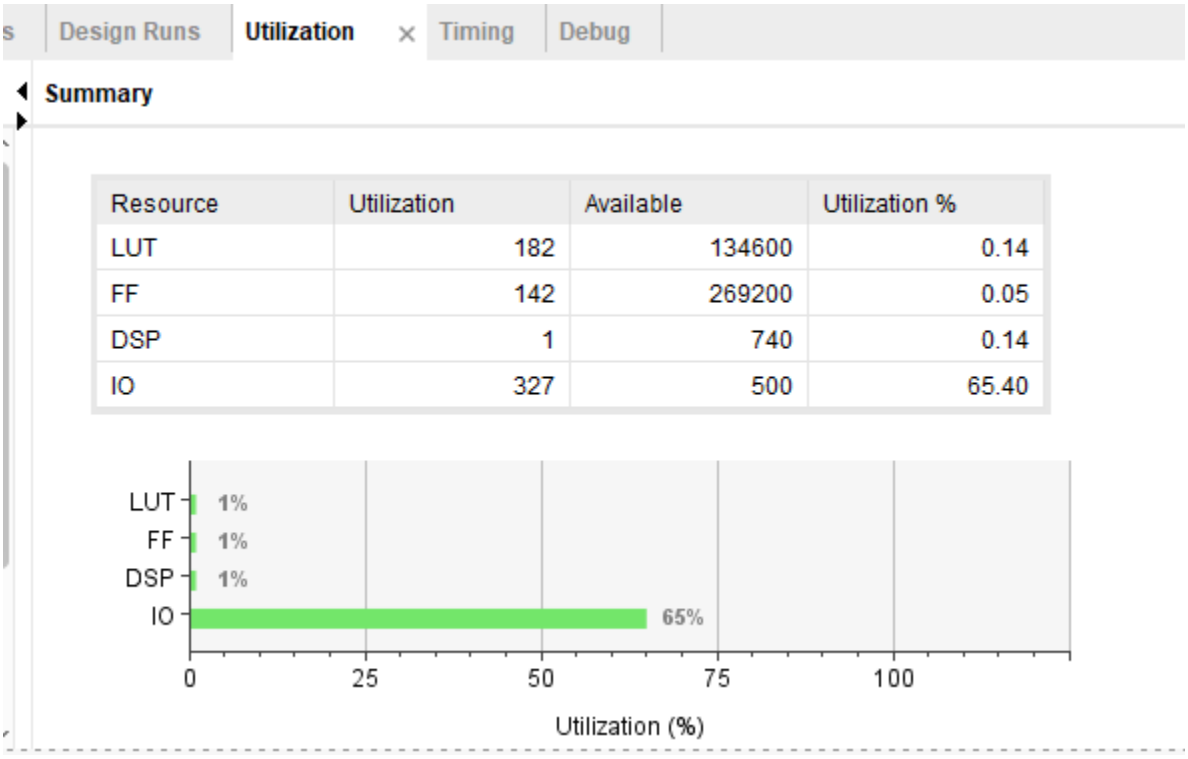


# *Synthesis*

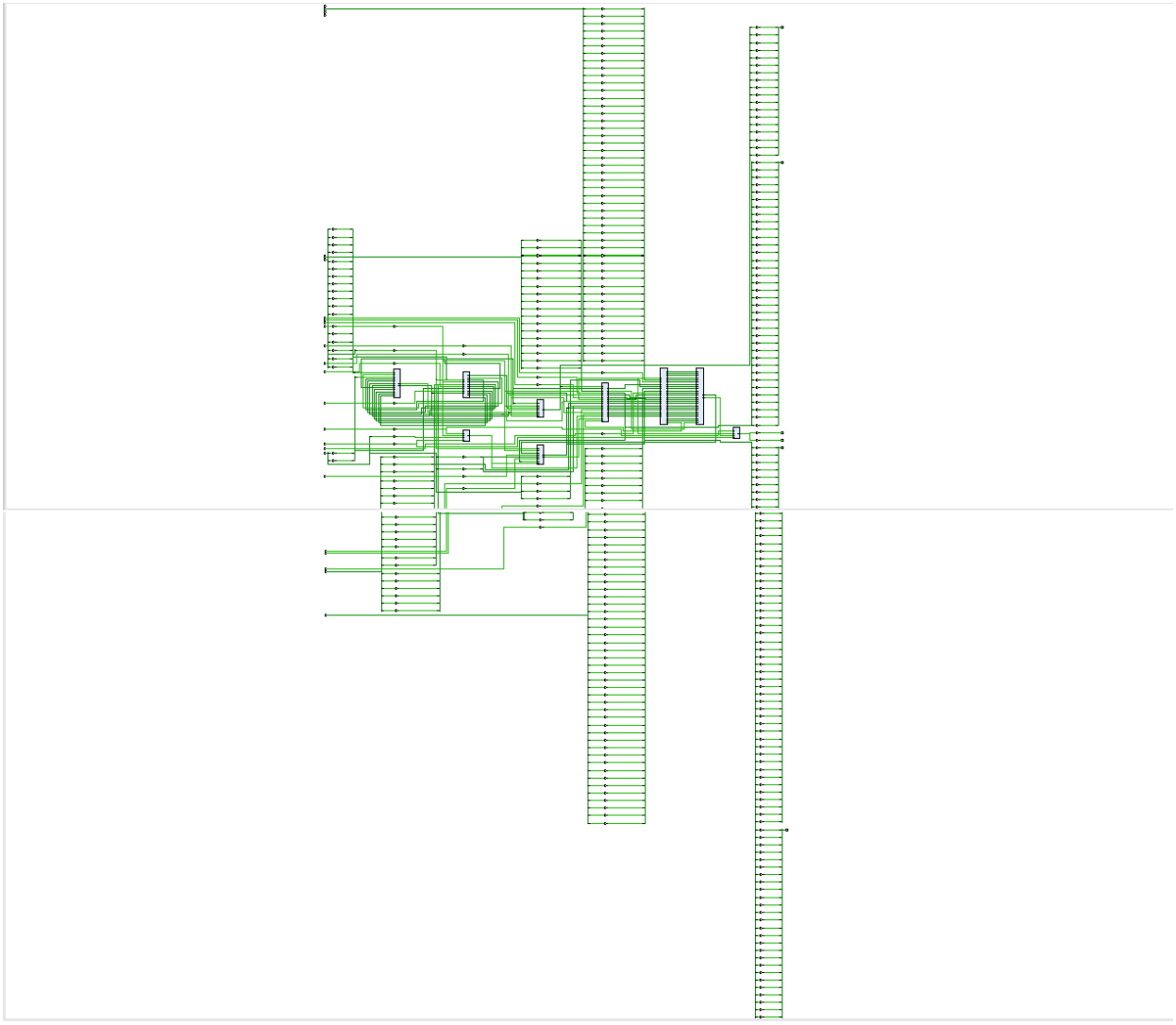
## “Messages” tab

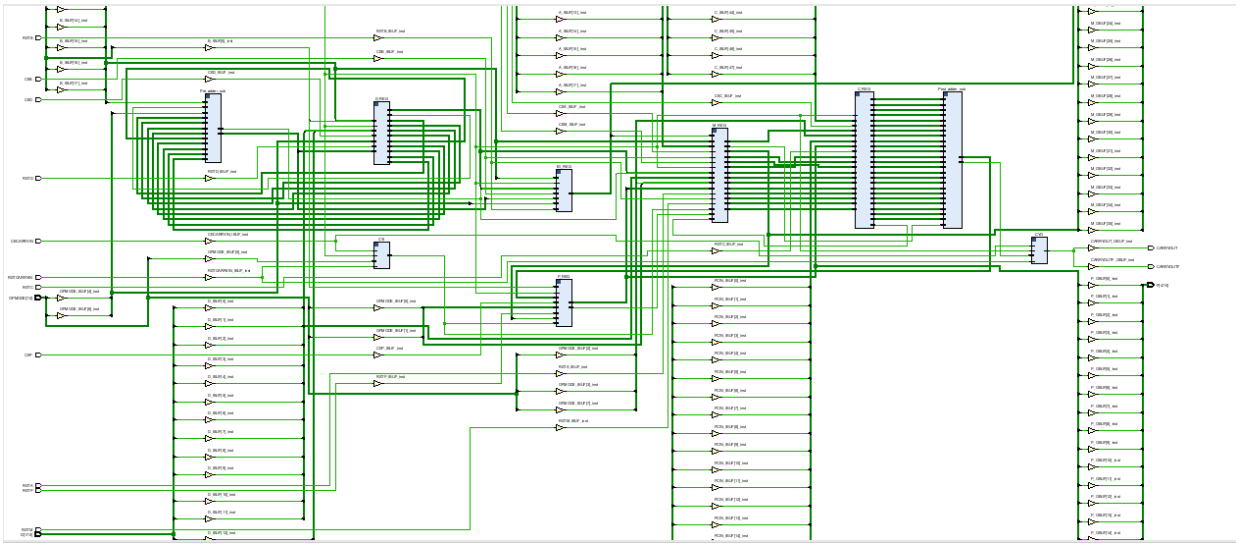



## Utilization Report

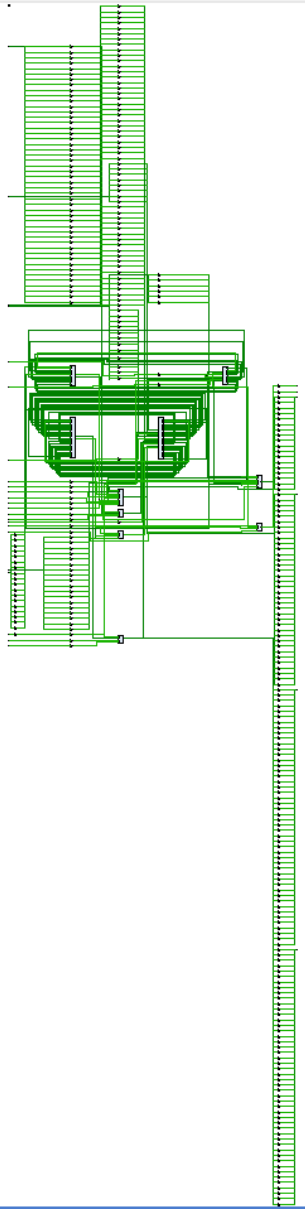


Schematic Snippets



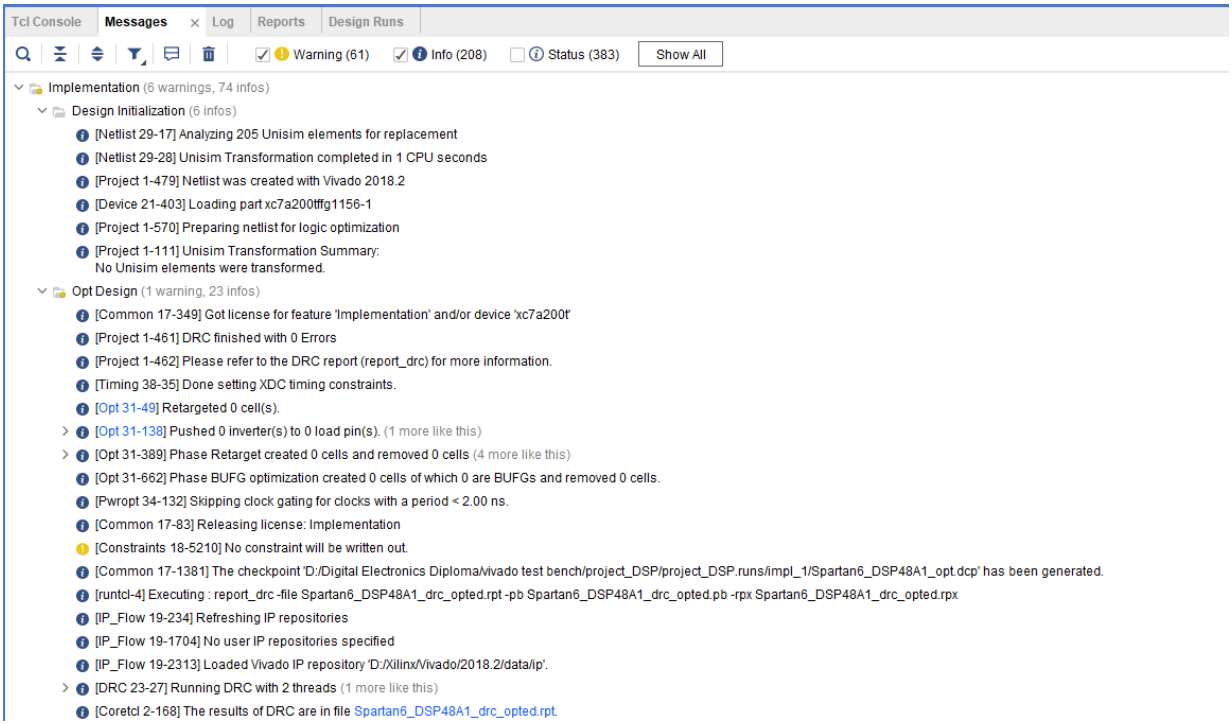


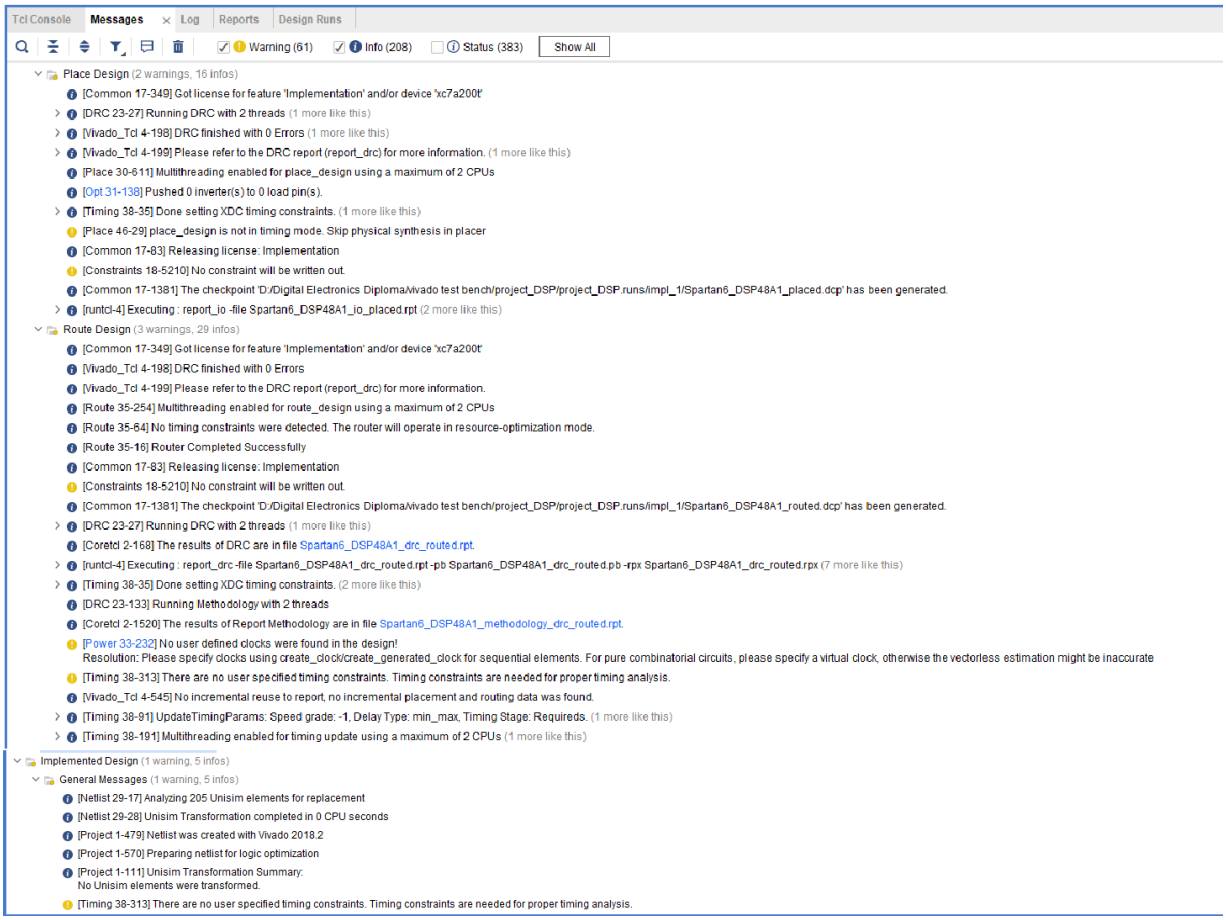
338 Cells 346 I/O Ports 871 Nets



# *Implementation*

## “Messages” tab




Tcl Console
Messages
Log
Reports
Design Runs
Warning (61)
Info (208)
Status (383)
Show All
Place Design (2 warnings, 16 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
[Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Timing 38-35] Done setting XDC timing constraints. (1 more like this)
[Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
[Common 17-83] Releasing license: Implementation
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'D:/Digital Electronics Diploma/vivado test bench/project_DSP/project_DSP.runs/impl_1/Spartan6_DSP48A1_placed.dcp' has been generated.
[runtcl-4] Executing : report_io -file Spartan6_DSP48A1_io_placed.rpt (2 more like this)
Route Design (3 warnings, 29 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
[Vivado_Tcl 4-198] DRC finished with 0 Errors
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
[Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
[Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.
[Route 35-16] Router Completed Successfully
[Common 17-83] Releasing license: Implementation
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'D:/Digital Electronics Diploma/vivado test bench/project_DSP/project_DSP.runs/impl_1/Spartan6_DSP48A1_routed.dcp' has been generated.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file Spartan6_DSP48A1_drc_routed.rpt -pb Spartan6_DSP48A1_drc_routed.pb -rpx Spartan6_DSP48A1_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file Spartan6_DSP48A1_methodology_drc_routed.rpt.
[Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
[Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
Implemented Design (1 warning, 5 infos)
General Messages (1 warning, 5 infos)
[Netlist 29-17] Analyzing 205 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

Schematic Snippets