

Project
Spartan6 - DSP48A1

Table of Contents

<i>RTL Code</i>	3
<i>Testbench Code</i>	6
<i>Do File</i>	9
<i>QuestaSim Snippets</i>	10
<i>Elaboration</i>	13
“Messages” tab	13
Schematic Snippets	13
<i>Synthesis</i>	14
“Messages” tab	14
Utilization Report	14
Schematic Snippets	15
<i>Implementation</i>	18
“Messages” tab	18
Schematic Snippets	20

RTL Code

```
1 module Spartan6_DSP48A1(A, B, C, D, CLK, CARRYIN, OPMODE, BCIN,  
2     RSTA, RSTB, RSTC, RSTD, RSTM, RSTP, RSTCARRYIN, RSTOPMODE,  
3     CEA, CEB, CEC, CED, CEM, CEP, CECARRYIN, CEOPMODE, PCIN,  
4     BCOUT, PCOUT, M, P, CARRYOUT, CARRYOUTF);  
5  
6     parameter A0REG=1'b0, A1REG=1'b1, B0REG=1'b0, B1REG=1'b1, CREG=1'b1, DREG=1'b1, MREG=1'b1, PREG=1'b1,  
7         CARRYINREG=1'b1, CARRYOUTREG=1'b1, OPMODEREG=1'b1, CARRYINSEL="OPMODE5", B_INPUT="DIRECT", RSTTYPE="SYNC";  
8  
9     input [17:0] A, B, D, BCIN;  
10    input [47:0] C, PCIN;  
11    input [7:0] OPMODE;  
12    input CLK, CARRYIN, RSTA, RSTB, RSTC, RSTD, RSTM,  
13        RSTP, RSTCARRYIN, RSTOPMODE, CEA, CEB, CEC, CED, CEM, CEP, CECARRYIN, CEOPMODE;  
14    output [47:0] P, PCOUT;  
15    output [17:0] BCOUT;  
16    output [35:0] M;  
17    output CARRYOUT, CARRYOUTF;  
18  
19    wire [7:0] OPMODE_MUX;  
20    wire [17:0] D_MUX, B_MUX0, A_MUX0, Pre_AdderMUX, Pre_AdderOUT, B_IN, A_MUX1, B_MUX1;  
21    wire [47:0] C_MUX, X_MUX, Z_MUX, M_MUX_extended, Post_AdderOUT, P_MUX;  
22    wire [35:0] MULT_OUT, M_MUX;  
23    wire CarryCascade_MUX, CYI_MUX, carryout, CYO_MUX;  
24  
25    REG_MUX #(18, DREG, RSTTYPE) D_REG(D, CLK, RSTD, CED, D_MUX);  
26    REG_MUX #(8, OPMODEREG, RSTTYPE) OPMODE_REG(OPMODE, CLK, RSTOPMODE, CEOPMODE, OPMODE_MUX);  
27    generate  
28        if (B_INPUT=="DIRECT")  
29            assign B_IN = B;  
30        else if(B_INPUT=="CASCADE")  
31            assign B_IN = BCIN;  
32        else  
33            assign B_IN = 'b0;  
34    endgenerate  
35  
36    REG_MUX #(18, B0REG, RSTTYPE) B0_REG(B_IN, CLK, RSTB, CEB, B_MUX0);  
37    REG_MUX #(18, A0REG, RSTTYPE) A0_REG(A, CLK, RSTA, CEA, A_MUX0);  
38    REG_MUX #(48, CREG, RSTTYPE) C_REG(C, CLK, RSTC, CEC, C_MUX);  
39    MUX2x1 Adder1MUX(B_MUX0, Pre_AdderOUT, OPMODE_MUX[4], Pre_AdderMUX);  
40    REG_MUX #(18, B1REG, RSTTYPE) B1_REG(Pre_AdderMUX, CLK, RSTB, CEB, B_MUX1);  
41    REG_MUX #(18, A1REG, RSTTYPE) A1_REG(A_MUX0, CLK, RSTA, CEA, A_MUX1);  
42    REG_MUX #(36, MREG, RSTTYPE) M_REG(MULT_OUT, CLK, RSTM, CEM, M_MUX);  
43    generate  
44        if (CARRYINSEL=="OPMODE5")  
45            assign CarryCascade_MUX= OPMODE_MUX[5];  
46        else if(CARRYINSEL=="CARRYIN")  
47            assign CarryCascade_MUX = CARRYIN;  
48        else  
49            assign CarryCascade_MUX = 'b0;  
50    endgenerate  
51    REG_MUX #(1, CARRYINREG, RSTTYPE) CYI(CarryCascade_MUX, CLK, RSTCARRYIN, CECARRYIN, CYI_MUX);  
52    assign M_MUX_extended = { {12 {M_MUX[35]} }, M_MUX };  
53    MUX4x1 X('b0, M_MUX_extended, P_MUX, {D[11:0], A, B}, OPMODE_MUX[1:0], X_MUX);  
54    MUX4x1 Z('b0, PCIN, P_MUX, C_MUX, OPMODE_MUX[3:2], Z_MUX);  
55    REG_MUX #(48, PREG, RSTTYPE) P_REG(Post_AdderOUT, CLK, RSTP, CEP, P_MUX);  
56    REG_MUX #(1, CARRYOUTREG, RSTTYPE) CYO(carryout, CLK, RSTCARRYIN, CECARRYIN, CYO_MUX);  
57  
58    adder_subtractor Pre_adder_sub (D_MUX, B_MUX0, 0, OPMODE_MUX[6], Pre_AdderOUT);  
59    adder_subtractor #(48) Post_adder_sub (Z_MUX, X_MUX, CYI_MUX, OPMODE_MUX[7], Post_AdderOUT, carryout);  
60  
61    assign MULT_OUT = A_MUX1 * B_MUX1;  
62    assign BCOUT = B_MUX1;  
63    assign M = M_MUX;  
64    assign CARRYOUT = CYO_MUX;  
65    assign CARRYOUTF = CYO_MUX;  
66    assign P = P_MUX;  
67    assign PCOUT = P_MUX;  
68    endmodule
```

```

1 module adder_subtractor(A,B,cin,operation,result,carryout);
2 parameter DATA_WIDTH = 18;
3 input [DATA_WIDTH-1:0] A,B;
4 input cin,operation;
5 output [DATA_WIDTH-1:0] result;
6 output carryout;
7
8 assign {carryout,result} = (operation)? (A-(B+cin)) : (A+(B+cin)) ;
9
10 endmodule

```

```

1 module MUX2x1(in0, in1, sel, out);
2     parameter WIDTH = 18;
3     input [WIDTH-1:0] in0, in1;
4     input sel;
5     output [WIDTH-1:0] out;
6     assign out = (sel == 0)? in0 : in1;
7 endmodule

```

```

1 module MUX4x1(in0, in1, in2, in3, sel, out);
2     input [47:0] in0, in1, in2, in3;
3     input [1:0] sel;
4     output [47:0] out;
5     assign out = (sel == 0)? in0 : (sel == 1)? in1 : (sel == 2)? in2 : in3;
6 endmodule

```

```

1 module REG_MUX(in, clk, rst, en, out);
2     parameter REG_WIDTH =18, REG_SEL=1, RST_TYPE="SYNC";
3     input [REG_WIDTH-1:0] in;
4     input rst, clk, en;
5     output [REG_WIDTH-1:0] out;
6
7     generate
8         if (REG_SEL)
9             Register #(.REG_WIDTH(REG_WIDTH), .RST_TYPE(RST_TYPE)) REG(in, rst, clk, en, out);
10        else
11            assign out = in;
12        endgenerate
13 endmodule

```

```
1 module Register(in, rst, clk, en, out);
2     parameter REG_WIDTH =18;
3     parameter RST_TYPE ="SYNC";
4
5     input [REG_WIDTH-1:0] in;
6     input rst, clk, en;
7     output reg [REG_WIDTH-1:0] out;
8
9     generate
10         if (RST_TYPE == "SYNC") begin
11             always @(posedge clk ) begin
12                 if (rst) begin
13                     out <= 'b0;
14                 end
15                 else if(en)
16                     out <= in;
17             end
18         end
19         else if(RST_TYPE == "ASYNC") begin
20             always @(posedge clk or posedge rst) begin
21                 if (rst) begin
22                     out <= 'b0;
23                 end
24                 else if(en)
25                     out <= in;
26             end
27         end
28     endgenerate
29 endmodule
```

Testbench Code

```
1  module DSP_48A1_tb();
2
3  parameter A0REG=1'b0, A1REG=1'b1, B0REG=1'b0, B1REG=1'b1, CREG=1'b1, DREG=1'b1, MREG=1'b1, PREG=1'b1,
4  CARRYINREG=1'b1, CARRYOUTREG=1'b1, OPMODEREG=1'b1, CARRYINSEL="OPMODE5", B_INPUT="DIRECT", RSTTYPE="SYNC";
5  reg [17:0] A,B,D,BCIN;
6  reg [47:0] C;
7  reg clk,RSTA,RSTB,RSTC,RSTD,RSTOPMODE,RSTM,RST_CARRYIN,RSTP;
8  reg CEA,CEB,CEC,CED,CE_OPMODE,CEM,CE_CARRYIN,CEP;
9  reg CARRYIN;
10 reg [47:0] PCIN;
11 reg [7:0] opmode;
12 wire [17:0] BCOUT;
13 wire [35:0] M;
14 wire [47:0] P,PCOUT;
15 wire CARRYOUT,CARRYOUTF;
16 Spartan6_DSP48A1 dut(A, B, C, D, clk, CARRYIN, opmode, BCIN,
17 RSTA, RSTB, RSTC, RSTD, RSTM, RSTP, RST_CARRYIN, RSTOPMODE,
18 CEA, CEB, CEC, CED, CEM, CEP, CE_CARRYIN, CE_OPMODE, PCIN,
19 BCOUT, PCOUT, M, P,CARRYOUT, CARRYOUTF);
20
21
22 initial begin
23     clk=0;
24     forever begin
25         #2 clk=~clk;
26     end
27 end
28 initial begin
29     RSTB=1;
30     RSTD=1;
31     #50;
32     repeat (20) begin
33         D=$random;
34         B=$random;
35         @(negedge clk);
36     end
37     RSTB=0;
```

```

38   RSTD=0;
39   RSTA=0;
40   RSTC=0;
41   RSTOPMODE=0;
42   RSTM=0;
43   RST_CARRYIN=0;
44   RSTP=0;
45   CEB=1;
46   CED=1;
47   CEA=1;
48   CEC=1;
49   CE_OPMODE=1;
50   CEM=1;
51   CE_CARRYIN=1;
52   CEP=1;
53   #2;
54   repeat (20) begin
55       A=5;
56       C=60;
57       D=7;
58       B=2;
59       BCIN=11;
60       opmode[6]=0;
61       opmode[4]=1;
62       CARRYIN=0;
63       PCIN='b0;
64       opmode[1:0]=2'b01;
65       opmode[3:2]=2'b11;
66       opmode[5]=1'b1;
67       opmode[7]=1;
68       @(negedge clk);
69   end
70   #2;
71   RSTB=1;
72   RSTD=1;
73   RSTA=1;
74   RSTC=1;

```

```

75   RSTOPMODE=1;
76   RSTM=1;
77   RST_CARRYIN=1;
78   RSTP=1;
79   #2;
80   RSTB=0;
81   RSTD=0;
82   RSTA=0;
83   RSTC=0;
84   RSTOPMODE=0;
85   RSTM=0;
86   RST_CARRYIN=0;
87   RSTP=0;
88   #2;
89   repeat (20) begin
90       A=5;
91       C=3;
92       D=7;
93       B=2;
94       BCIN=11;
95       opmode[6]=1;
96       opmode[4]=1;
97       CARRYIN=0;
98       PCIN=0;
99       opmode[1:0]=2'b01;
100      opmode[3:2]=2'b11;
101      opmode[5]=1'b0;
102      opmode[7]=0;
103      @(negedge clk);
104   end
105   #2;
106   RSTB=1;
107   RSTD=1;
108   RSTA=1;
109   RSTC=1;
110   RSTOPMODE=1;
111   RSTM=1;

```



```

112 RST_CARRYIN=1;
113 RSTP=1;
114 #2;
115 RSTB=0;
116 RSTD=0;
117 RSTA=0;
118 RSTC=0;
119 RSTOPMODE=0;
120 RSTM=0;
121 RST_CARRYIN=0;
122 RSTP=0;
123 #2;
124 repeat (20) begin
125     A=5;
126     C=60;
127     D=7;
128     B=2;
129     BCIN=11;
130     opmode[6]=0;
131     opmode[4]=1;
132     CARRYIN=0;
133     PCIN=0;
134     opmode[1:0]=2'b01;
135     opmode[3:2]=2'b11;
136     opmode[5]=1'b1;
137     opmode[7]=0;
138     @(negedge clk);
139 end
140 #2;
141 RSTB=1;
142 RSTD=1;
143 RSTA=1;
144 RSTC=1;
145 RSTOPMODE=1;
146 RSTM=1;
147 RST_CARRYIN=1;
148 RSTP=1;

```

```

149 #2;
150 RSTB=0;
151 RSTD=0;
152 RSTA=0;
153 RSTC=0;
154 RSTOPMODE=0;
155 RSTM=0;
156 RST_CARRYIN=0;
157 RSTP=0;
158 #2;
159 repeat (20) begin
160     A=5;
161     C=60;
162     D=7;
163     B=2;
164     BCIN=11;
165     opmode[6]=1;
166     opmode[4]=1;
167     CARRYIN=0;
168     PCIN=0;
169     opmode[1:0]=2'b01;
170     opmode[3:2]=2'b11;
171     opmode[5]=1'b0;
172     opmode[7]=1;
173     @(negedge clk);
174 end
175 #2;
176 RSTB=1;
177 RSTD=1;
178 RSTA=1;
179 RSTC=1;
180 RSTOPMODE=1;
181 RSTM=1;
182 RST_CARRYIN=1;
183 RSTP=1;
184 #2;
185 RSTB=0;

```



```

185     RSTB=0;
186     RSTD=0;
187     RSTA=0;
188     RSTC=0;
189     RSTOPMODE=0;
190     RSTM=0;
191     RST_CARRYIN=0;
192     RSTP=0;
193     #2;
194     repeat (30) begin
195         A=5;
196         C=60;
197         D=7;
198         B=2;
199         BCIN=11;
200         opmode[6]=1;
201         opmode[4]=0;
202         CARRYIN=0;
203         PCIN=0;
204         opmode[1:0]=$random;
205         opmode[3:2]=$urandom_range(0,2);
206         opmode[5]=1'b0;
207         opmode[7]=1;
208         @(negedge clk);
209     end
210     #2 $stop;
211 end
212 endmodule

```

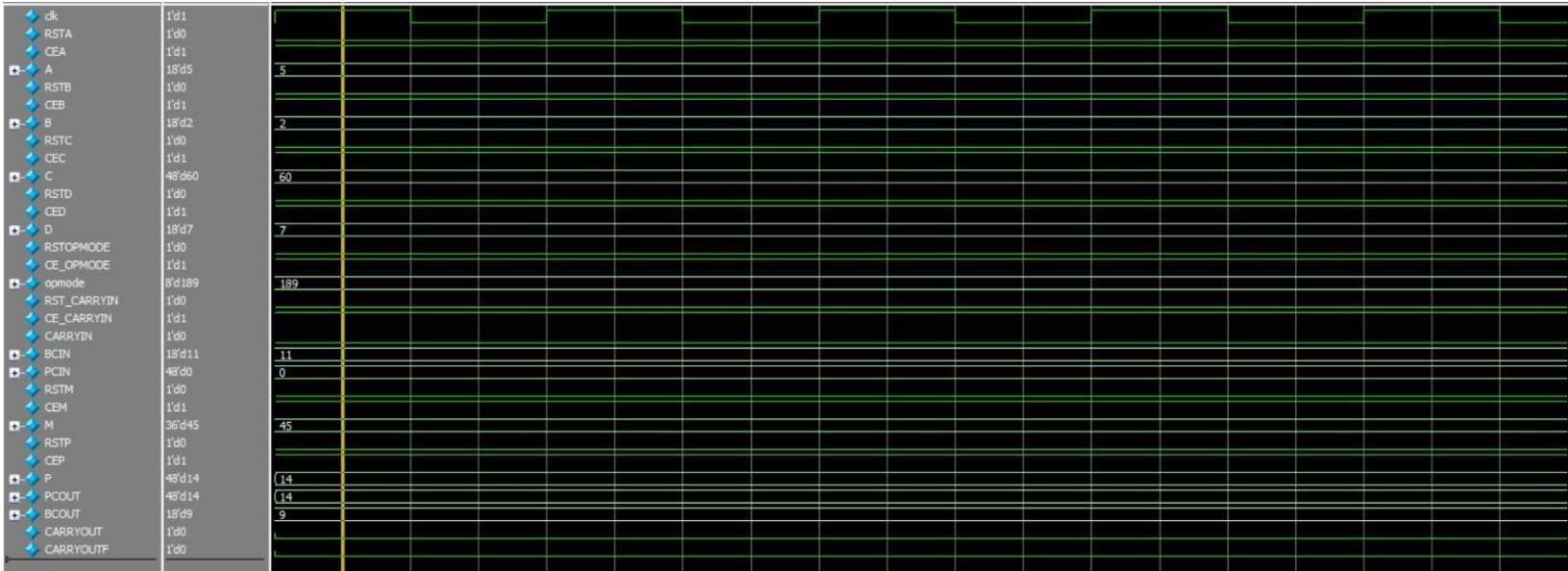
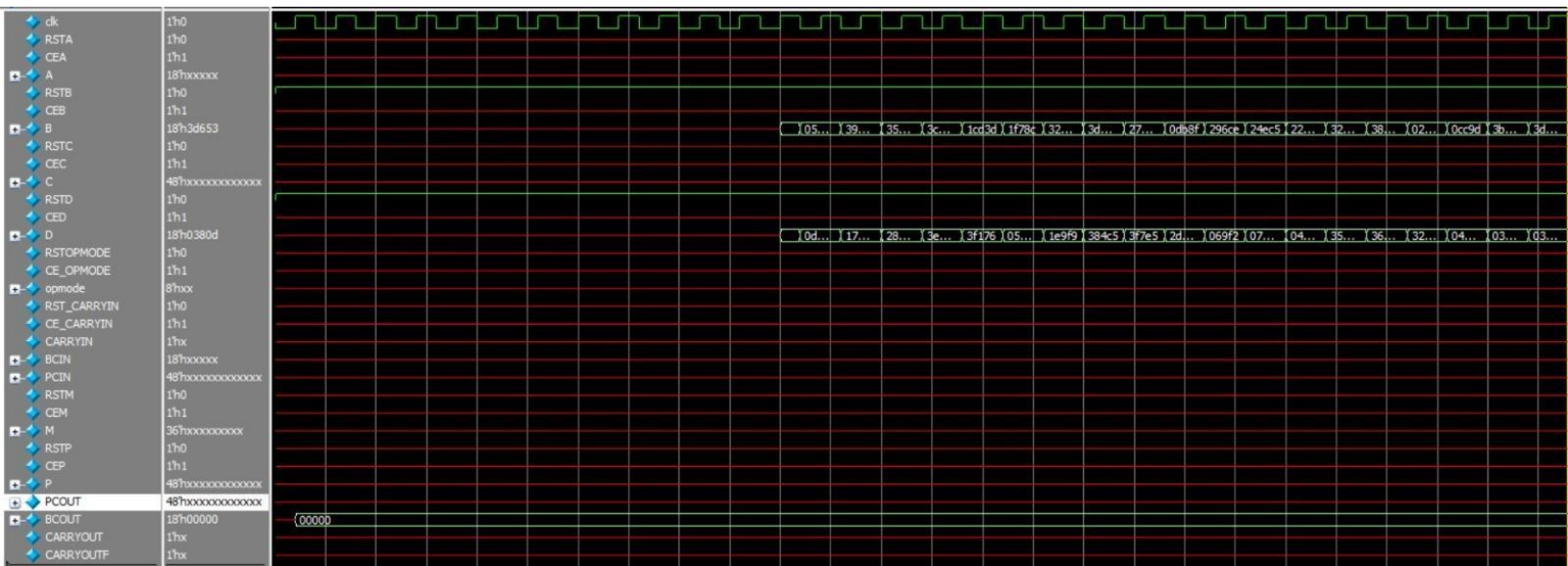
Do File

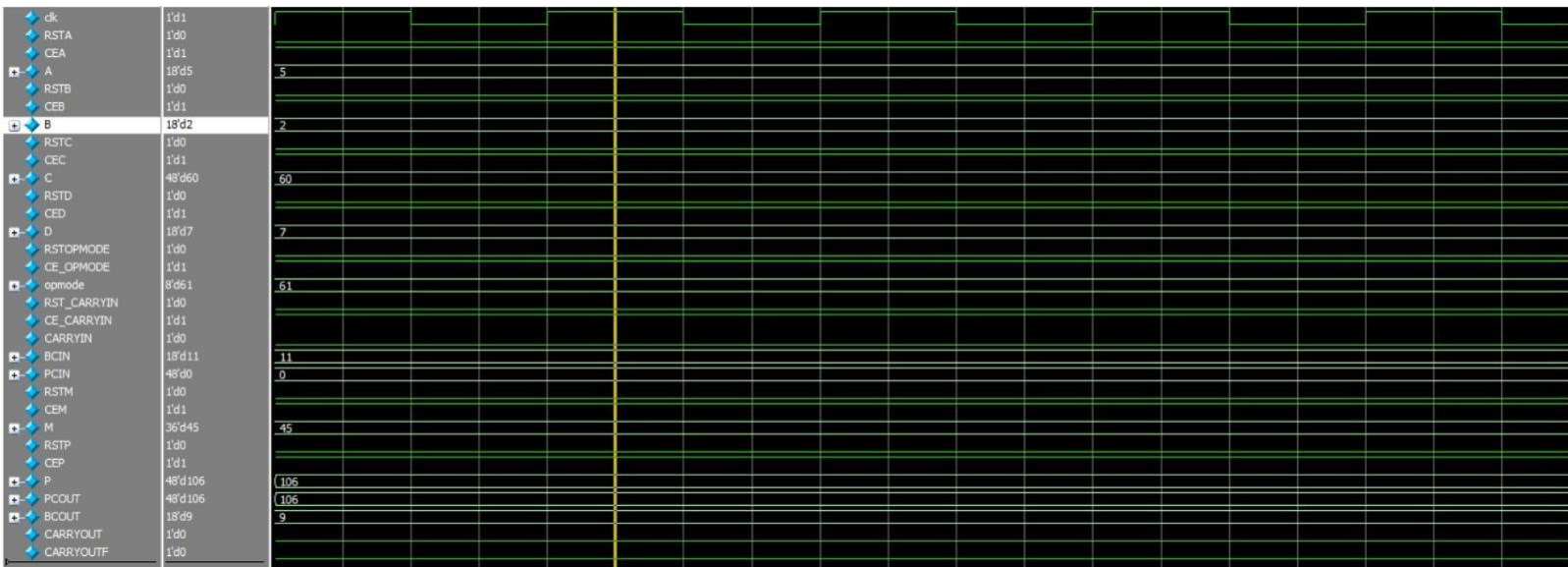
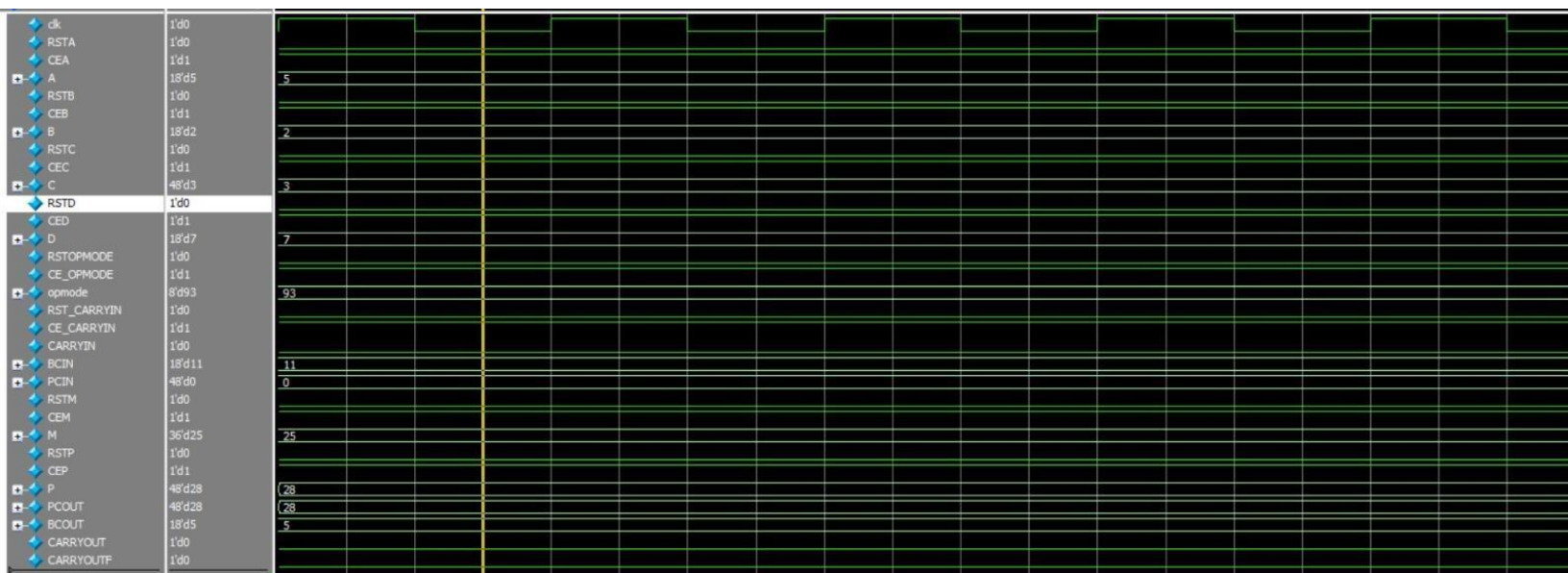
```

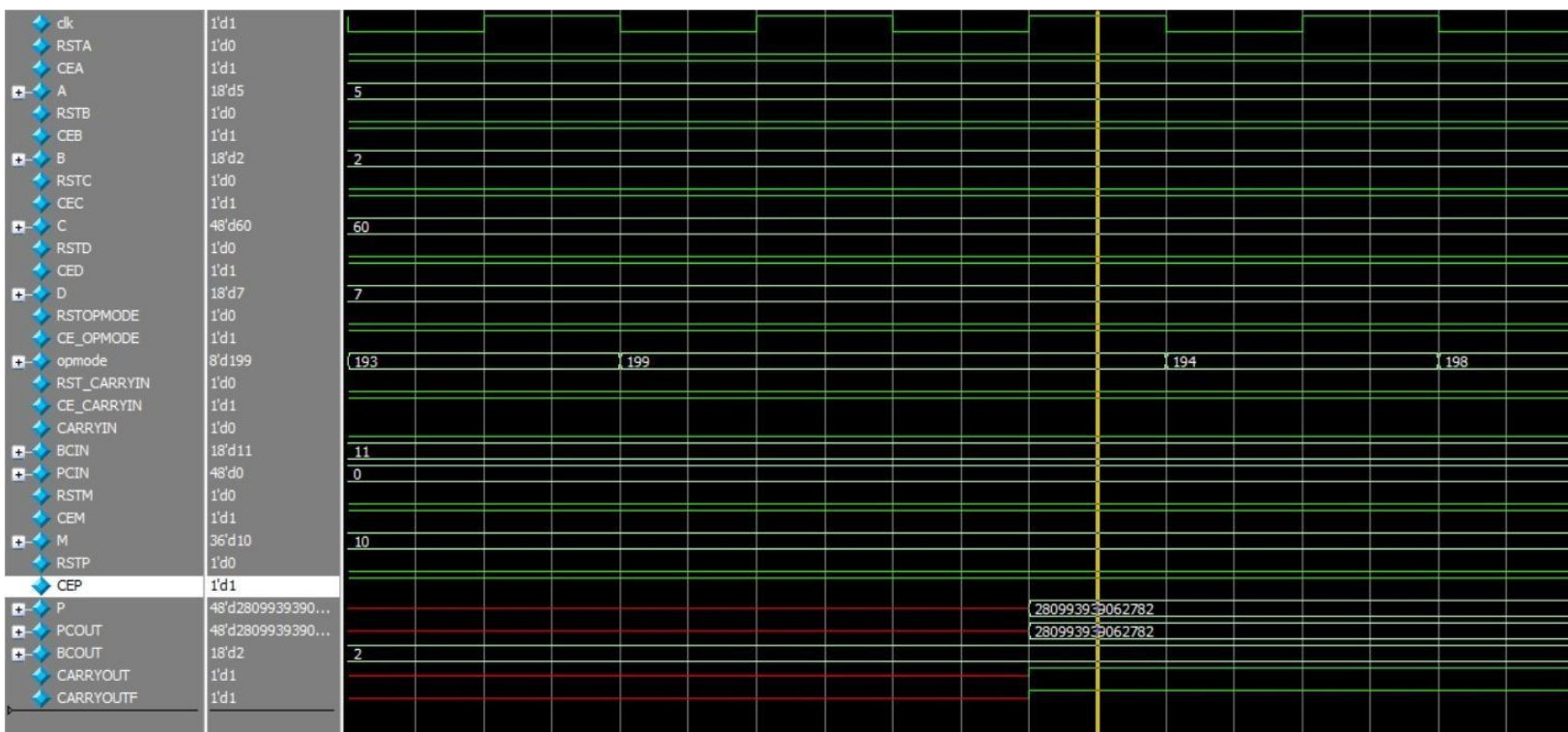
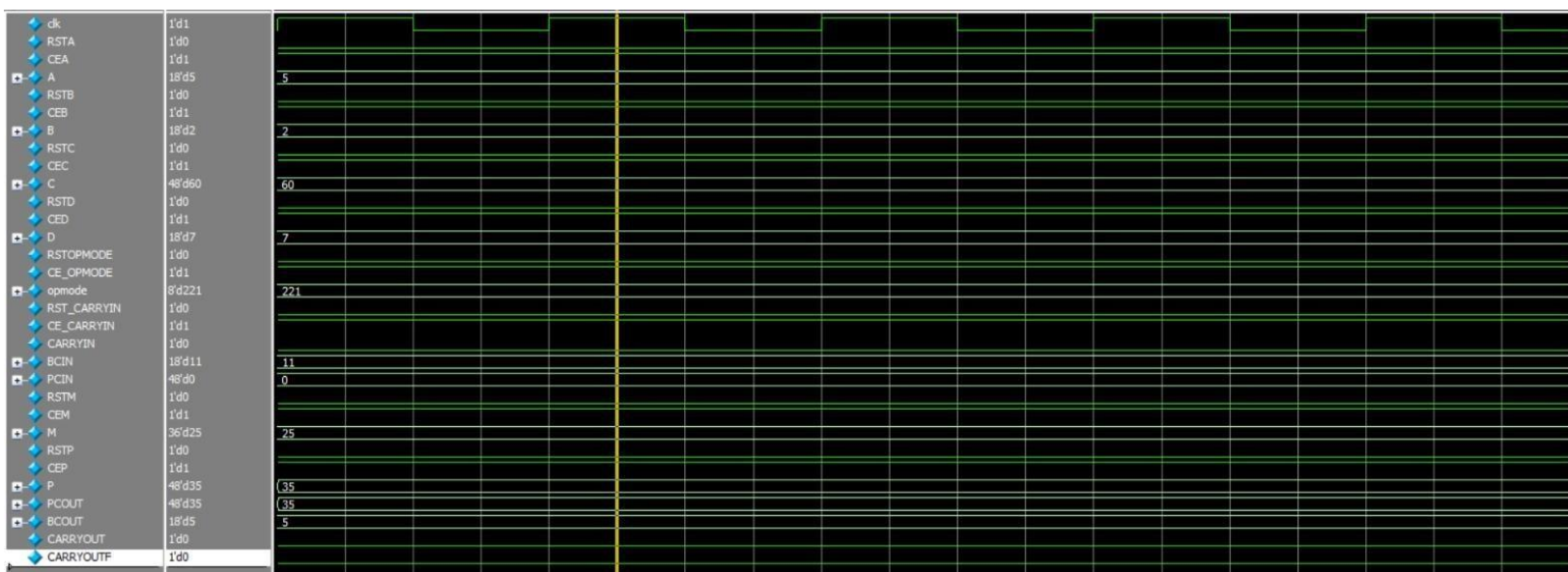
1 vlib work
2 vlog adder_sub.v REG_MUX.v Register.v MUX4x1.v MUX2x1.v Spartan6_DSP48A1.v DSP_48A1_tb.v
3 vsim -voptargs=+acc work.DSP_48A1_tb
4 add wave *
5 run -all

```

QuestaSim Snippets







Elaboration

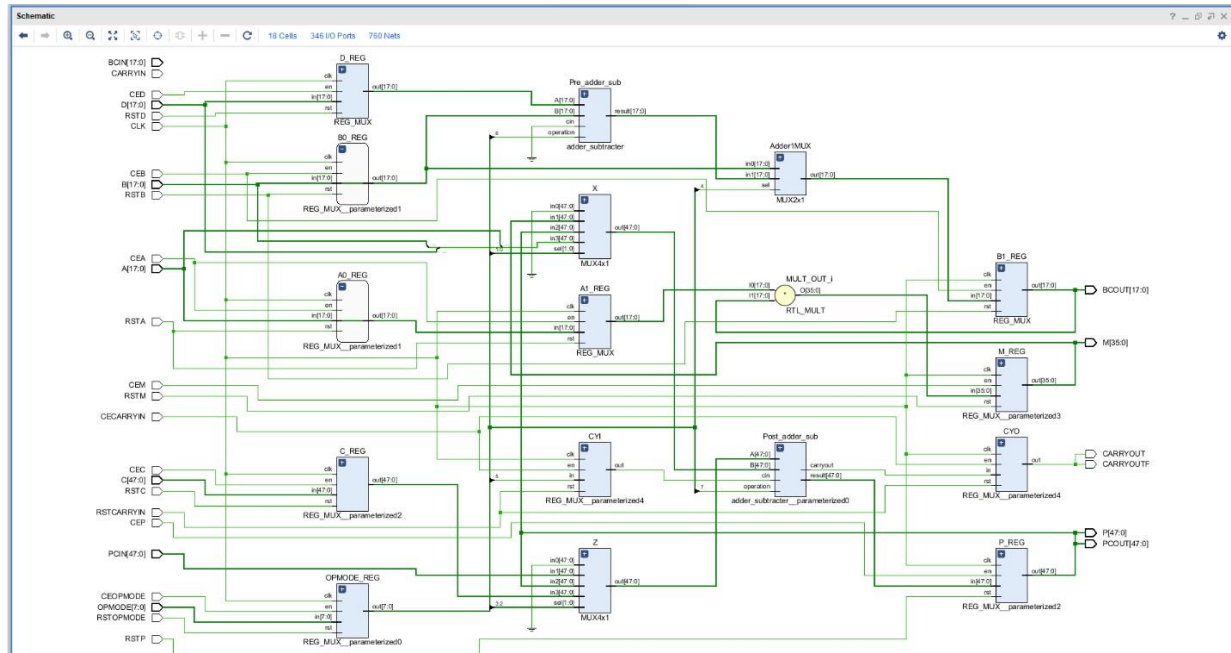
“Messages” tab

Tcl Console Messages x Log Reports Design Runs

Warning (61) Info (208) Status (383) Show All

- Vivado Commands (3 infos)
 - General Messages (3 infos)
- Elaborated Design (2 infos)
 - General Messages (2 infos)
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Schematic Snippets



Synthesis

“Messages” tab

Tcl Console Messages x Log Reports Design Runs

Q [Warning (61)] [Info (208)] [Status (383)] Show All

[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

▼ Synthesis (47 warnings, 43 infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- [Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [Spartan6_DSP48A1.v:1] (13 more like this)
- [Synth 8-6155] done synthesizing module 'Register' (1#1) [Register.v:1] (13 more like this)
- [Synth 8-350] instance 'Pre_adder_sub' of module 'adder_subtractor' requires 6 connections, but only 5 given [Spartan6_DSP48A1.v:58]
- [Synth 8-3331] design REG_MUX__parameterized0 has unconnected port clk (44 more like this)
- [Device 21-403] Loading part xc7a200tfg1156-1
- [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [adder_sub.v:8] (1 more like this)
- [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [Register.v:13]
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 205 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint D:/Digital Electronics Diploma/vivado test bench/project_DSP/project_DSP.runs/synth_1/Spartan6_DSP48A1.dcp has been generated.
- [runtcd-4] Executing : report_utilization -file Spartan6_DSP48A1_utilization_synth.rpt -pb Spartan6_DSP48A1_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Fri Aug 18 20:10:09 2023...

▼ Synthesized Design (1 warning, 7 infos)

▼ General Messages (1 warning, 7 infos)

- [Netlist 29-17] Analyzing 205 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
- [Timing 38-35] Done setting XDC timing constraints.
- [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

Utilization Report

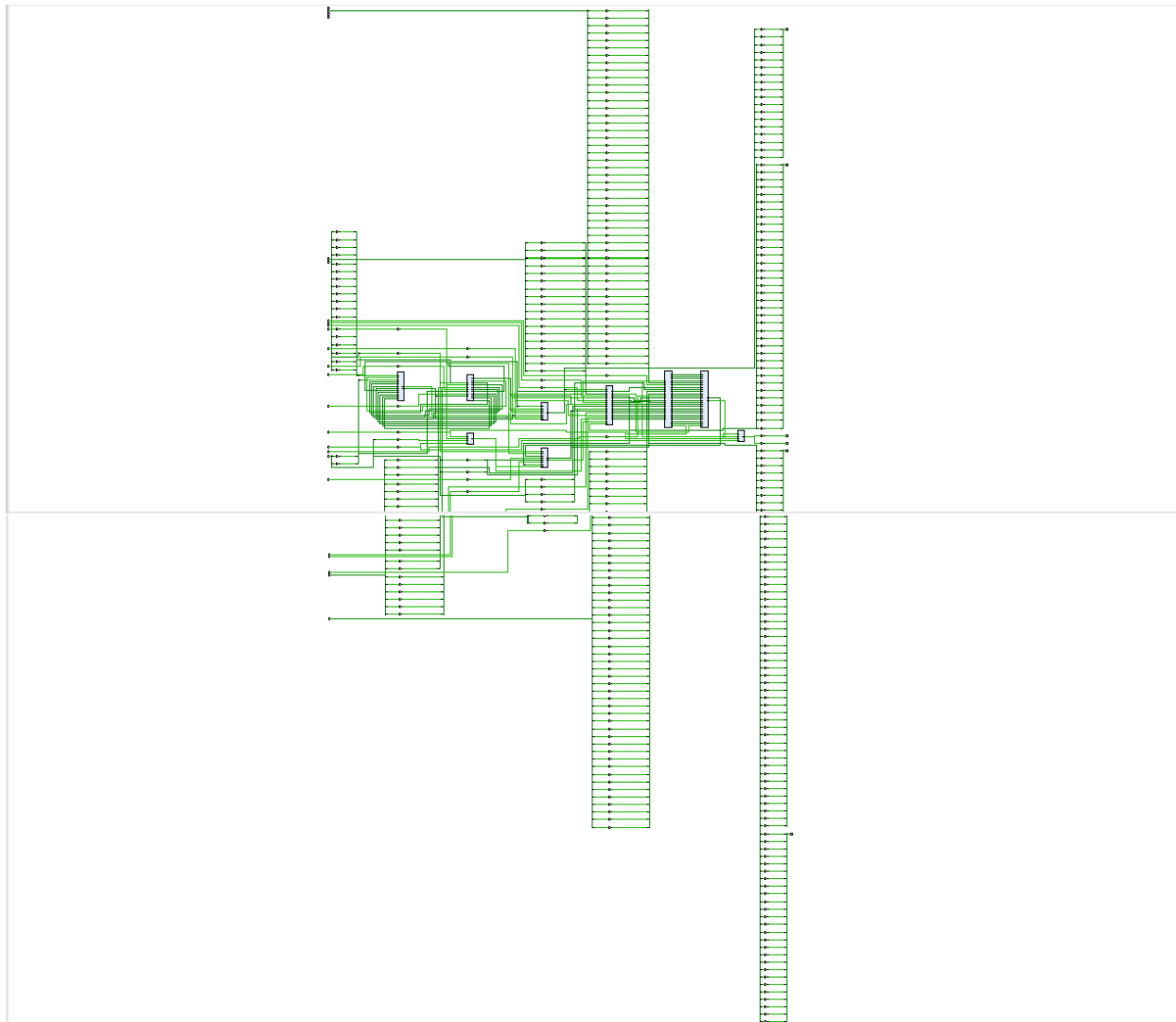
s Design Runs Utilization x Timing Debug

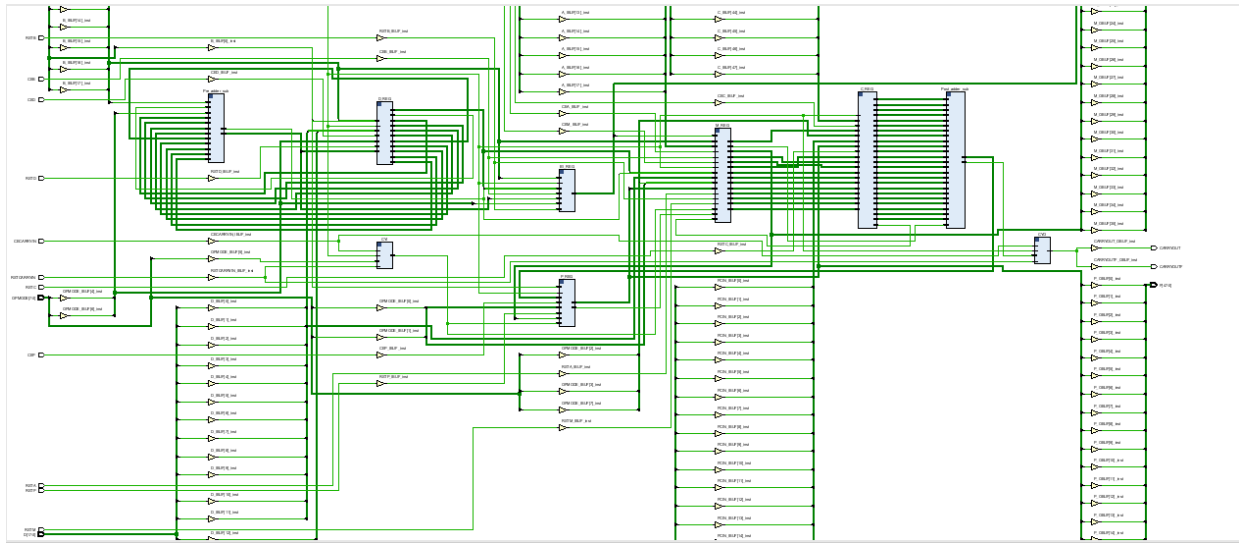
Summary

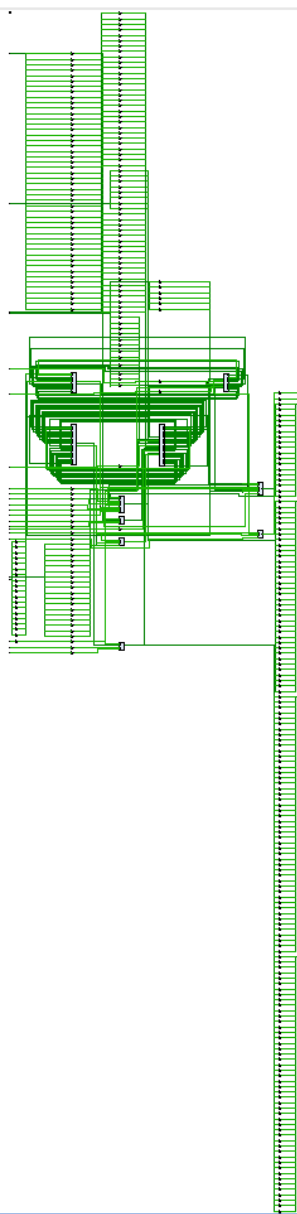
Resource	Utilization	Available	Utilization %
LUT	182	134600	0.14
FF	142	269200	0.05
DSP	1	740	0.14
IO	327	500	65.40

Utilization (%)

Schematic Snippets







Implementation

“Messages” tab

Tcl Console Messages x Log Reports Design Runs

Warning (61) Info (208) Status (383) Show All

Implementation (6 warnings, 74 infos)

Design Initialization (6 infos)

- [Netlist 29-17] Analyzing 205 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a200tffg1156-1
- [Project 1-570] Preparing netlist for logic optimization
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Opt Design (1 warning, 23 infos)

- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
- [Project 1-461] DRC finished with 0 Errors
- [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- [Timing 38-35] Done setting XDC timing constraints.
- [Opt 31-49] Retargeted 0 cell(s).
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
- [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- [Common 17-83] Releasing license: Implementation
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/Digital Electronics Diploma/Vivado test bench/project_DSP/project_DSP.runs/impl_1/Spartan6_DSP48A1_opt.dcp' has been generated.
- [runtcl-4] Executing : report_drc -file Spartan6_DSP48A1_drc_opted.rpt -pb Spartan6_DSP48A1_drc_opted.pb -rpx Spartan6_DSP48A1_drc_opted.rpx
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Xilinx/Vivado/2018.2/data/ip'.
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Corecl 2-168] The results of DRC are in file [Spartan6_DSP48A1_drc_opted.rpt](#).

Tcl Console Messages | Log Reports Design Runs

[Warning \(61\)](#) [Info \(208\)](#) [Status \(383\)](#) [Show All](#)

- Place Design (2 warnings, 16 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - [Opt 31-138] Pushed 0 Inverter(s) to 0 load pin(s).
 - [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 - [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
 - [Common 17-83] Releasing license: Implementation
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint D:/Digital Electronics Diploma/Vivado test bench/project_DSP/project_DSP.runs/impl_1/Spartan6_DSP48A1_placed.dcp has been generated.
 - [Junit4-J] Executing : report_io -file Spartan6_DSP48A1_io_placed.rpt (2 more like this)
- Route Design (3 warnings, 29 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
 - [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - [Route 35-84] No timing constraints were detected. The router will operate in resource-optimization mode.
 - [Route 35-16] Router Completed Successfully
 - [Common 17-83] Releasing license: Implementation
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint D:/Digital Electronics Diploma/Vivado test bench/project_DSP/project_DSP.runs/impl_1/Spartan6_DSP48A1_routed.dcp has been generated.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [CoreNet 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_routes.drp.
 - [Junit4-J] Executing : report_drc -file Spartan6_DSP48A1_drc_routes.drp -pb Spartan6_DSP48A1_drc_routes.pb -rpx Spartan6_DSP48A1_drc_routes.rpx (7 more like this)
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [DRC 23-133] Running Methodology with 2 threads
 - [CoreNet 2-1520] The results of ReportMethodology are in file Spartan6_DSP48A1_methodology_drc_routes.drp.
 - [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
 - [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
 - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
 - [Timing 38-81] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
 - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
- Implemented Design (1 warning, 5 infos)
 - General Messages (1 warning, 5 infos)
 - [NetList 29-17] Analyzing 205 Unisim elements for replacement
 - [NetList 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

Schematic Snippets

