XADC

Table

Description automatically generated

**Reference Inputs (VREFP and VREFN)**

VREFP and VREFN are providing differential reference voltage for XADC.

the reference voltage between VREFP and VREFN should be maintained at 1.25V ± 0.2% using an external reference IC.

The XADC also has an on-chip reference option which is selected by connecting VREFP and VREFN to ADCGND.

Diagram

Description automatically generated

**Analog Power Supply and Ground (VCCADC and GNDADC)**

Common ground impedance is a mechanism for noise coupling and needs to be carefully considered when designing the PCB.

The filtering should ensure no more than 1 LSB (250 uV) of noise on the reference output to minimize any impact on ADC accuracy at 12 bits.

Some PCB considerations:

Place the 100nF capacitor as close as possible to the package balls.

Place anti-alias filters for analog inputs close to the FPGA.

Place external reference IC and any dedicated analog power supply regulation as close to the FPGA as possible.

**Analog Inputs**

AD0P to AD15P and

AD0N to AD15N

Use anti-alias filter at the input.