Roll No: _____

Amrita Vishwa Vidyapeetham

M.TechFirst Assessment – February 2016
Second Semester

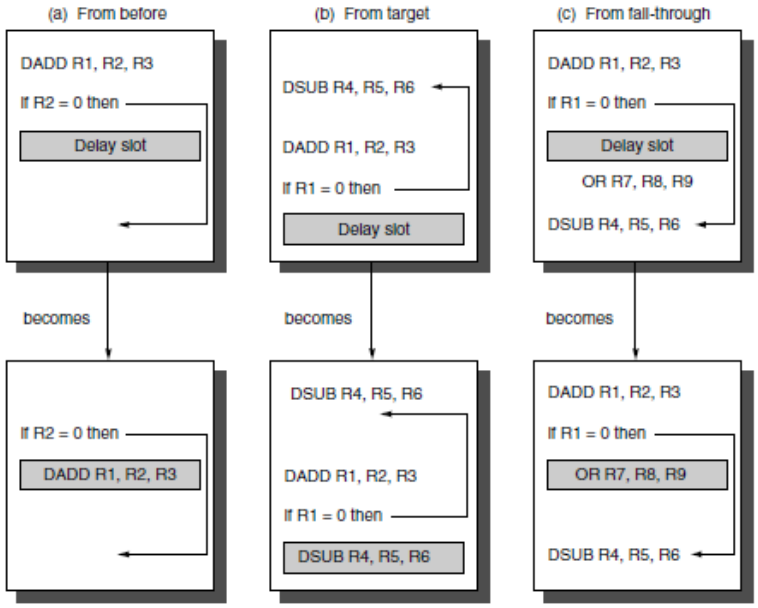
Embedded Systems

ES705 Multicore Architecture – Answer Key

Time: Two Hours **Maximum: 50 Marks**

Answer all Questions

1. What are different ways of scheduling the branch delay slot? **(4 marks)**



2. Consider the following performance measurements for a program: **(4 marks)**

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	4 GHz	4 GHz
CPI	1.0	1.1

Which computer has the higher MIPS rating and which computer is faster?

$$\text{MIPS} = \frac{\text{Instruction count}}{\frac{\text{Instruction count} \times \text{CPI}}{\text{Clock rate}} \times 10^6} = \frac{\text{Clock rate}}{\text{CPI} \times 10^6}$$

Computer A, MIPS = $4 \times 10^9 / 1.0 \times 10^6 = 4 \times 10^3$
Computer B, MIPS = $4 \times 10^9 / 1.1 \times 10^6 = 3.6 \times 10^3$
Computer A has higher MIPS and is faster.

3. What are the benchmarks for evaluating the performance of processors? **(4 marks)**

- *kernels*, which are small, key pieces of real applications;
- *toy programs*, which are 100-line programs from beginning programming assignments, such as quicksort; and
- *synthetic benchmarks*, which are fake programs invented to try to match the profile and behavior of real applications, such as Dhrystone.

The goal of benchmark suite is to characterize the relative performance of two computers – EEMBC(Electronic Design News Embedded Microprocessor Benchmark consortium) and SPEC (Standard Performance Evaluation Corporation).

4. You are designing a system for a real-time application in which specific deadlines must be met. Finishing the computation faster gains nothing. You find that your system can execute the necessary code, in the worst case, twice as fast as necessary.

a) How much energy do you save if you execute at the current speed and turn off the system when the computation is complete? **(2 marks)**

50%

b) How much energy do you save if you set the voltage and frequency to be half as much? **(2 marks)**

Energy = ½ capacitive load × V^2

Changing the frequency does not affect energy but only power. So the new energy is

$Energy_{new}$ = ½ capacitive load × (½ $V)^2$

= ¼ (½ capacitive load × V^2)

Energy saved is ¼ of the old energy.

5. You have a system that contains a special processor for doing floating-point operations.You have determined that 50% of your computations can use the floating-point processor. The speedup of the floating pointing-point processor is 15. What is the overall speedup achieved by using the floating-point processor. **(4 marks)**

F=0.5, Speedup = 15

Overall speedup achieved by using the floating-point processor = 1/((1-F)+F/S)

= 1/(0.5+0.033) = 1.876

6. Consider the following code fragment:

```
Loop:LD R1, 0(R2)
     DADDI R1, R1, #1
     SD 0(R2, R1
     DADDI R2, R2, #4
     DSUB R4, R3, R2
     BNEZ R4, Loop
```

Show the timing sequence for RISC pipeline without any forwarding or bypassing hardware but assuming a register read and write in the same clock cycle. **(4 marks)**

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD	R1, 0(R2)	F	D	X	M	W													
DADDI	R1, R1, #1		F	s	s	D	X	M	W										
SD	0(R2), R1					F	s	s	D	X	M	W							
DADDI	R2, R2, #4								F	D	X	M	W						
DSUB	R4, R3, R2									F	s	s	D	X	M	W			
BNEZ	R4, Loop												F	s	s	D	X	M	W

7. Consider an unpipelined processor, which has 2-ns clock cycle. It uses 4 cycles for ALU operations and 5 cycles for branches and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 35% and 25%respectively. There is a 0.125ns of clock overhead due to clock skew and set up. Ignoring any latency impact, how much speed up in the instruction execution rate can be obtained from a pipeline? **(4 marks)**

Average instruction execution time

= 2 ns x ((40% + 25%) x 4 + 35% x 5)

= 8.7ns

Speedup from pipeline

= Average instruction time unpiplined/Average instruction time pipelined

= 8.7ns/1.125ns = 7.73

8. Consider a load/store computer with the following instruction mix:

Operation	Frequency	No. of Clock cycles
ALU ops	35%	1
Loads	25%	2
Stores	15%	2
Branches	25%	3

a) Compute the CPI. **(2 marks)**

CPI_{old} = (0.35x1) + (0.25x2) + (0.15x2) + (0.25x3) = 1.9

b) It is observed that 35% of the ALU ops are paired with a load, and it is proposed to replace these ALU ops and their loads with a new instruction. The new instruction takes 1 clock cycle. With the new instruction added, branches take 5 clock cycles, Compute the CPI for the new version. **(2 marks)**

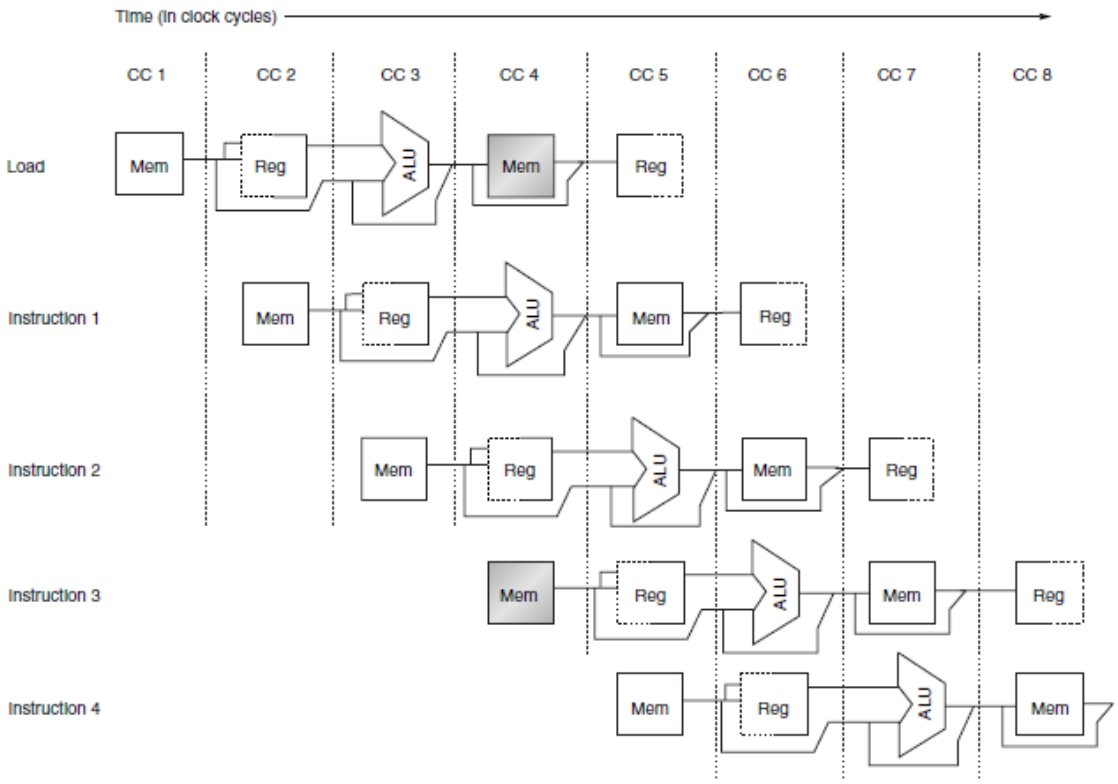
0.35 x 0.35 = 0.1225

CPI_{new} = ((0.35–0.1225)x1 + (0.25– 0.1225)x2 + 0.15x2 + 0.25x5 + 0.1225x1) / (1-0.1225)

= 2.455

9. Why do designers allow structural hazards? Explain with an example and data path diagrams. **(6 marks)**

The primary reason is to reduce cost of the unit, since pipelining all the functional units, or duplicating them, may be too costly. For example, processors thatsupport both an instruction and a data cache access every cycle require twice as much total memorybandwidth and often have higher bandwidth at the pins. Likewise, fully pipelininga floating-point multiplier consumes lots of gates.



10. Consider the following code:

```
LDR R3, R0, R1
LDR R2, R0, R3
ADD R3, R2, R2
ADD R3, R3, R2
ADDI R1, R1, 4
SUBI R4, R4, 1
```

List and specify the type of hazards. Use forwarding wherever possible to rectify the hazards. Show the rectification using pipeline data path diagram. **(6 marks)**

Refer class notes

11. Consider a computer implemented in single-cycle implementation. When the stages are split by functionality, the stages do not require exactly the same amount of time. The original machine had a clock cycle time of 7 ns. After the stages were split, the measured time were IF, 1 ns; ID, 1.5ns; EX, 1ns; MEM, 2ns; and WB, 1.5 ns. The pipeline register delay is 0.1ns.

(i) What is the clock cycle time of the 5-stage pipelined machine? **(1 mark)**

Out of the 5 stages, MEM stage is the slowest (largest execution time) with 2ns and there is an overhead of pipeline register delay of 0.1ns. Therefore, the clock cycle time for the pipeline system, CT (new) = 2ns + 0.1ns = 2.1ns

(ii) If there is a stall every 4 instructions, what is the CPI of the new machine? **(1 mark)**

CPI = Ideal CPI + Stall cycles

Ideal CPI is assumed to be 1. There is a stall every 4 instructions. So, per instruction the stall cycles = 1/4 = 0.25

Therefore, CPI(with stalls) = 1 + 0.25 = 1.25

(iii) What is the speedup of the pipelined machine over the single cycle machine? **(2 marks)**

Speedup = execution time for non-pipelined architecture / execution time for pipelined architecture

Execution Time = I × CPI × Cycle Time

Assume CPI for non-pipelined as 1.

Speedup = (Ix1x7)/(Ix1.25x2.1) = 7/2.625 = 2.67 times speedup

(iv) If the pipelined machine had an infinite number of stages, what would its speedup be over the single-cycle machine? **(2 marks)**

The speedup is equal to the number of tasks/instructions
