



# Sharif University of Technology

## Computer Architecture

### **Quartus II Tutorial**

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Spring 2017

# Download

- Windows:

Quartus:

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/QuartusLiteSetup15.1.0.185-windows.exe>

Modelsim:

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/ModelSimSetup-15.1.0.185-windows.exe>

Devices:

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclone-15.1.0.185.qdz>

or

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclonev-15.1.0.185.qdz>

- Linux:

All Files:

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/Quartus-lite-15.1.0.185-linux.tar>

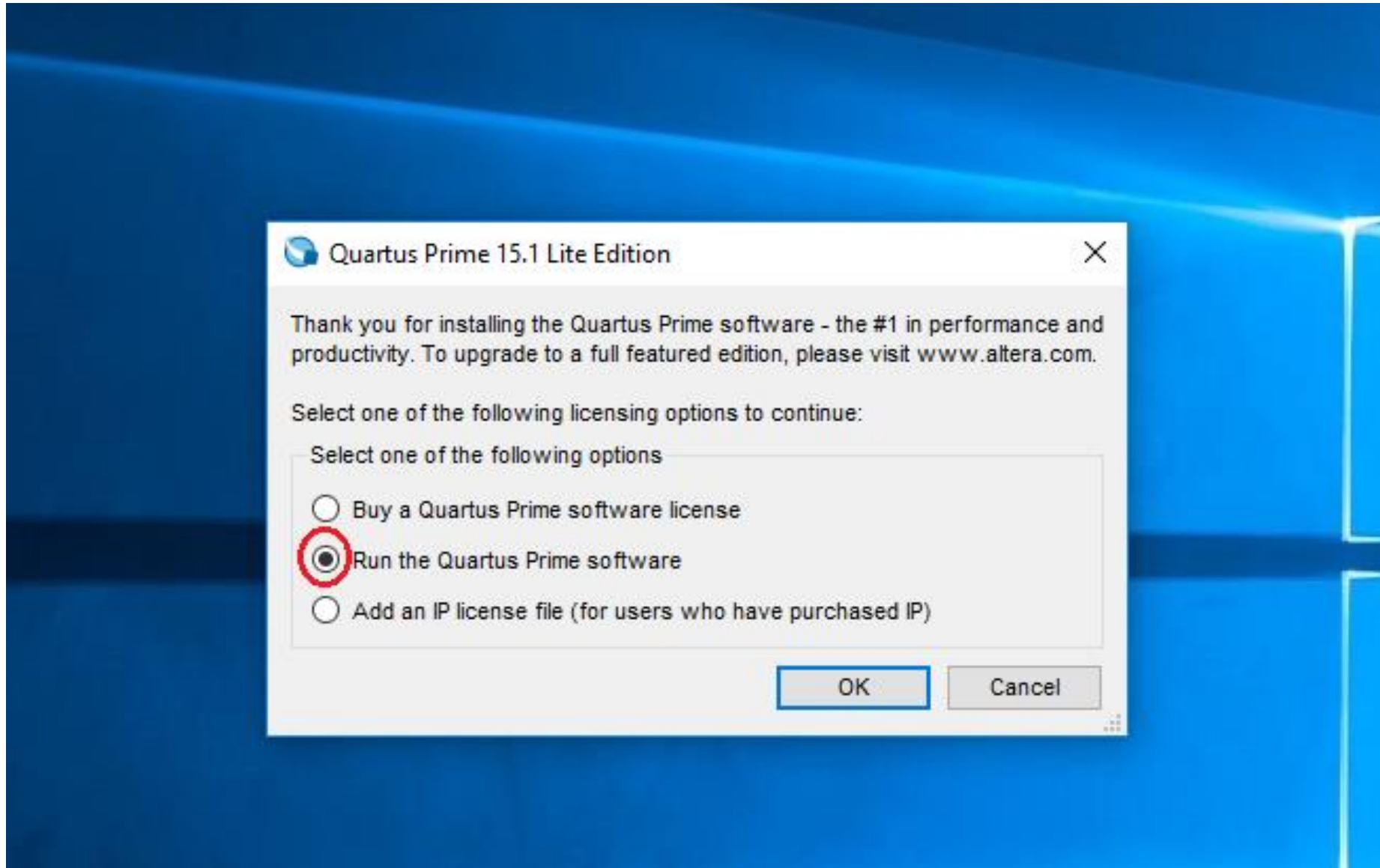
- Mac:

Run the windows version in Parallel Windows

# Install

- Put all files in the same folder and run Quartus install
- Do NOT change any of the default install settings

# After Install



# Install Devices (Manual)

- Download .qdz file

- Windows

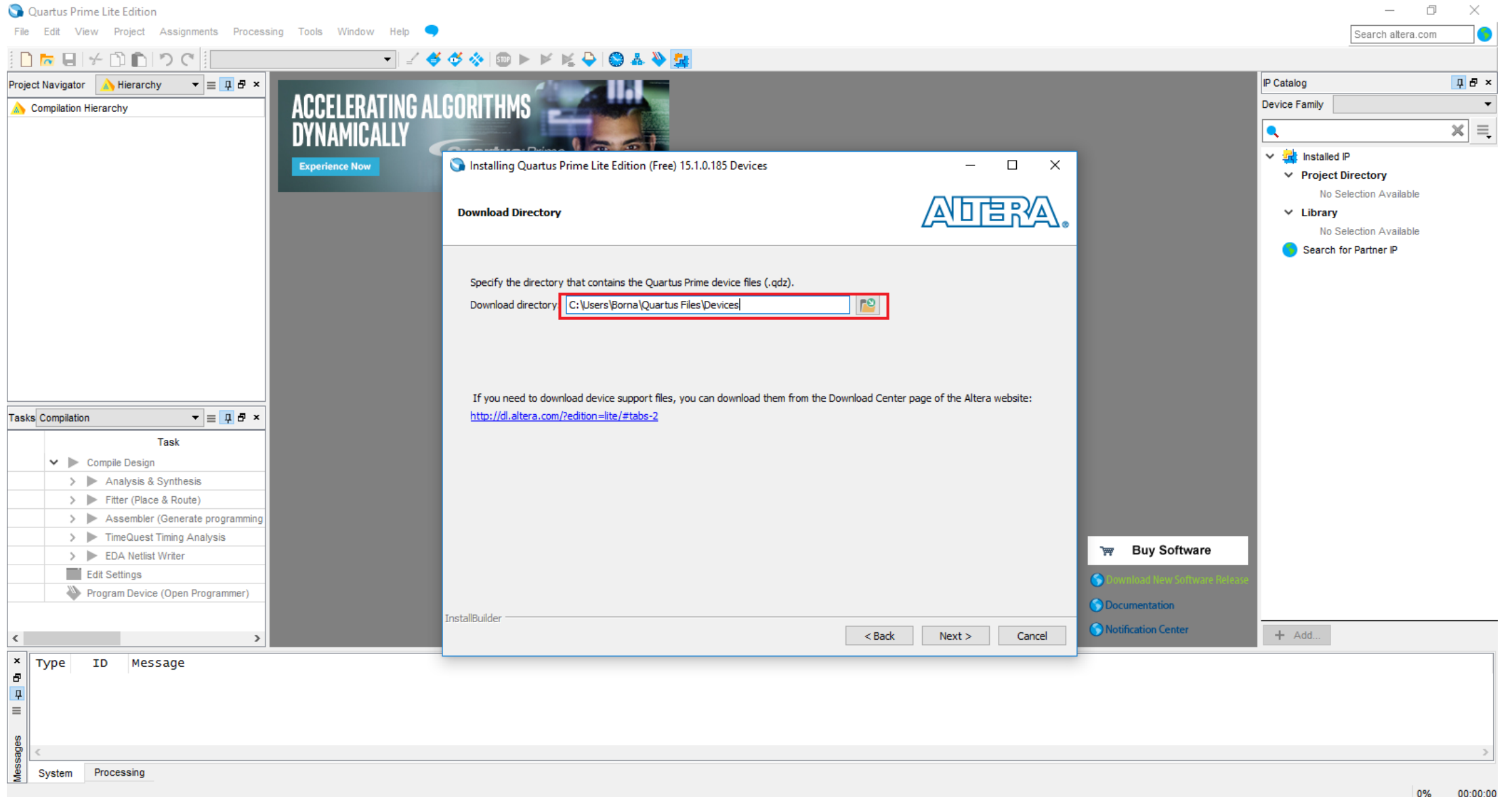
<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclone-15.1.0.185.qdz>

- Linux

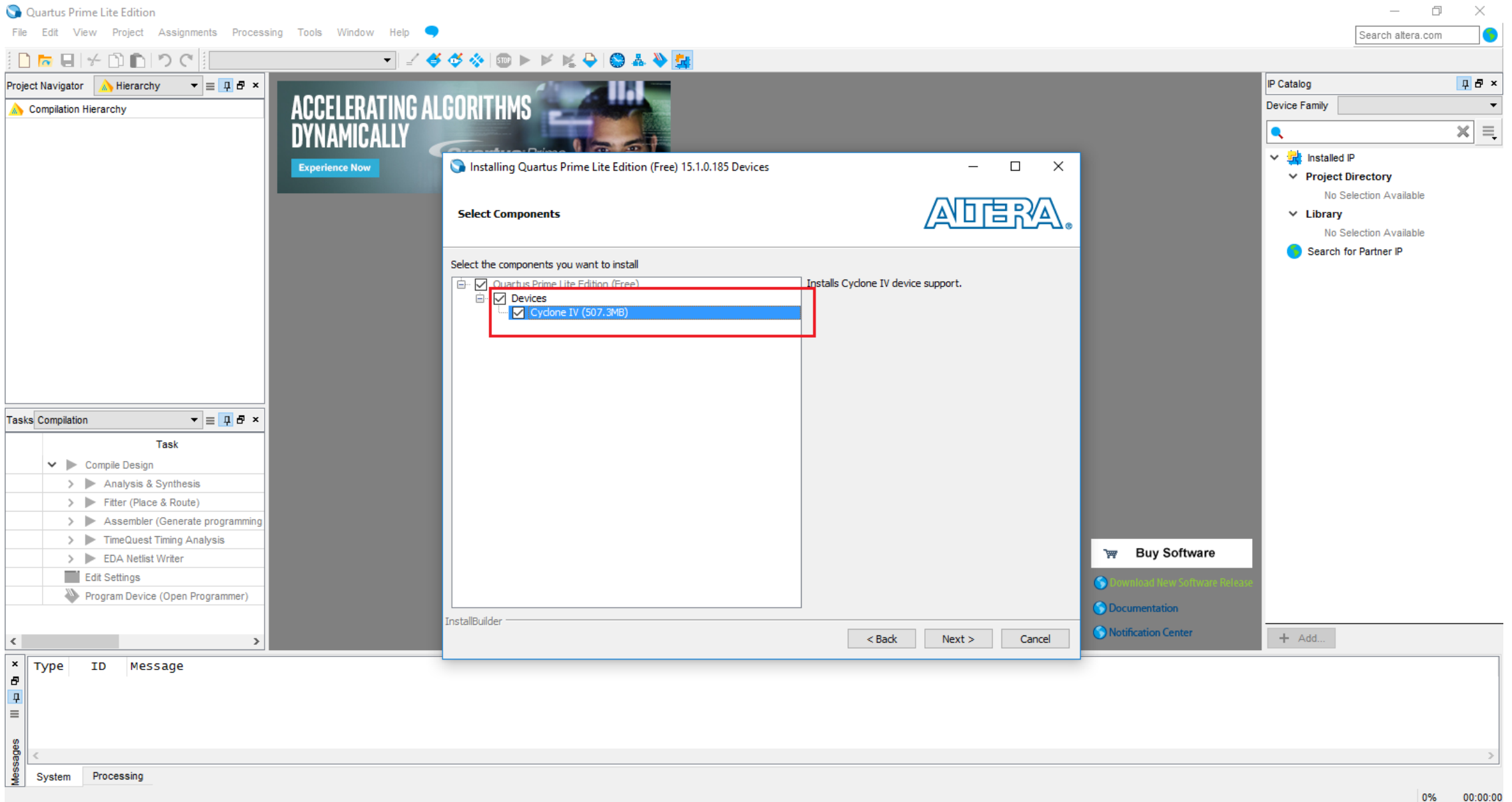
In the same zip folder as quartus

- Install .qdz file as devices

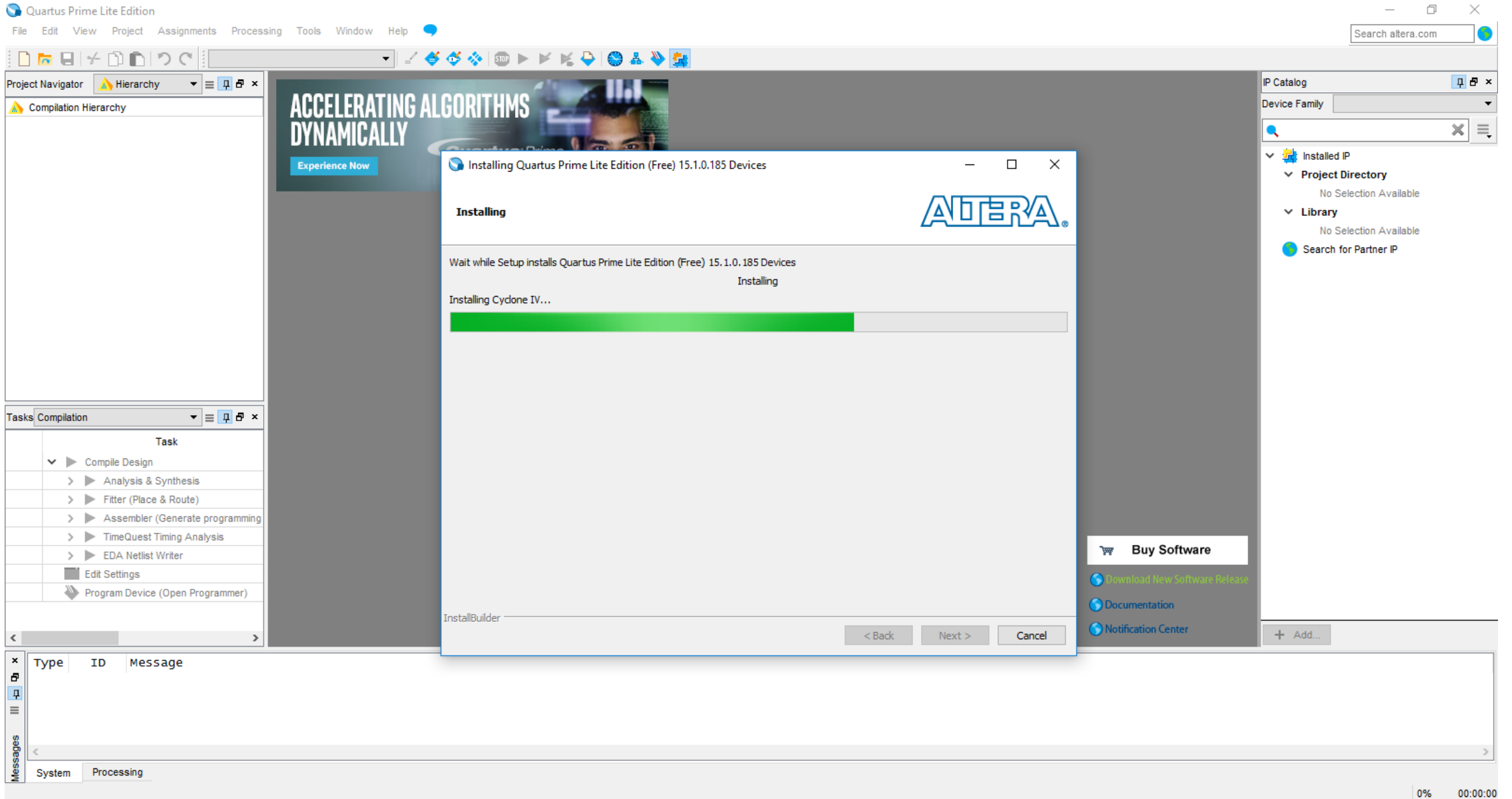
# Install .qdz file as devices (Manual)



# Install .qdz file as devices (Manual)



# Install .qdz file as devices (Manual)





# Install Modelsim (Manual)

- Download
  - Windows

<ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/ModelSimSetup-15.1.0.185-windows.exe>

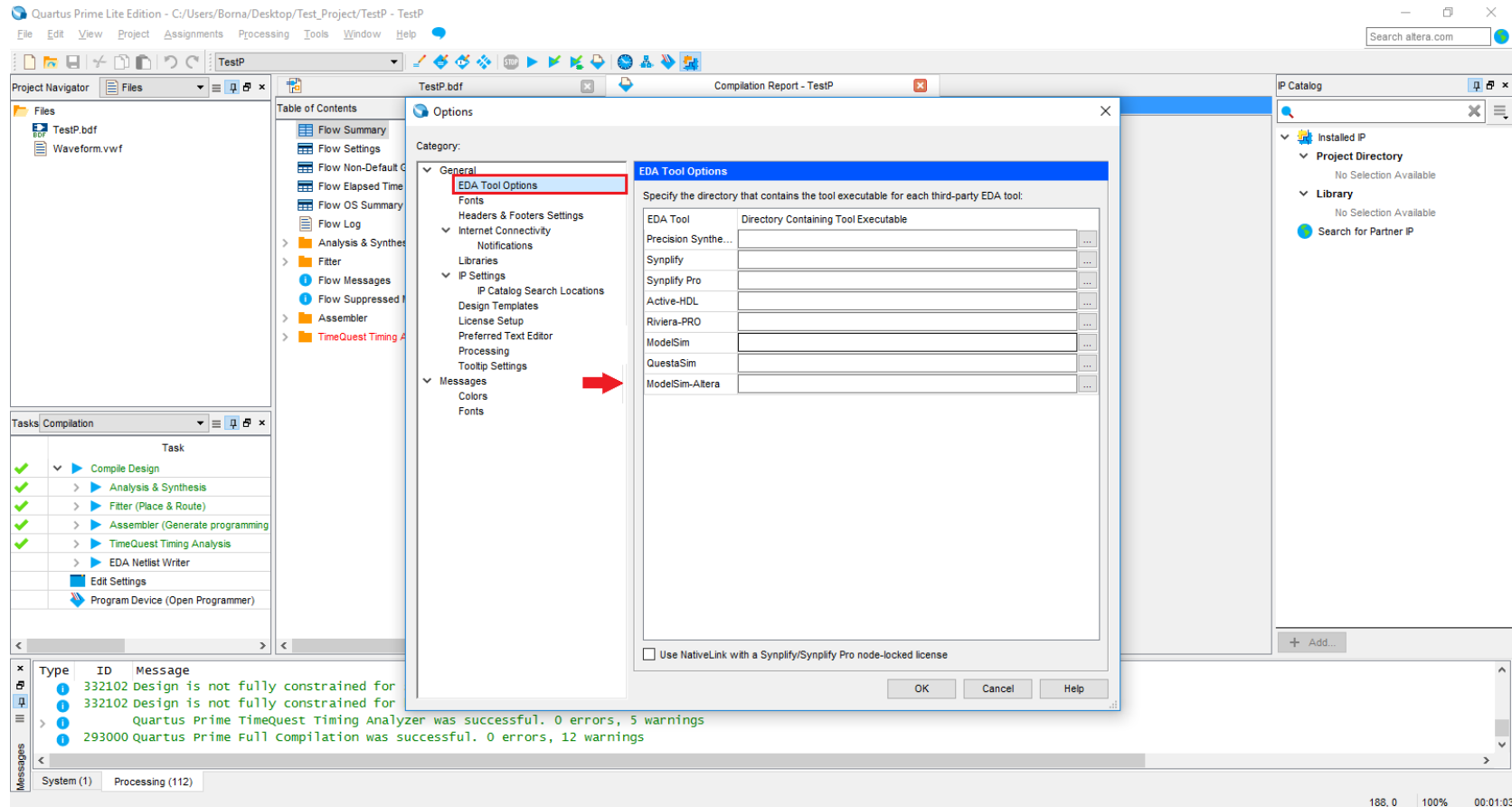
- Linux

In the same zip folder as quartus

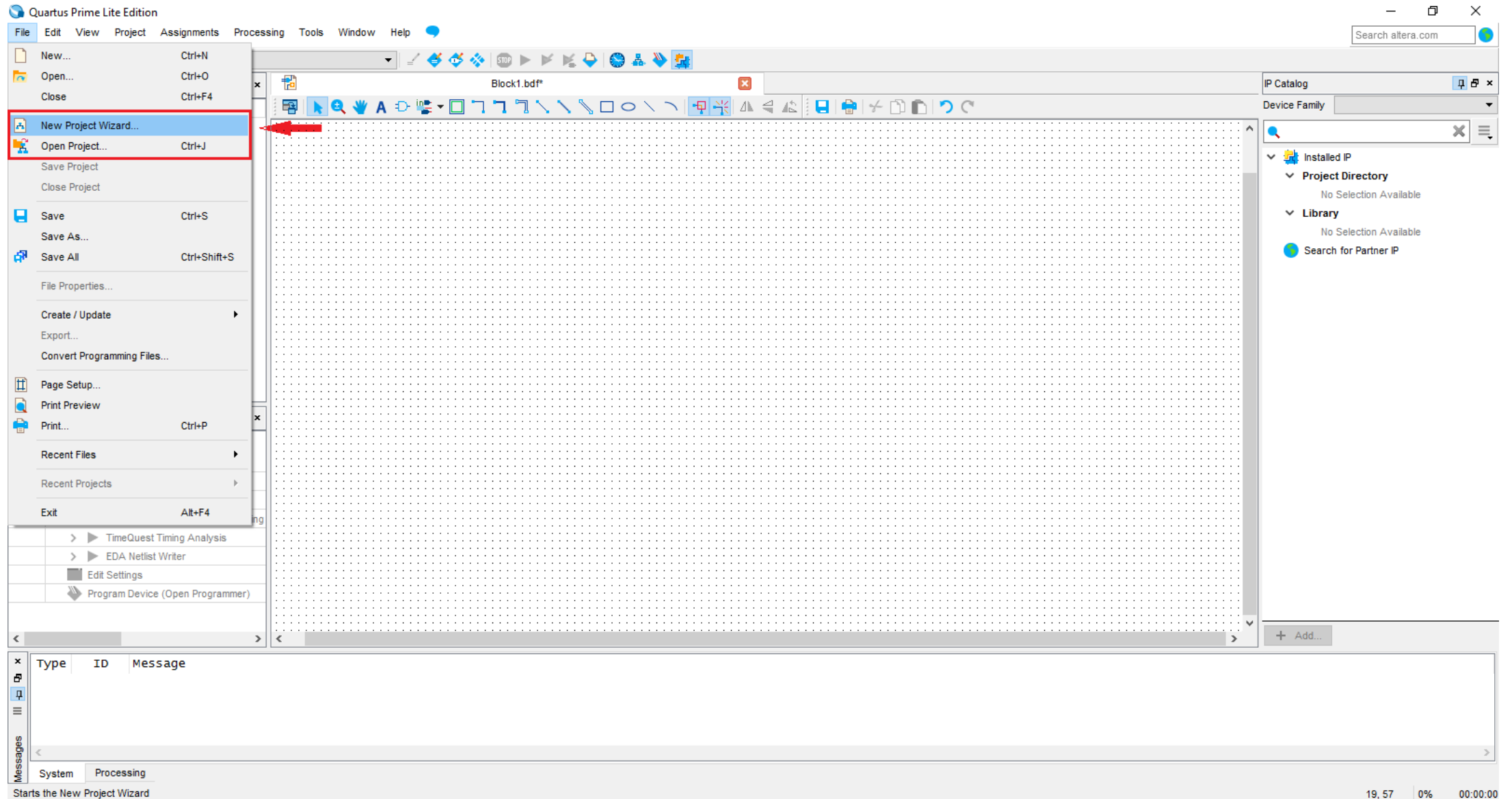
- Add To Executables

# Add Modelsim To Executables (Manual)

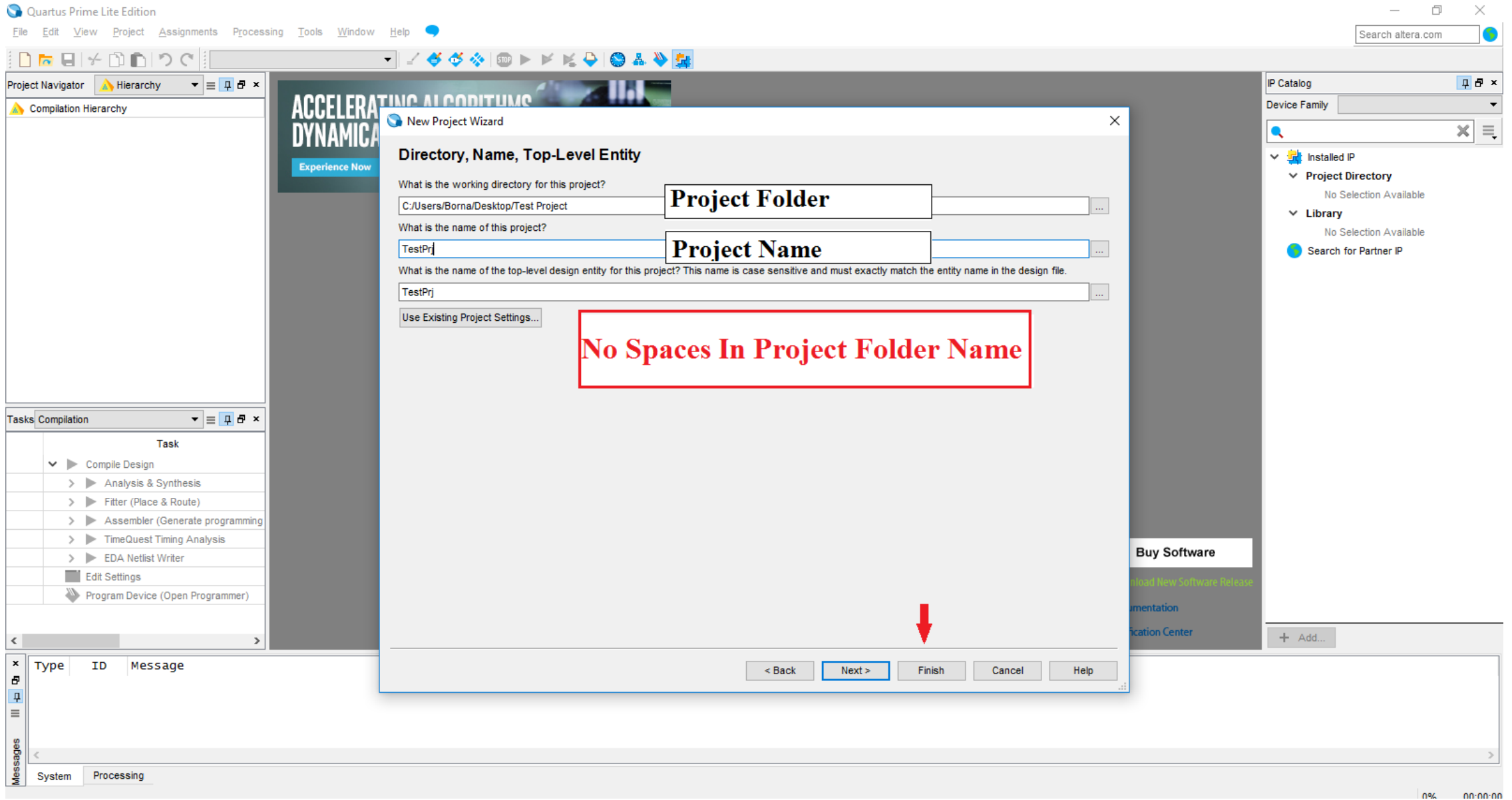
- Tools => Options => EDA Tool Options
- Add ModelSim-Installation-Path/bin to Modelsim-Altera



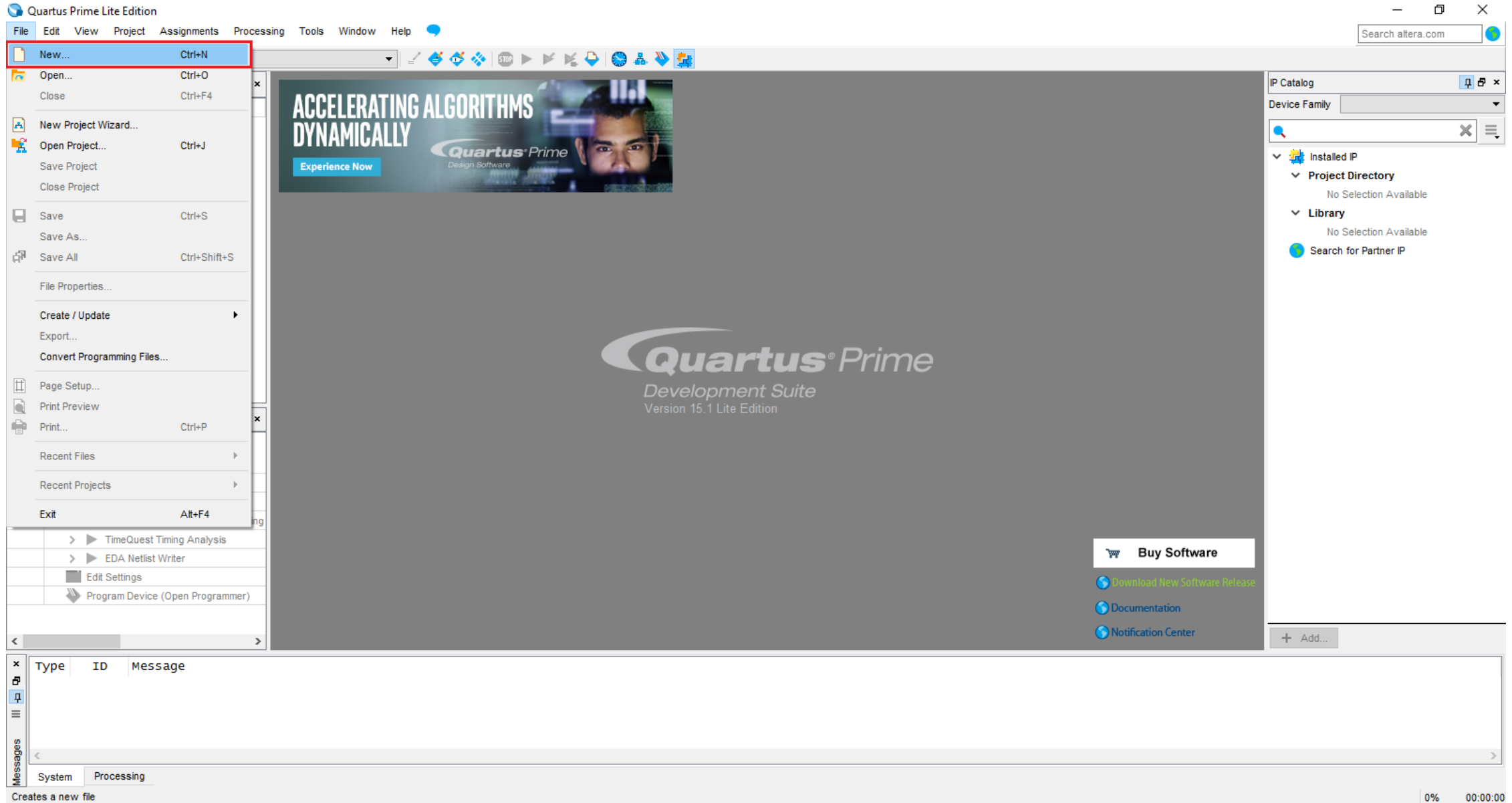
# Open A Project



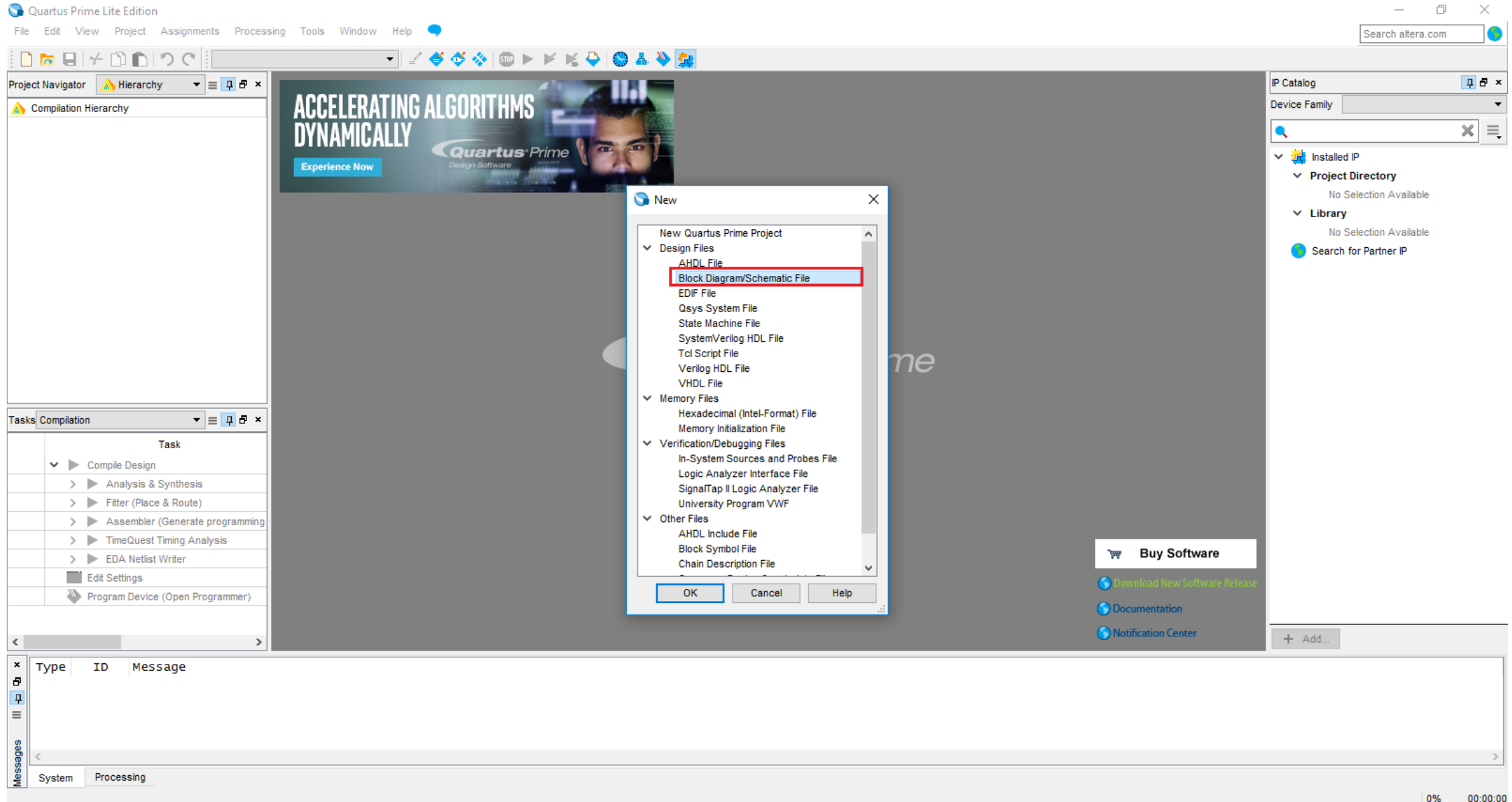
# Project Wizard



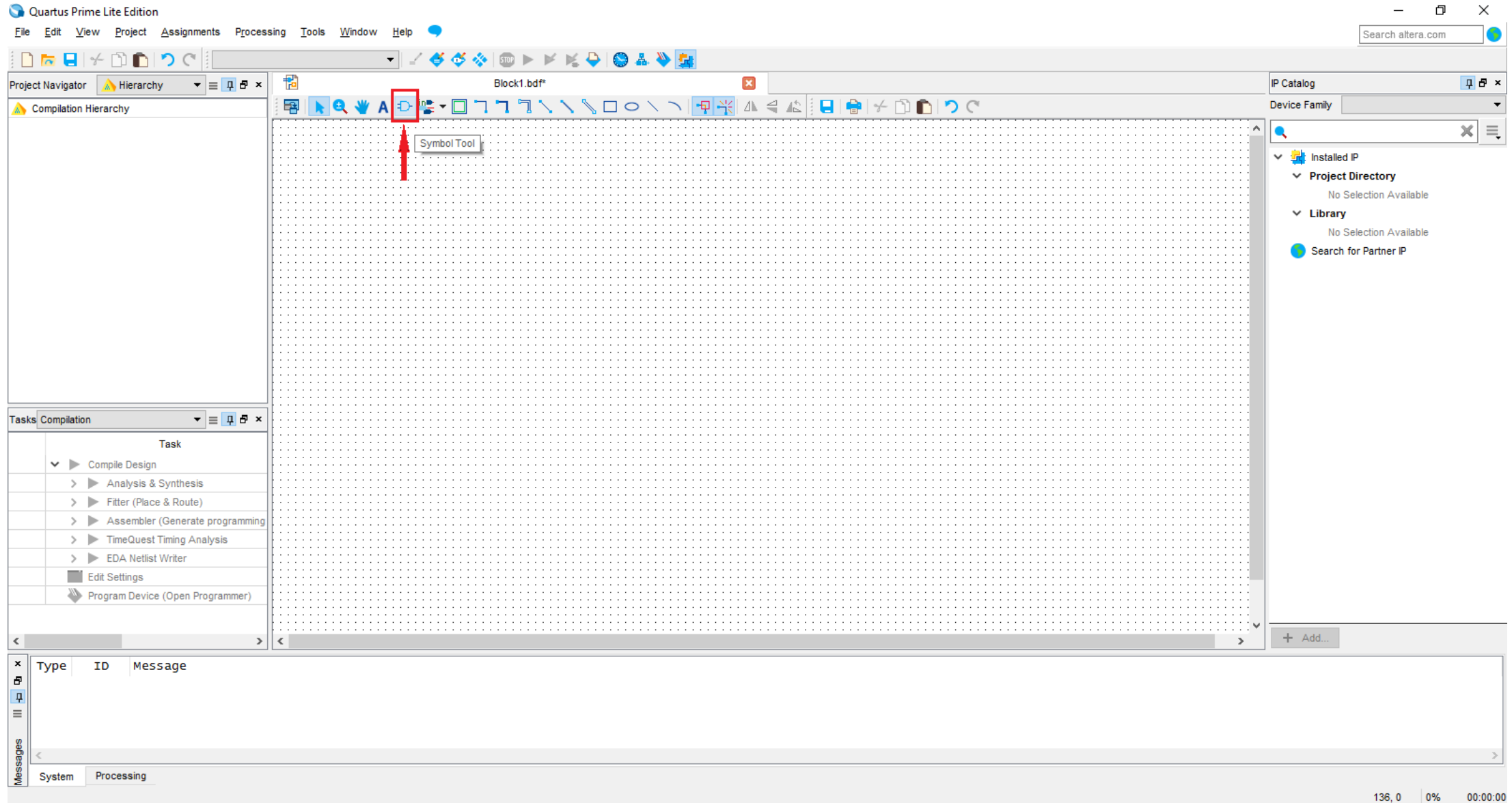
# Open Block Diagram / Schematic File



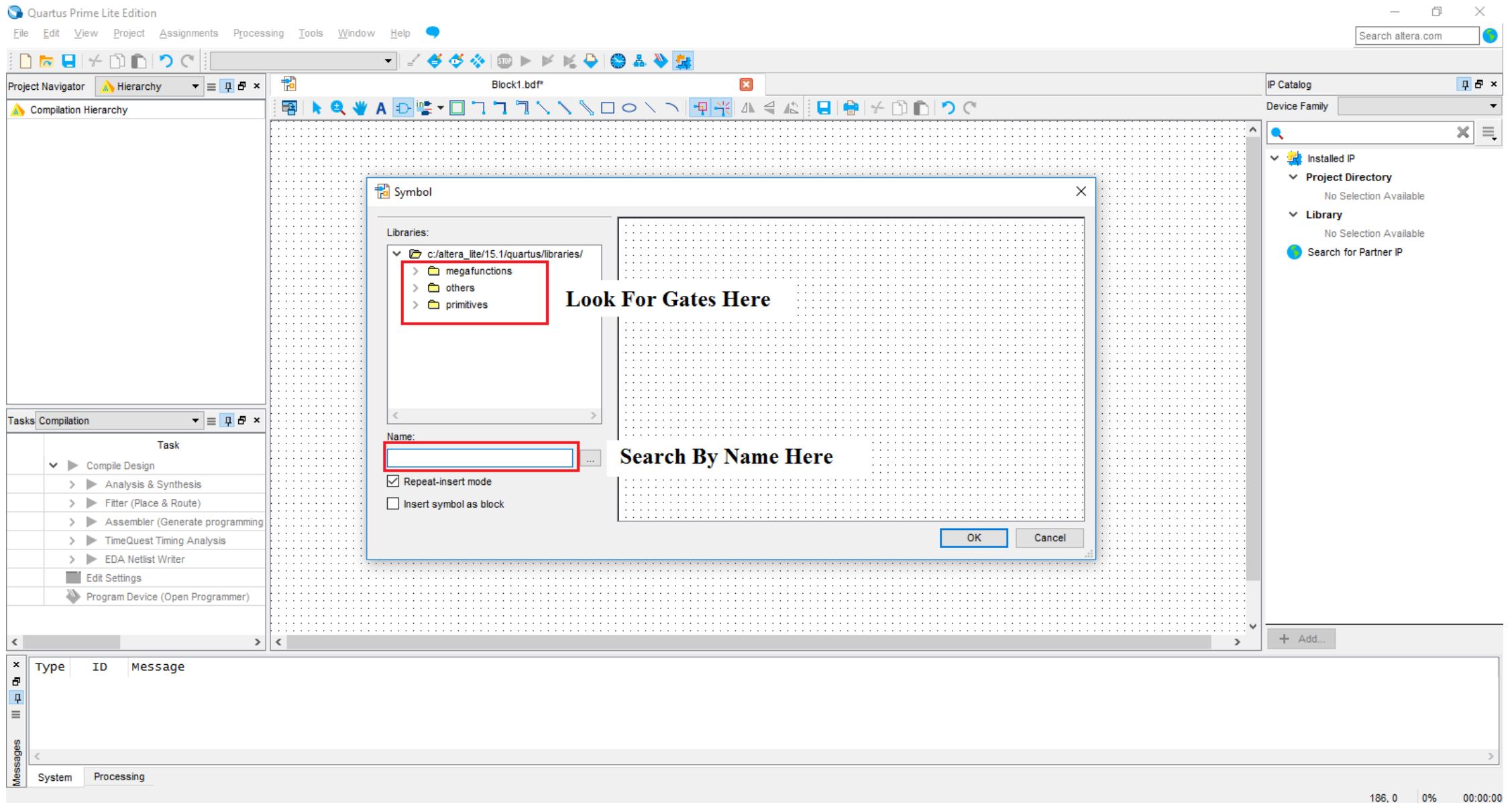
# Open Block Diagram / Schematic File



# Insert Modules & Symbols

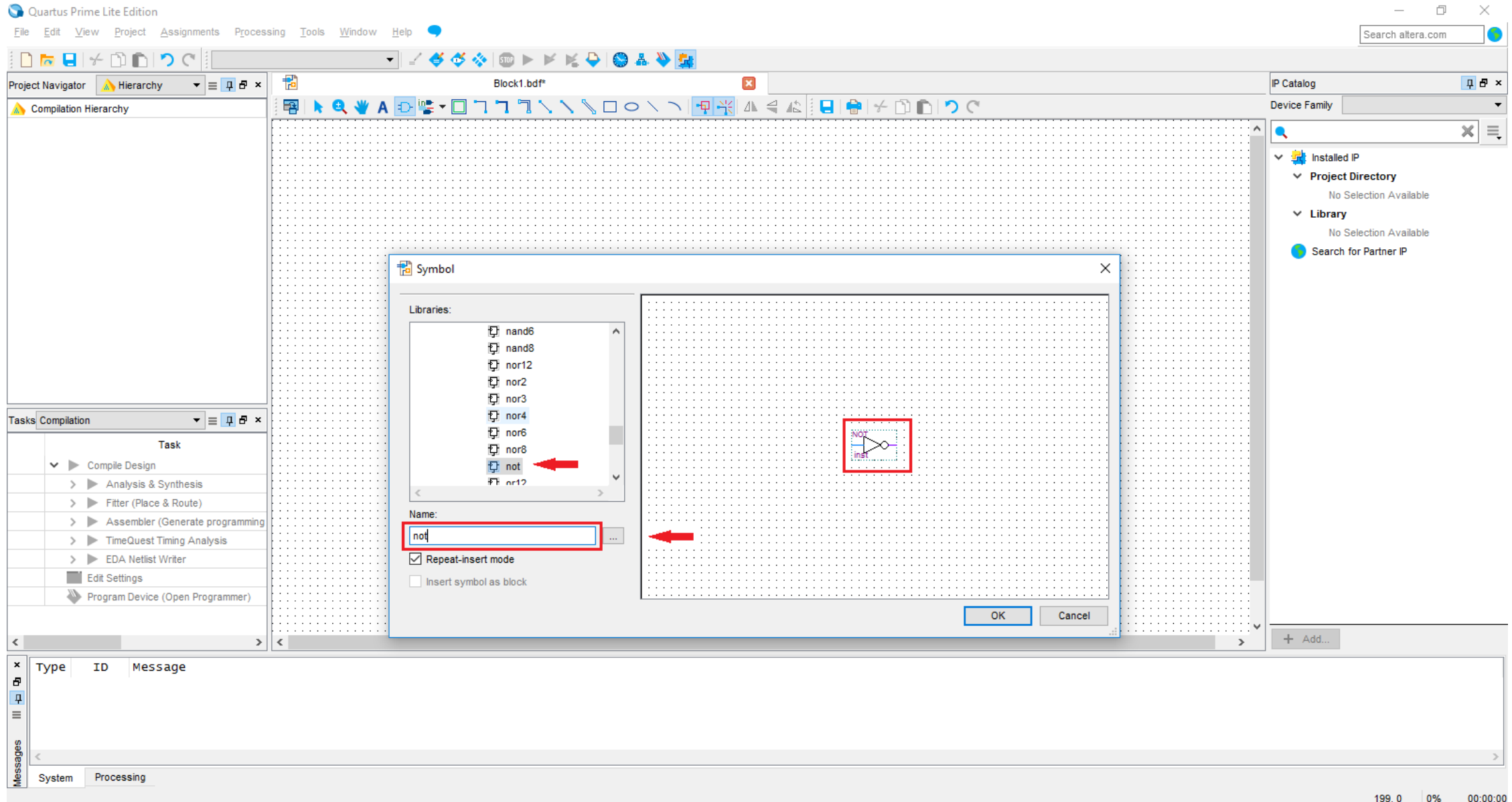


# Insert Modules & Symbols

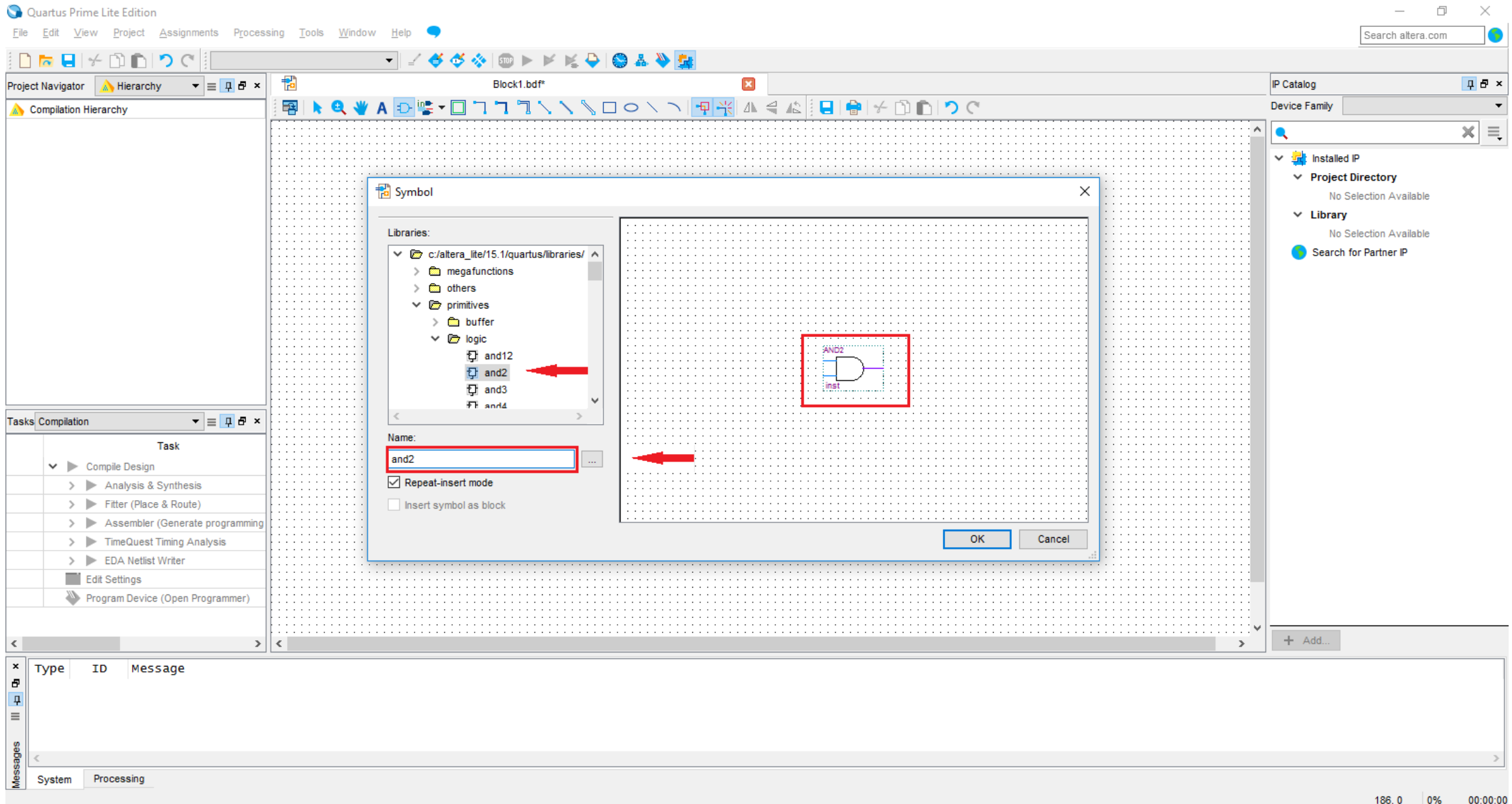




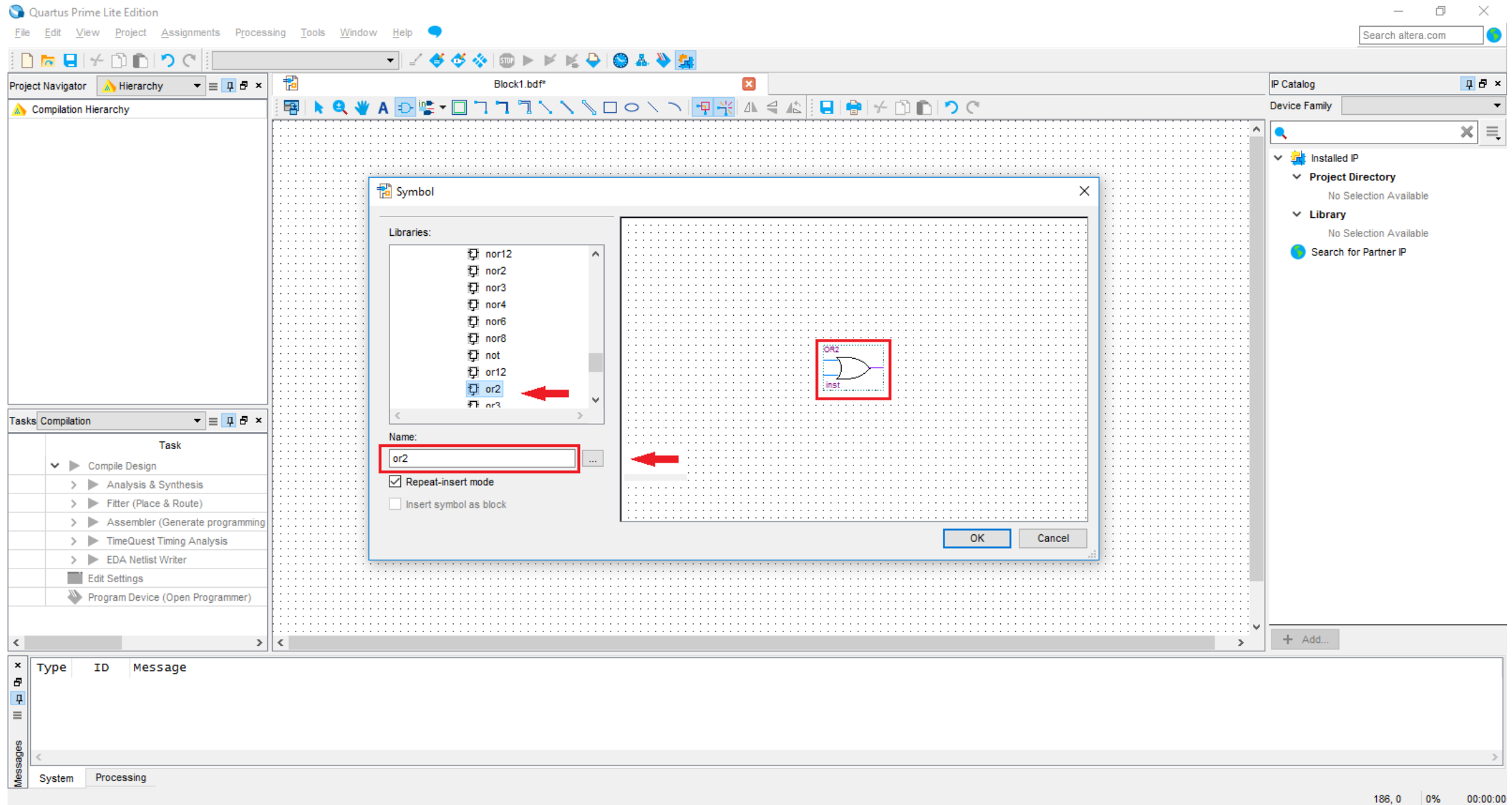
# Example: Not



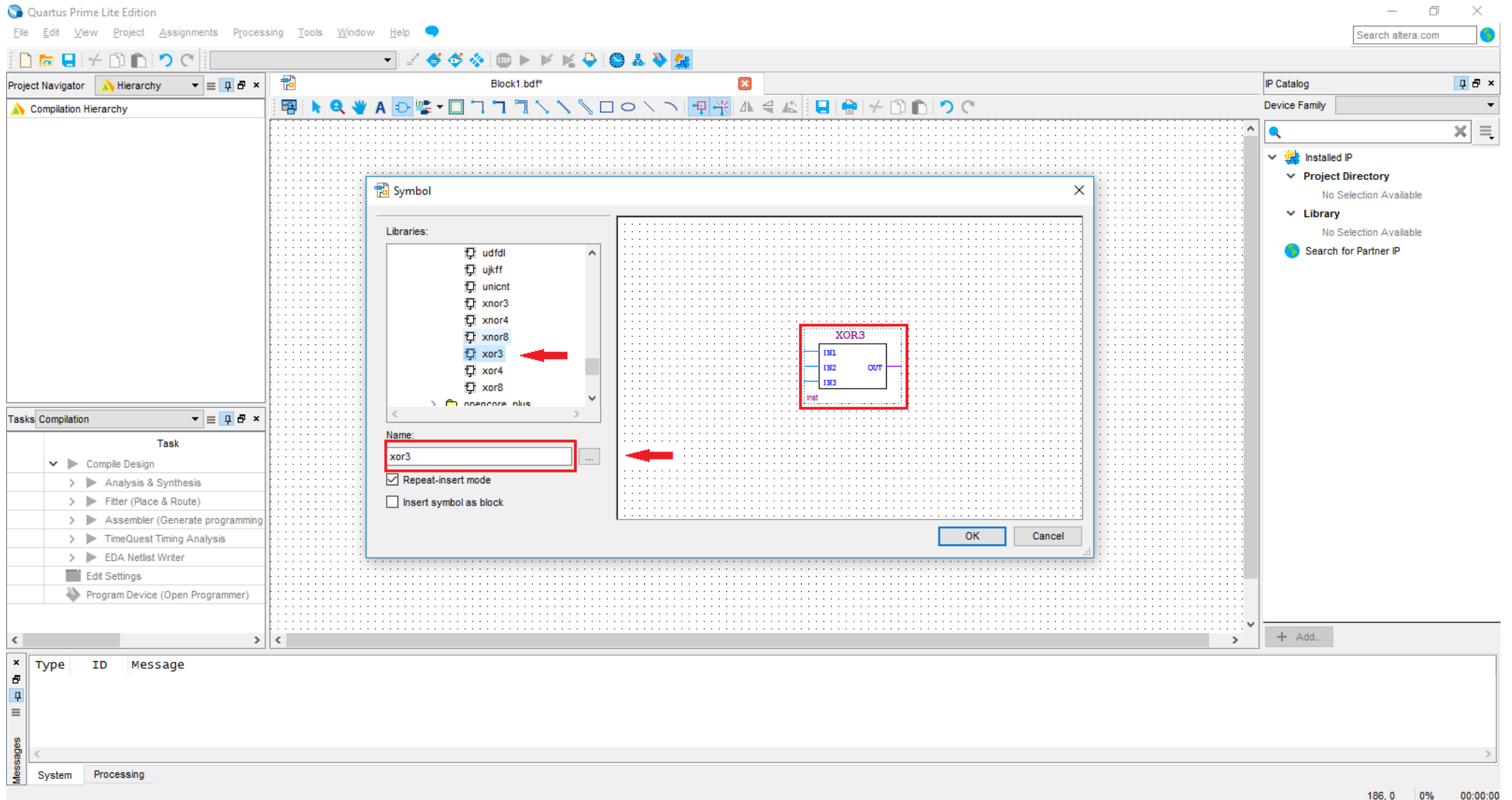
# Example: 2 Input AND (and2)



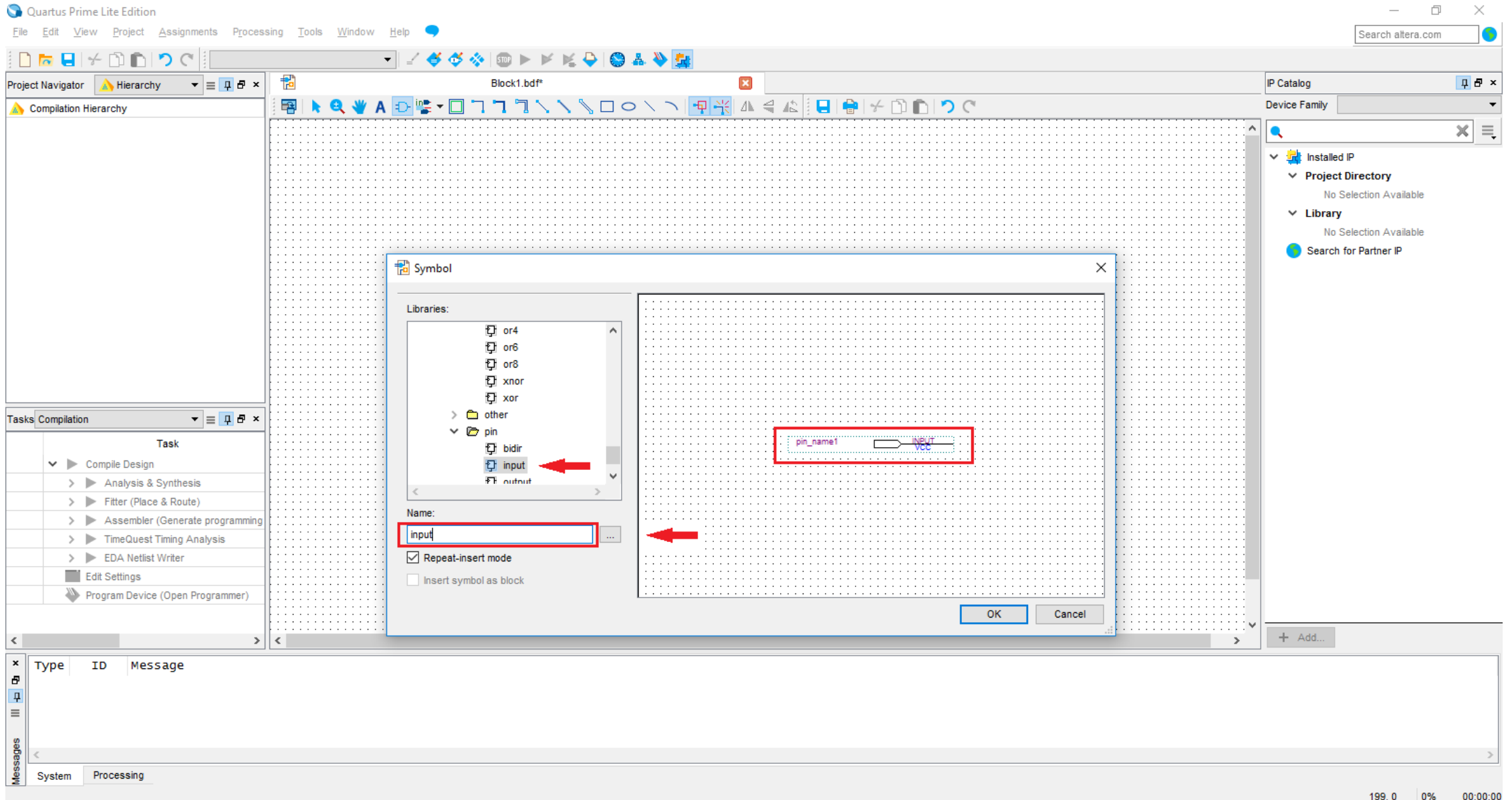
# Example: 2 Input OR (or2)



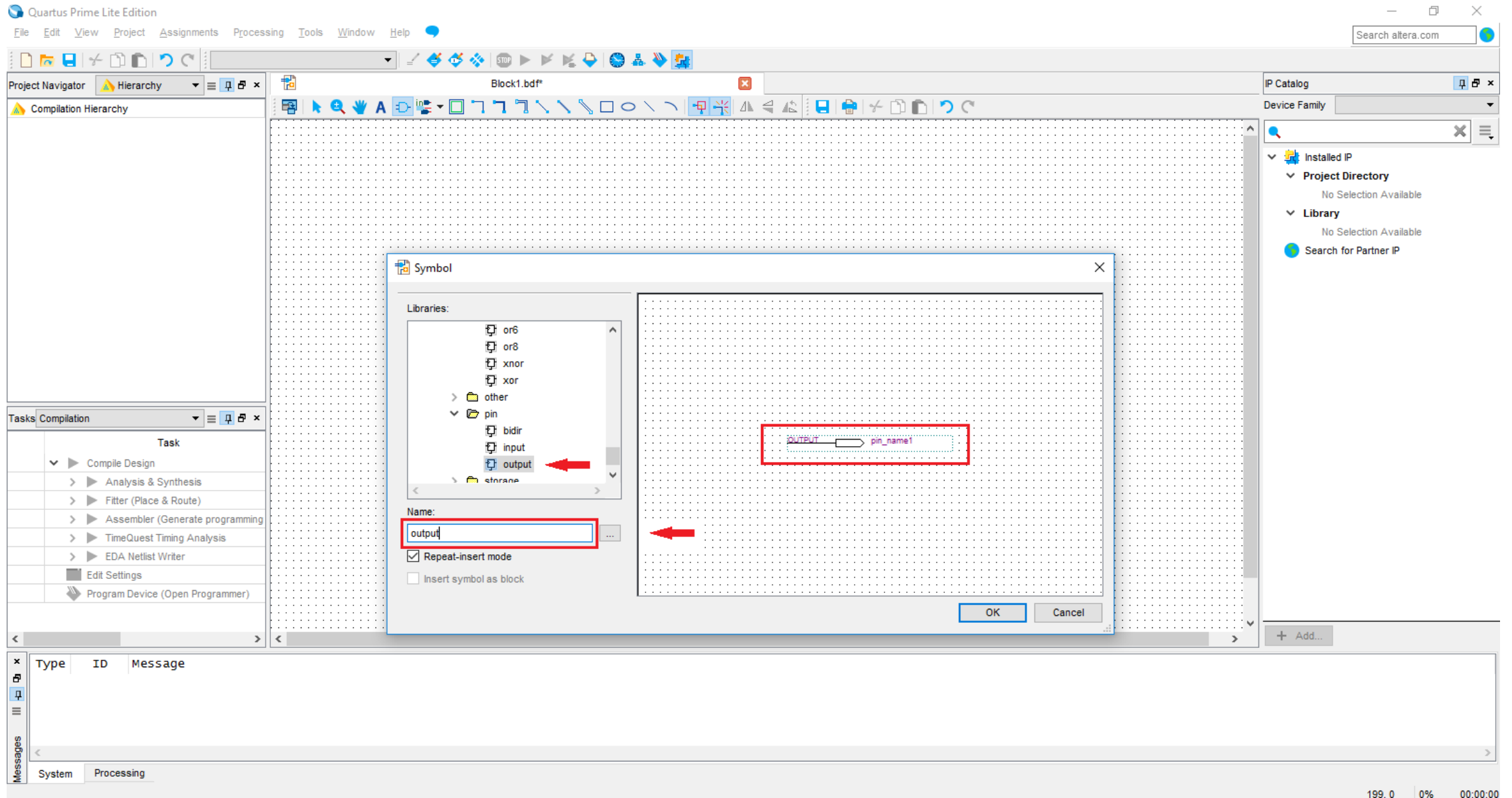
# Example: 3 Input XOR (xor3)



# Example: Input



# Example: Output



# Example: Wiring

The screenshot displays the Quartus Prime Lite Edition software interface. The main workspace shows a wiring diagram titled "Block1.bdf". The diagram features four input buffers labeled A, B, C, and D, each connected to a VCC source. The outputs of these buffers are connected to two AND gates, labeled inst1 and inst2. A red arrow points to a single-width wire connecting the outputs of the input buffers to the AND gates. The interface includes a Project Navigator on the left, a Tasks window at the bottom left, and an IP Catalog on the right. The status bar at the bottom indicates 229,0 0% 00:00:00.

Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy Block1.bdf

Compilation Hierarchy

Tasks Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Edit Settings
  - Program Device (Open Programmer)

IP Catalog

Device Family

Installed IP

- Project Directory
  - No Selection Available
- Library
  - No Selection Available
- Search for Partner IP

Single Width Wire

A B C D

inst1 inst2

229,0 0% 00:00:00

# Example: Wiring (Bus)

The screenshot displays the Quartus Prime Lite Edition interface. The main workspace shows a schematic diagram titled "Multiple Width Wire (Bus)". The diagram illustrates a bus connection between two 4-bit signals, A[3:0] and O[3:0]. A red box highlights the input signal A[3:0], and a green box highlights the output signal O[3:0]. A red text overlay in the center of the workspace reads "Bus Widths Should Always Match". The diagram includes a 4-bit bus labeled "input[3:0]" and a 4-bit bus labeled "output[3:0]". The interface also shows the Project Navigator, IP Catalog, and Tasks panels.

Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy

Compilation Hierarchy

Block1.bdf\*

Multiple Width Wire (Bus)

Bus Widths Should Always Match

Tasks Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

IP Catalog

Device Family

Installed IP

- Project Directory
  - No Selection Available
- Library
  - No Selection Available
- Search for Partner IP

Messages

Type	ID	Message
System		Processing

224, 0 0% 00:00:00



# Example: Connecting By Wire

The screenshot displays the Quartus Prime Lite Edition software interface. The main workspace shows a logic design titled "Connection By Wire" on a grid background. The design includes two input blocks labeled "A" and "B", each with a "VCC" pin. These inputs are connected to the inputs of an "AND2" block (labeled "inst"). The output of the "AND2" block is connected to an "OUTPUT" block, which is labeled "Res".

The interface includes several panels:

- Project Navigator:** Shows the "Compilation Hierarchy" and "Tasks" sections.
- Tasks:** Lists compilation tasks such as "Compile Design", "Analysis & Synthesis", "Fitter (Place & Route)", "Assembler (Generate programming)", "TimeQuest Timing Analysis", "EDA Netlist Writer", "Edit Settings", and "Program Device (Open Programmer)".
- IP Catalog:** Shows the "Device Family" and "Search for Partner IP" options.
- Messages:** A panel at the bottom left showing "Type", "ID", and "Message" columns.

The status bar at the bottom right indicates "195, 80 | 0% | 00:00:00".

# Example: Connecting By Name

Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator Hierarchy Block1.bdf\*

Compilation Hierarchy

Tasks Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Edit Settings
  - Program Device (Open Programmer)

Connecting By Name

In1 In2 In3[3:0]

A B C[3:0]

AND6

Res

Out

IP Catalog

Device Family

Installed IP

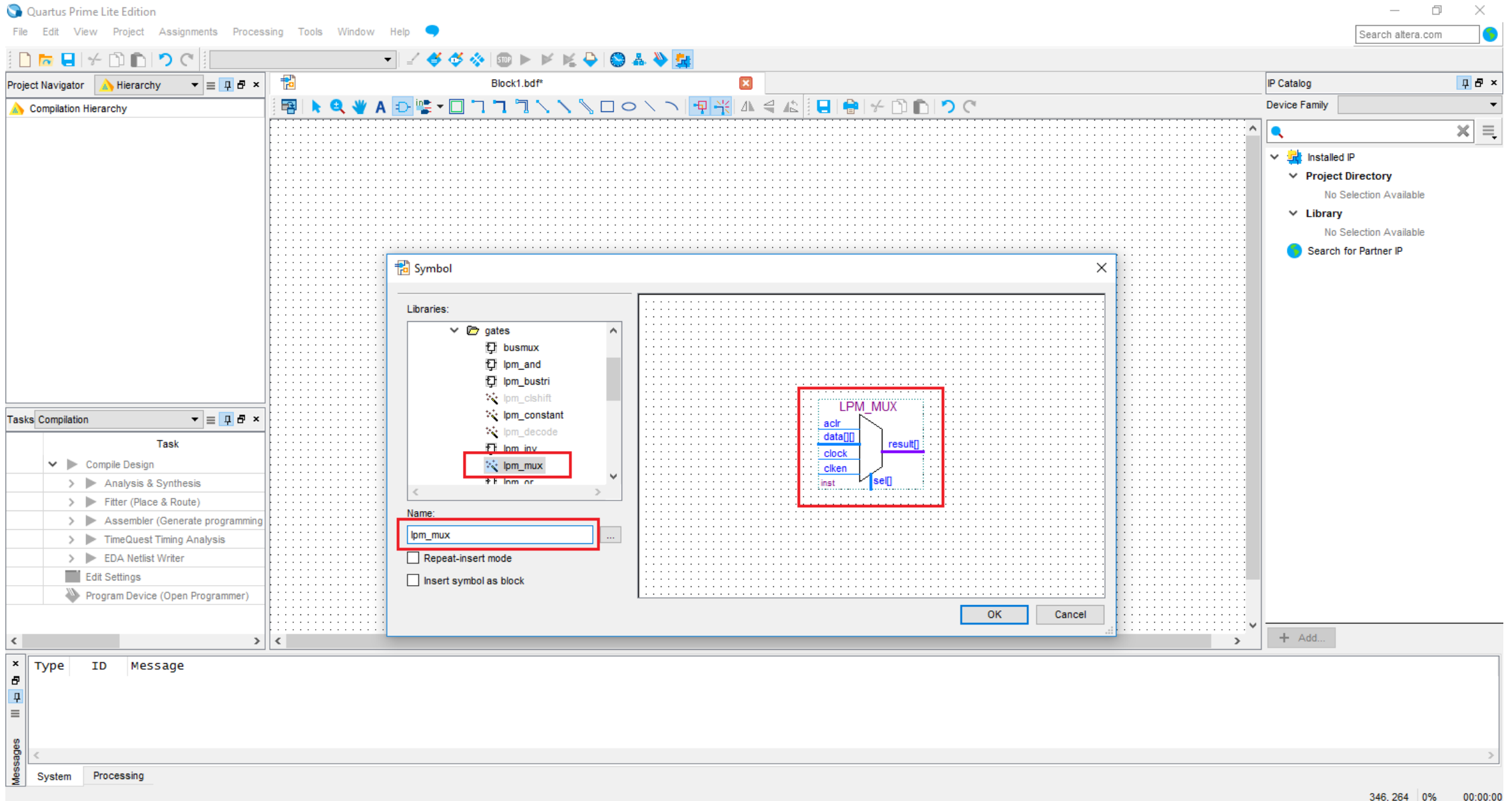
- Project Directory
  - No Selection Available
- Library
  - No Selection Available
- Search for Partner IP

Messages

Type	ID	Message
System		Processing

367,153 0% 00:00:00

# Example: Multiplexer (lpm Family)



# Example: Multiplexer (lpm Family)

The screenshot displays the Quartus Prime Lite Edition interface. The main workspace shows a block diagram with an LPM\_MUX block. A red arrow points to the parameters table for this block.

Parameter	Value
LPM_PIPELINE	
LPM_SIZE	
LPM_WIDTH	
LPM_WIDTHS	CEIL(LOG2(LPM_SIZE))

The LPM\_MUX block has the following ports: `aclr`, `data[]`, `clock`, `clken`, `rst`, and `result[]`.

The left sidebar contains the Project Navigator, Tasks (Compilation), and Messages panels. The right sidebar contains the IP Catalog and Device Family selection.

System Processing

341,114 0% 00:00:00

# Example: Multiplexer (lpm Family)

The screenshot displays the Quartus Prime Lite Edition interface. The main workspace shows a grid with a red arrow pointing to the 'Parameter' tab of the 'Symbol Properties' dialog box. The dialog box contains a table with the following data:

	Name	Value	Type	Description
1	LPM_PIPELINE			Output latency in clock cycles - requires us
2	LPM_SIZE			Number of inputs per MUX, any integer > 1
3	LPM_WIDTH			Number of MUXes, any integer > 0
4	LPM_WIDTHS	CEIL(LOG2(LPM_SIZE))		Width of sel[] port
5	<NEW>			

The interface also shows the Project Navigator on the left, the Tasks pane with 'Compile Design' selected, and the IP Catalog on the right. The status bar at the bottom indicates 'System' and 'Processing' modes.

# Example: Multiplexer (lpm Family)

The screenshot shows the Quartus Prime Lite Edition interface. The main workspace displays a grid with a block symbol. A red arrow points to the 'Symbol Properties' dialog box, which is open and showing the 'Parameter' tab. The dialog box contains a table with parameters for the Multiplexer block.

Name	Value	Type	Description
1 LPM_PIPELINE			Output latency in clock cycles - requires us
2 LPM_SIZE	32		Number of inputs per MUX, any integer > 1
3 LPM_WIDTH			Number of MUXes, any integer > 0
4 LPM_WIDTHS	CEIL(LOG2(LPM_SIZE))		Width of sel[] port
5 <NEW>			

The 'LPM\_SIZE' parameter is highlighted with a red box, and its value '32' is also highlighted. The 'Description' for 'LPM\_SIZE' is 'Number of inputs per MUX, any integer > 1'. The 'OK' button is highlighted with a blue box.

The interface also shows the 'Project Navigator' on the left, the 'Tasks' panel at the bottom left, and the 'IP Catalog' on the right. The status bar at the bottom indicates 'System' and 'Processing' modes, with a progress bar showing 0% completion.

The screenshot shows the Quartus Prime Lite Edition software interface. The main workspace displays a schematic diagram of a block labeled "Block1.bdf\*". A red arrow points to the "Symbol Properties" dialog box, which is open and showing the "Parameter" tab. The dialog box contains a table with the following parameters:

Name	Value	Type	Description
1 LPM_PIPELINE			Output latency in clock cycles - requires us
2 LPM_SIZE	32		Number of inputs per MUX, any integer > 1
3 LPM_WIDTH			Number of MUXes, any integer > 0
4 LPM_WIDTHS	1		Width of sel[] port
5 <NEW>			

The "LPM\_WIDTH" parameter is highlighted with a red box, and its value is being set to 8 from a dropdown menu. The "LPM\_WIDTHS" parameter is also highlighted with a red box, and its value is being set to 1 from a dropdown menu. The "Symbol Properties" dialog box has "OK", "Cancel", and "Help" buttons at the bottom.

# Example: Multiplexer (lpm Family)

Quartus Prime Lite Edition - C:/Users/Borna/Desktop/Test Project/TestPrj - TestPrj

File Edit View Project Assignments Processing Tools Window Help

TestPrj

Project Navigator Hierarchy

Entity: Instance

Cyclone IV E: AUTO

TestPrj

Block1.bdf\*

Parameter Value

LPM_PIPELINE	
LPM_SIZE	8
LPM_WIDTH	2
LPM_WIDTHS	CEIL(LOG2(LPM_SIZE))

IP Catalog

Installed IP

- Project Directory  
No Selection Available
- Library  
No Selection Available
- Search for Partner IP

Tasks Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Edit Settings
  - Program Device (Open Programmer)

Messages

Type ID Message

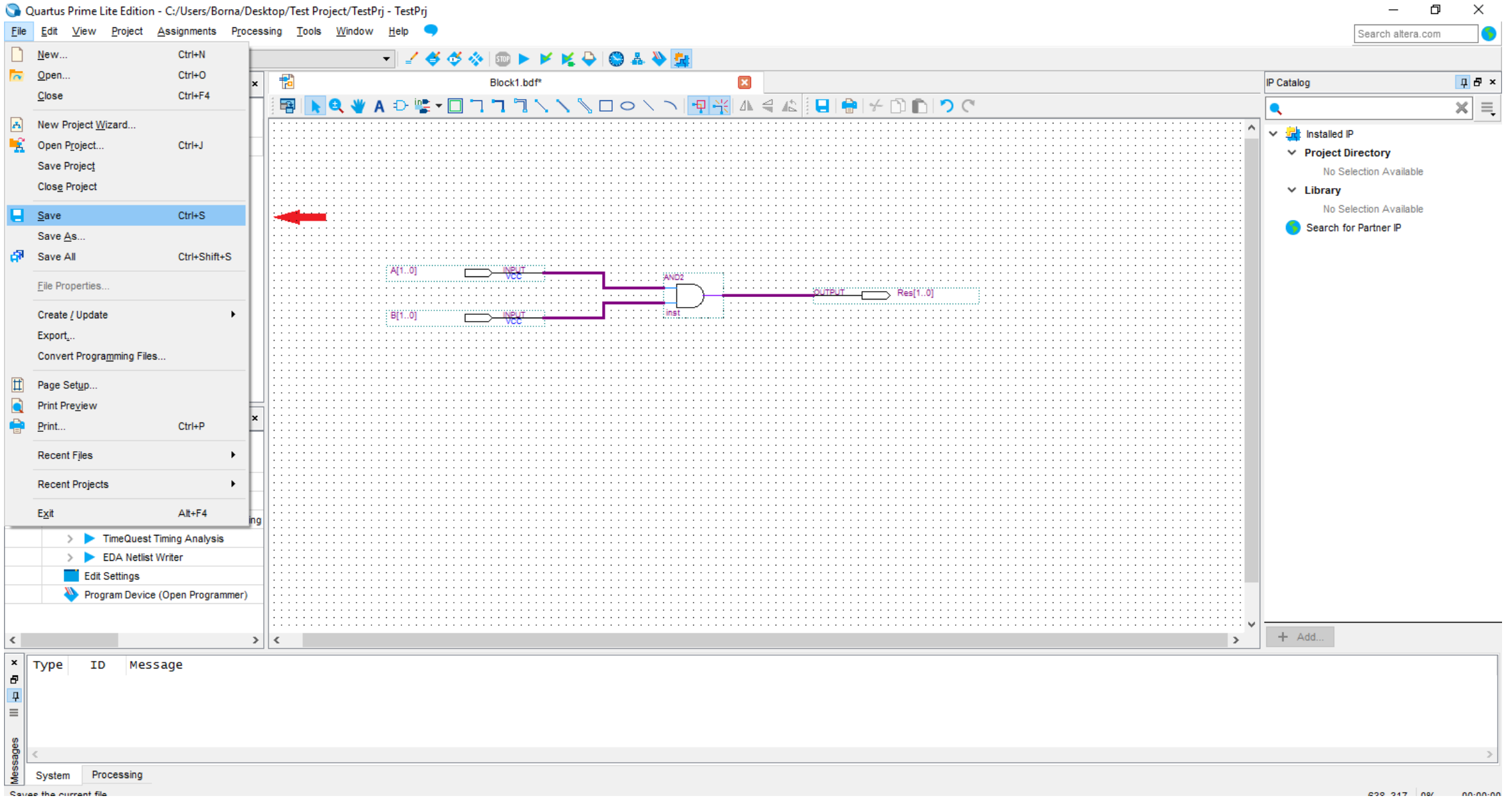
System Processing

575, 52 0% 00:00:00

The diagram illustrates an 8-to-1 multiplexer (LPM\_MUX) configuration in Quartus Prime Lite Edition. The multiplexer has 8 data inputs, labeled A[1..0] through H[1..0], each connected to a VCC source. These inputs are connected to internal multiplexer blocks (Muxin[7][1..0] through Muxin[0][1..0]). A 2-bit select input, Sel[2..0], is connected to the 'sel[]' port of the LPM\_MUX block. The output of the multiplexer, result[], is connected to a 2-bit output register, Res[2..0]. A parameter table on the right specifies the LPM\_PIPELINE, LPM\_SIZE (8), LPM\_WIDTH (2), and LPM\_WIDTHS (CEIL(LOG2(LPM\_SIZE))). The IP Catalog on the right shows no selection available for Project Directory or Library. The Tasks Compilation panel on the left lists tasks like Compile Design, Analysis & Synthesis, Fitter, Assembler, TimeQuest Timing Analysis, EDA Netlist Writer, Edit Settings, and Program Device. The Messages panel at the bottom shows System and Processing messages.

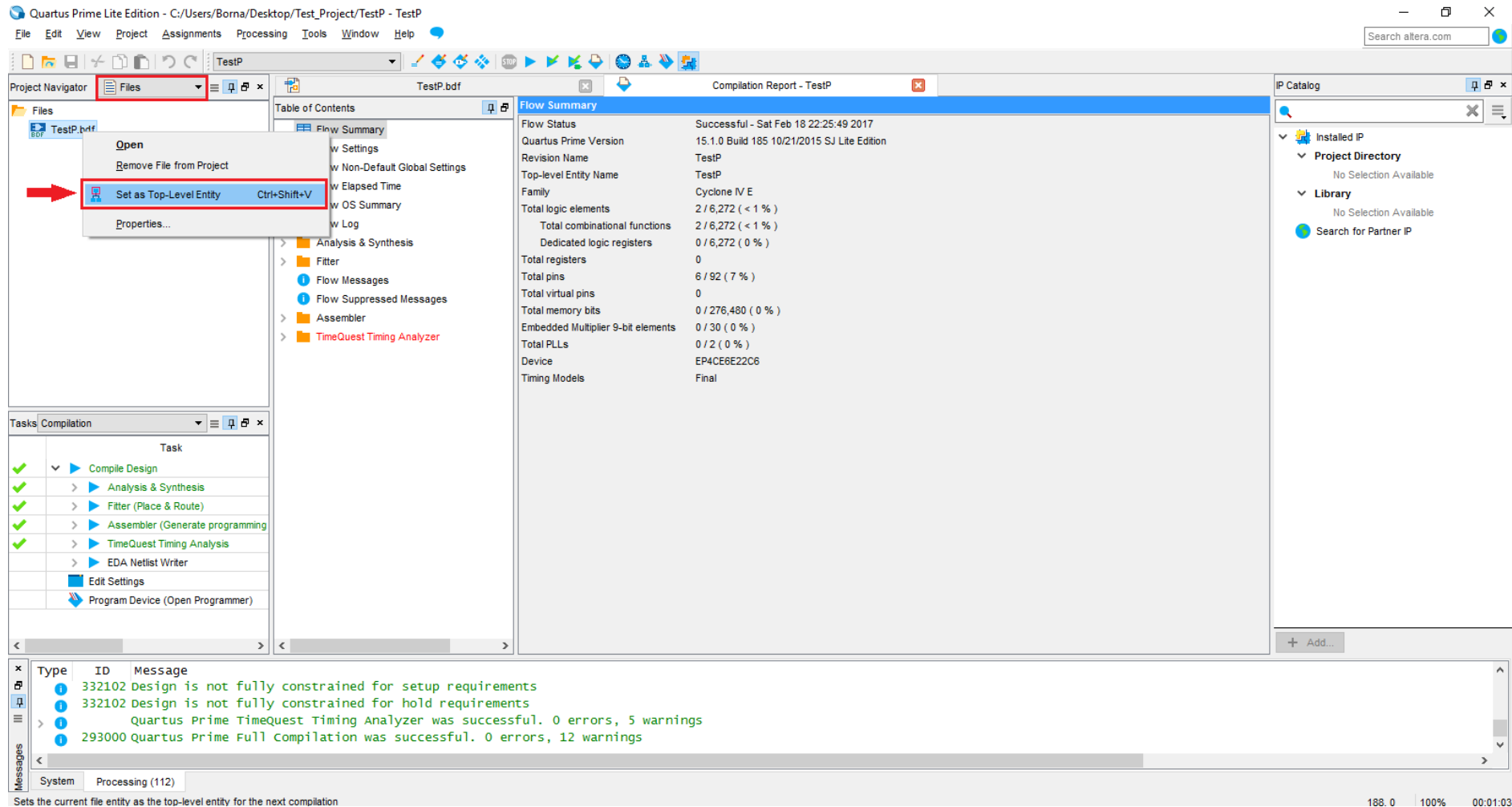


# Save Your Design (.bdf file)



# Compile Your Design

- Set Your Design as Top Level Entity



# Compile Your Design

The screenshot displays the Quartus Prime Lite Edition interface for a project named 'TestPrj'. A red arrow points to the 'Start Compilation' button (a blue play icon) in the top toolbar, with a tooltip that reads 'Start Compilation - Ctrl+L'. The main workspace shows a logic diagram with two 1-bit inputs, A[1..0] and B[1..0], each connected to a VCC source. These inputs are connected to the inputs of an AND2 gate. The output of the AND2 gate is connected to a 1-bit output, Res[1..0]. The left sidebar contains the 'Project Navigator' with a 'Hierarchy' view showing the project structure. Below it is the 'Tasks' panel, which lists various tasks under the 'Compile Design' category, including 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming)', 'TimeQuest Timing Analysis', 'EDA Netlist Writer', 'Edit Settings', and 'Program Device (Open Programmer)'. The right sidebar shows the 'IP Catalog' with sections for 'Installed IP', 'Project Directory', and 'Library'. The bottom status bar indicates 'Starts a new compilation' and shows progress information: '301, 4 | 0% | 00:00:00'.

Quartus Prime Lite Edition - C:/Users/Borna/Desktop/Test Project/TestPrj - TestPrj

File Edit View Project Assignments Processing Tools Window Help

TestPrj

Project Navigator

Hierarchy

Entity: Instance

Cyclone IV E: AUTO

TestPrj

Tasks

Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Edit Settings
  - Program Device (Open Programmer)

IP Catalog

Installed IP

- Project Directory
  - No Selection Available
- Library
  - No Selection Available
- Search for Partner IP

Starts a new compilation

301, 4 | 0% | 00:00:00

# Compile Your Design, After a While ...

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the 'Compilation Report - TestPrj' for 'TestPrj.bdf'. The report indicates a successful compilation on Saturday, February 18, 2017, at 21:58:32. The report includes details about the Quartus Prime version (15.1.0), the device (EP4CE6E22C6), and various resource usage statistics. The 'Messages' window at the bottom shows a list of messages, with the final message highlighted: '293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings'. A red arrow points to this message with the text 'Ignore Warnings'.

Quartus Prime Lite Edition - C:/Users/Borna/Desktop/Test Project/TestPrj - TestPrj

File Edit View Project Assignments Processing Tools Window Help

TestPrj

Project Navigator

Entity: Instance

Cyclone IV E: AUTO

TestPrj

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- TimeQuest Timing Analyzer

Flow Summary

Flow Status	Successful - Sat Feb 18 21:58:32 2017
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Lite Edition
Revision Name	TestPrj
Top-level Entity Name	TestPrj
Family	Cyclone IV E
Total logic elements	2 / 6,272 (< 1 %)
Total combinational functions	2 / 6,272 (< 1 %)
Dedicated logic registers	0 / 6,272 (0 %)
Total registers	0
Total pins	6 / 92 (7 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

Tasks/Compilation

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming)
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)

Messages

Type	ID	Message
Warning	332102	Design is not fully constrained for setup requirements
Warning	332102	Design is not fully constrained for hold requirements
Warning	293000	Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings
Warning	293000	Quartus Prime Full Compilation was successful. 0 errors, 12 warnings

System Processing (112)

375, 4 100% 00:01:26

Ignore Warnings

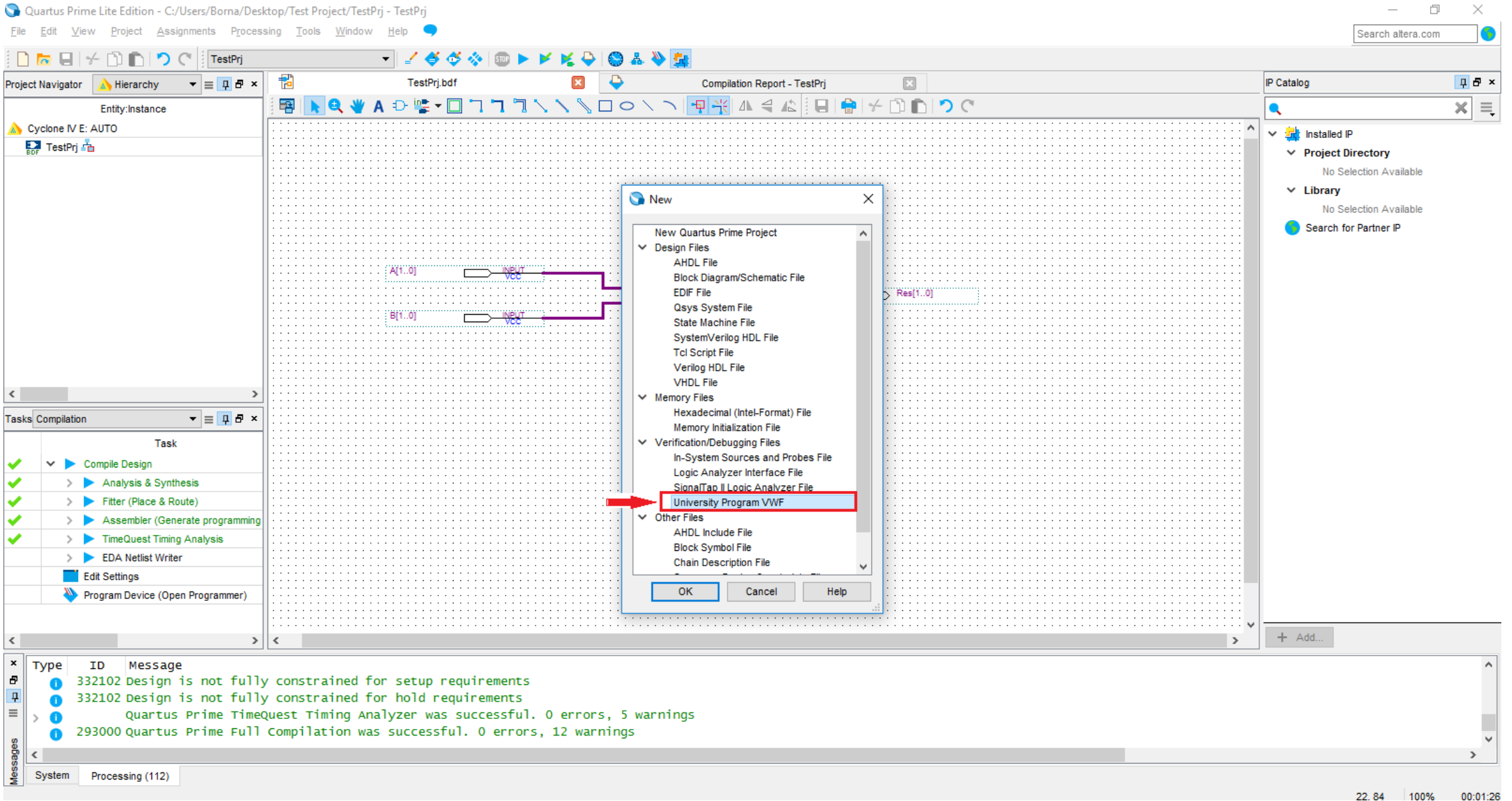
# Create a Waveform

The screenshot displays the Quartus Prime Lite Edition interface. The **File** menu is open, with the **New...** option highlighted. The main workspace shows a logic diagram with two 1-bit inputs, A[1..0] and B[1..0], each connected to a VCC source. These inputs are connected to the inputs of an AND2 gate. The output of the AND2 gate is connected to a 2-bit output, Res[1..0]. The Messages window at the bottom shows the following messages:

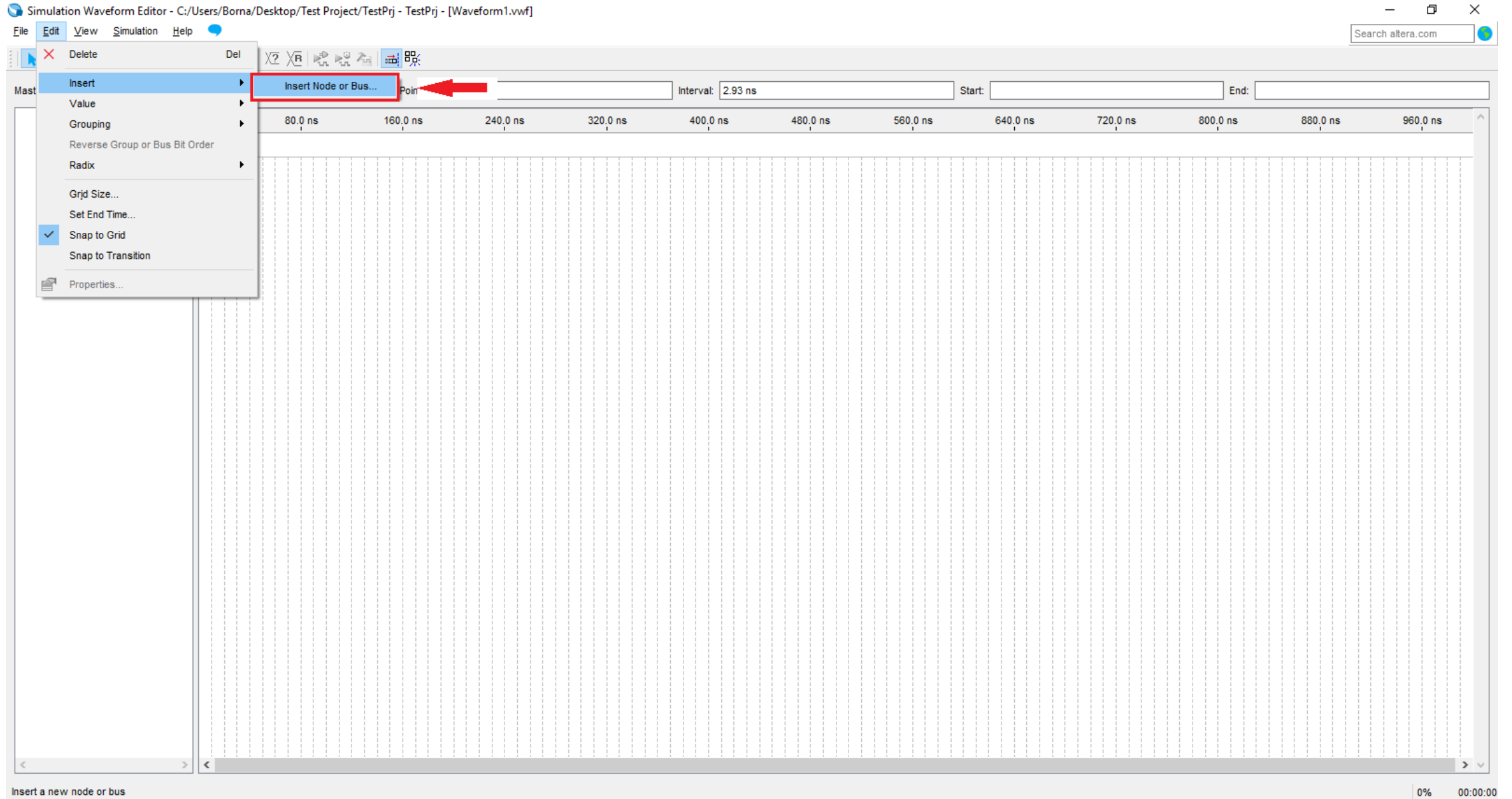
Type	ID	Message
Warning	332102	Design is not fully constrained for setup requirements
Warning	332102	Design is not fully constrained for hold requirements
Success		Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings
Success		Quartus Prime Full Compilation was successful. 0 errors, 12 warnings

The status bar at the bottom indicates "Creates a new file" and shows the project name "TestPrj", the file name "TestPrj.bdf", and the compilation report "Compilation Report - TestPrj". The IP Catalog on the right shows "Installed IP" with "Project Directory" and "Library" both having "No Selection Available". The search bar at the top right contains "Search altera.com".

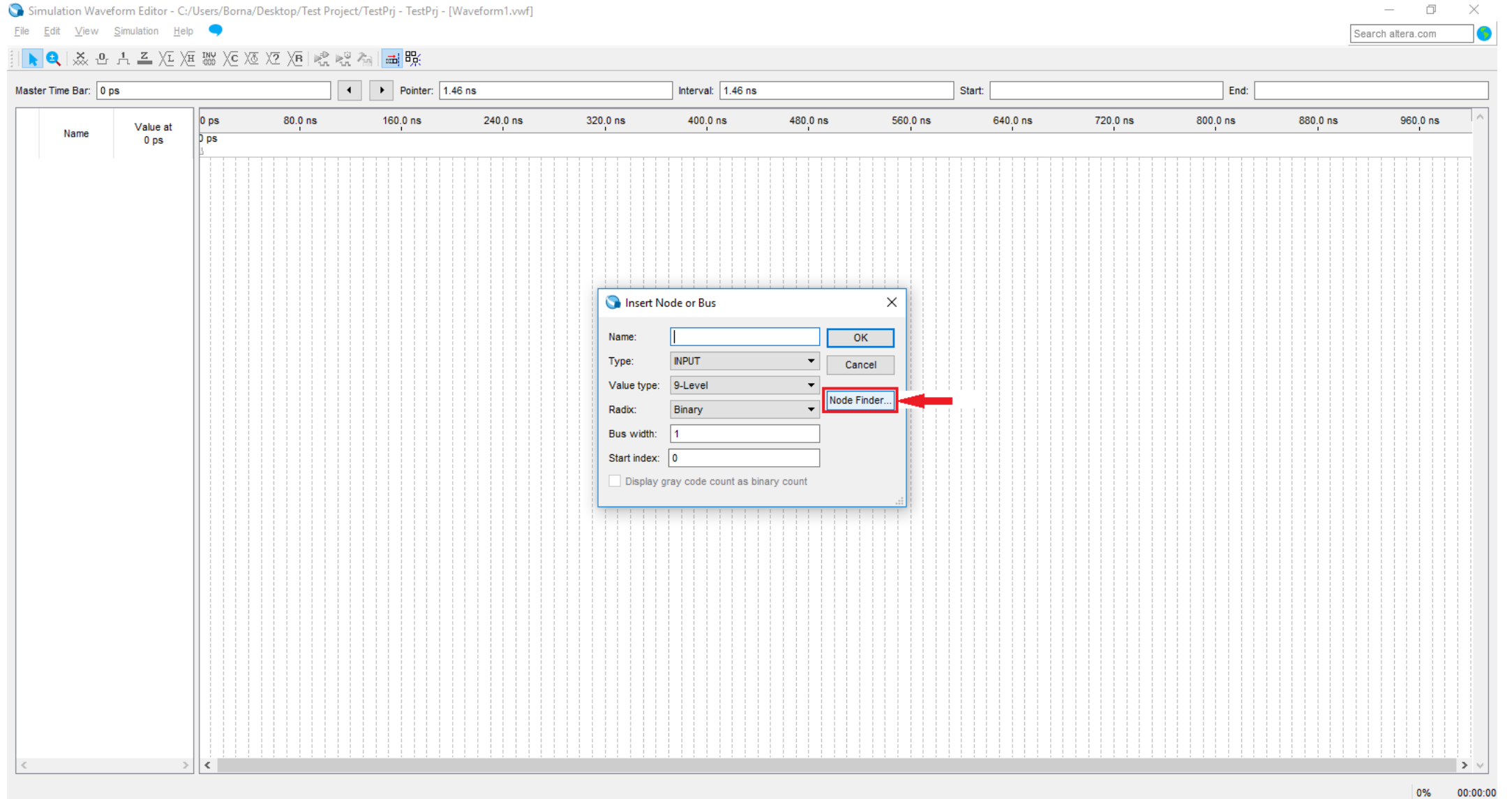
# Create a Waveform



# Add Signals & Buses

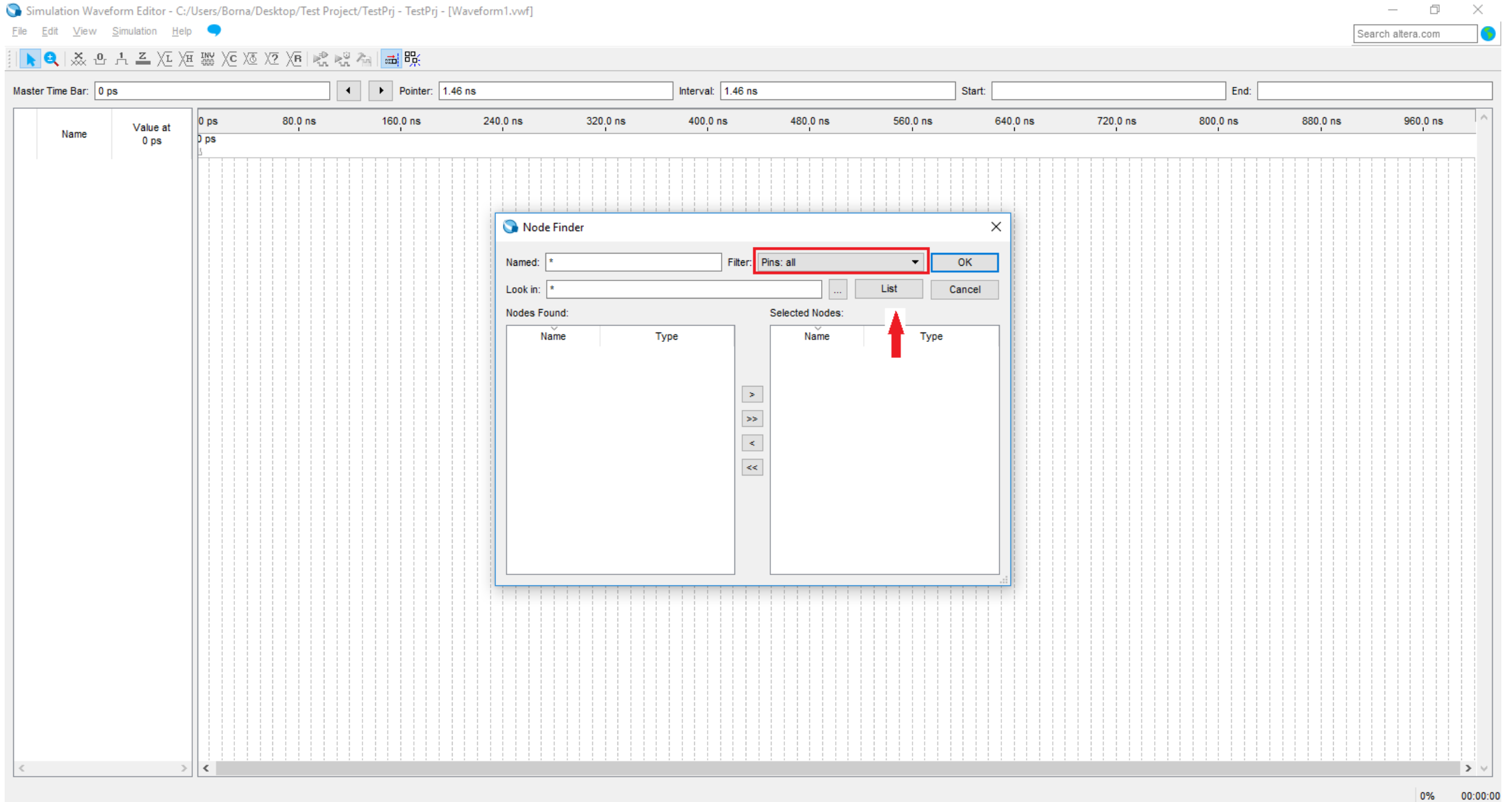


# Add Signals & Buses





# Add Signals & Buses



# Add Signals & Buses

Simulation Waveform Editor - C:/Users/Borna/Desktop/Test Project/TestPrj - TestPrj - [Waveform1.vwf]

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 1.46 ns Interval: 1.46 ns Start: End:

0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns

Name Value at 0 ps

Node Finder

Named: \* Filter: Pins: all OK

Look in: \* List Cancel

Nodes Found:

Name	Type
in A	Input Group
in A[0]	Input
in A[1]	Input
in B	Input Group
in B[0]	Input
in B[1]	Input
out Res	Output Group
out Res[0]	Output
out Res[1]	Output

> >> < <<

Selected Nodes:

Name	Type
------	------

0% 00:00:00

# Add Signals & Buses

Simulation Waveform Editor - C:/Users/Borna/Desktop/Test Project/TestPrj - TestPrj - [Waveform1.vwf]

File Edit View Simulation Help

Master Time Bar: 0 ps Pointer: 1.46 ns Interval: 1.46 ns Start: End:

0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns

Name Value at 0 ps

Node Finder

Named: \* Filter: Pins: all OK

Look in: \* List Cancel

Nodes Found:

Name	Type
in A	Input Group
in A[0]	Input
in A[1]	Input
in B	Input Group
in B[0]	Input
in B[1]	Input
out Res	Output Group
out Res[0]	Output
out Res[1]	Output

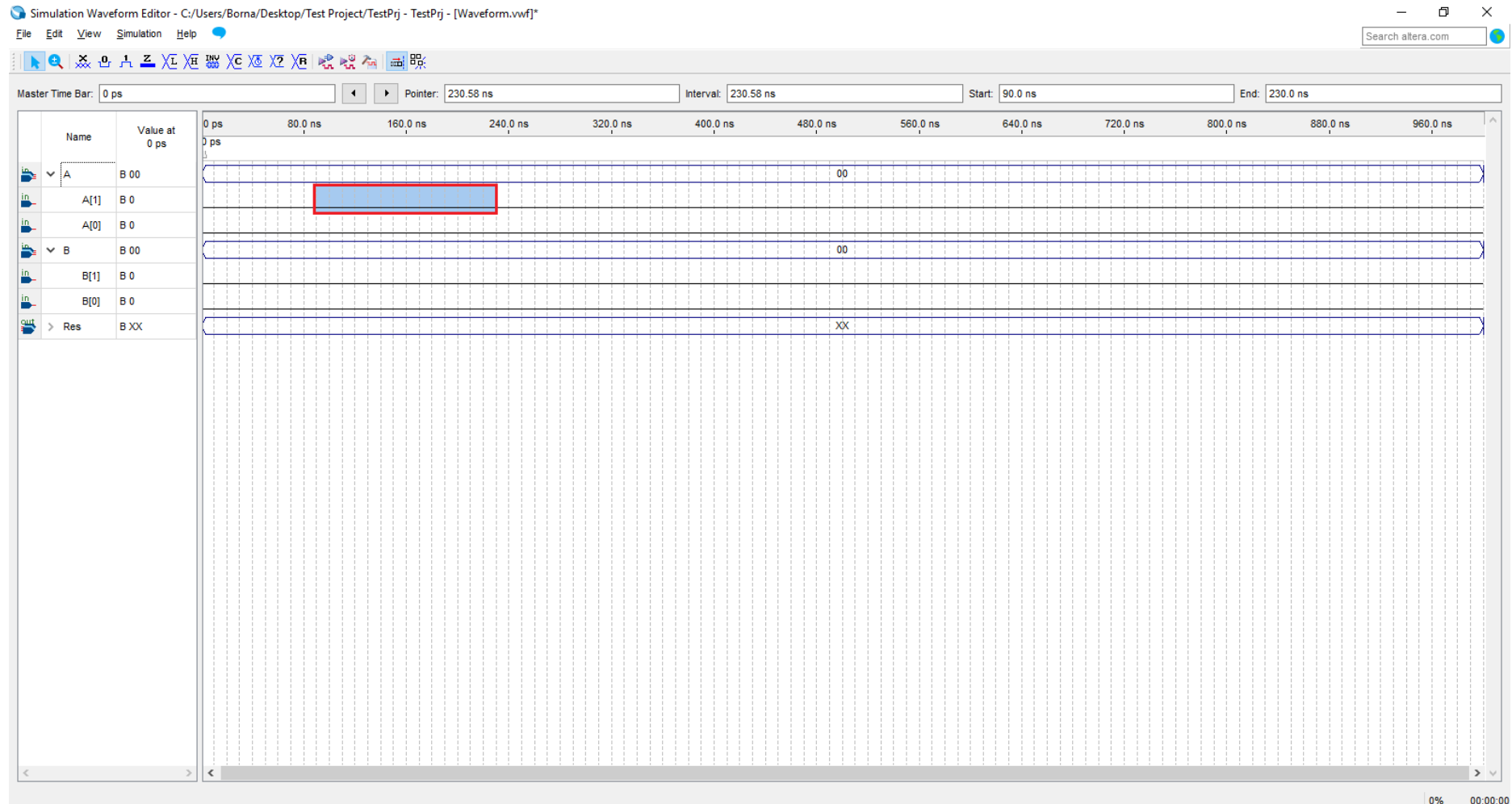
Selected Nodes:

Name	Type
in A	Input Group
in A[0]	Input
in A[1]	Input
in B	Input Group
in B[0]	Input
in B[1]	Input
out Res	Output Group
out Res[0]	Output
out Res[1]	Output

0% 00:00:00

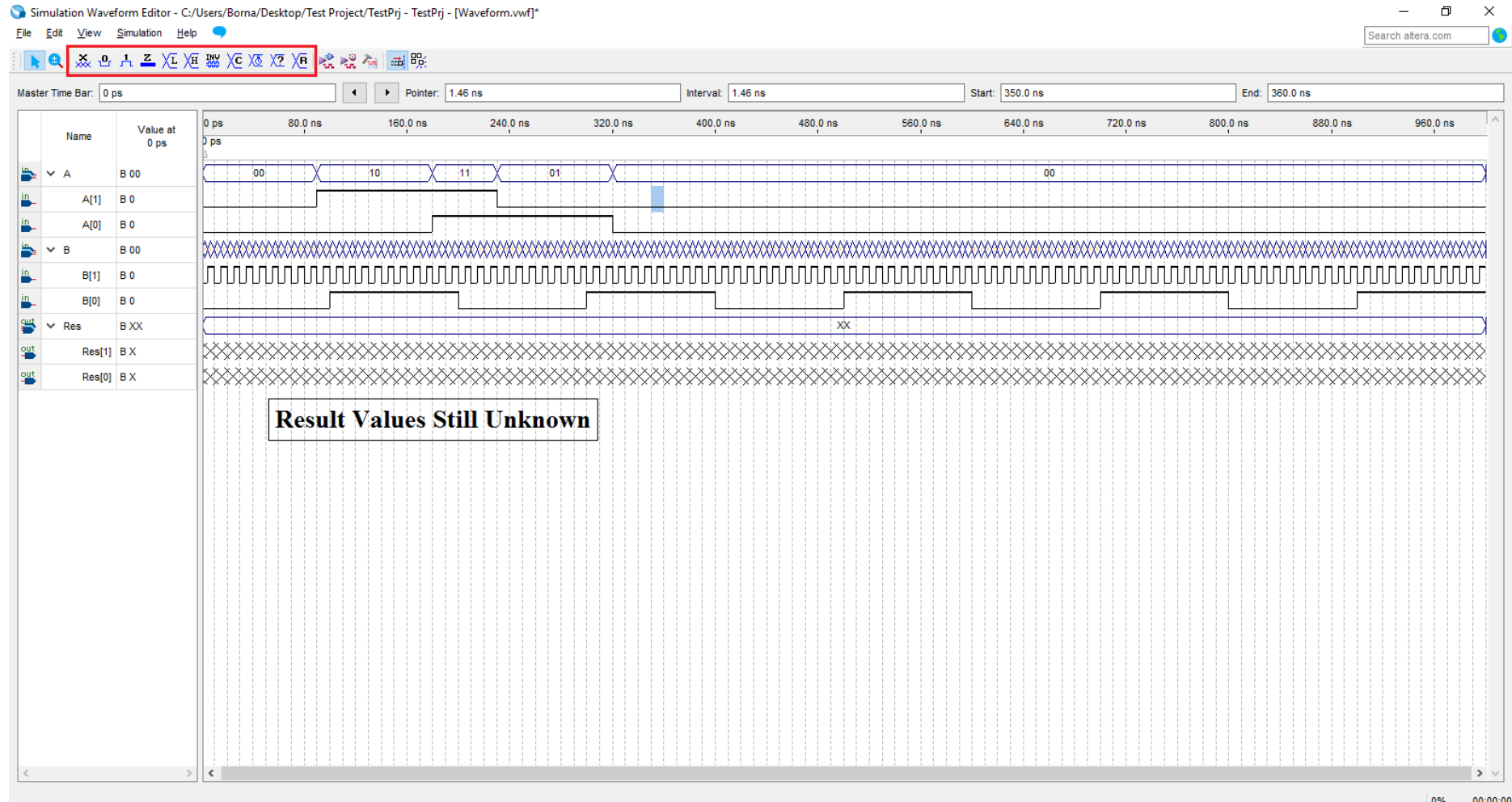
# Assign Value to Input Signals

- Select Signal and Radius

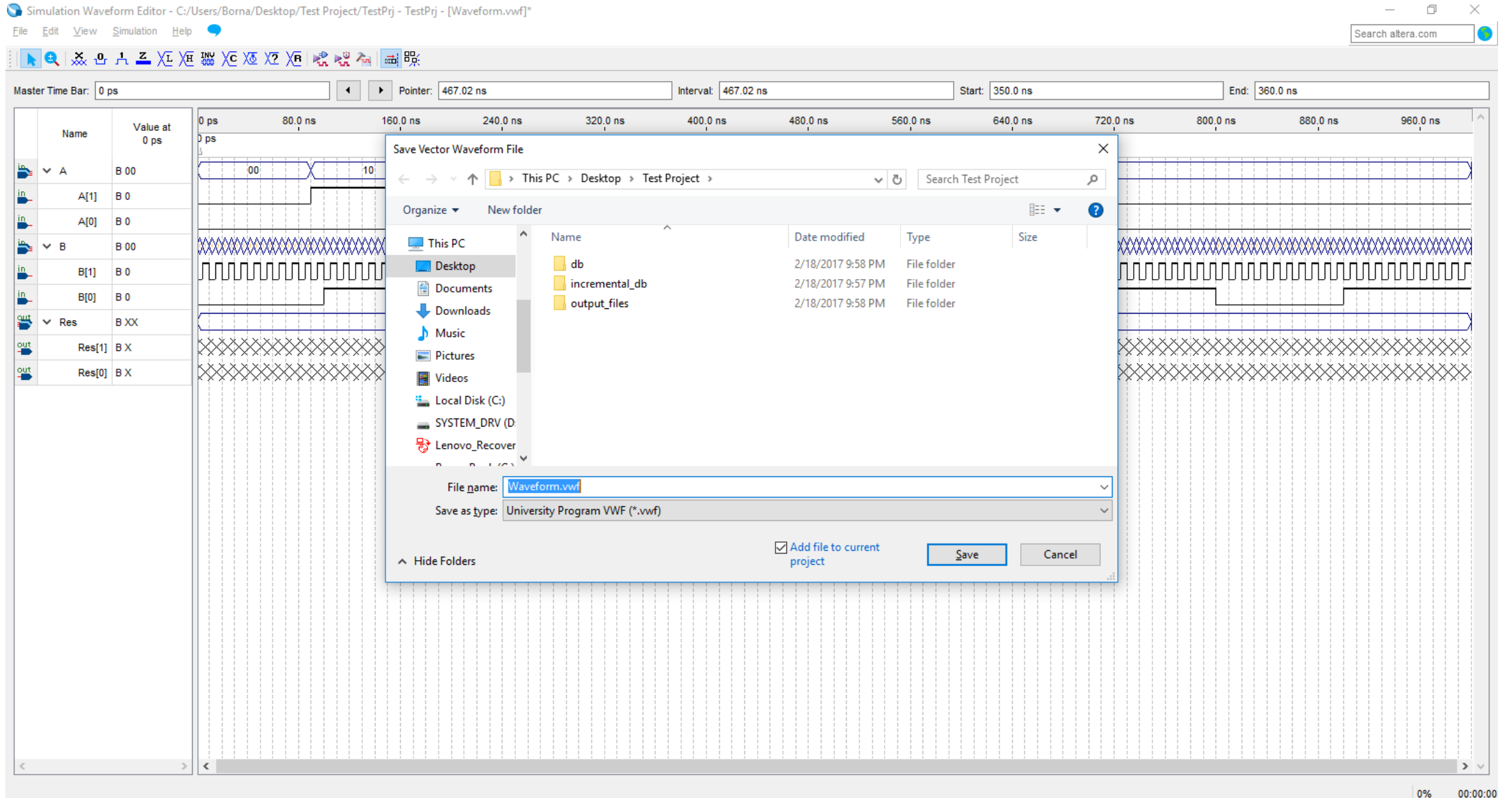


# Assign Value to Input Signals

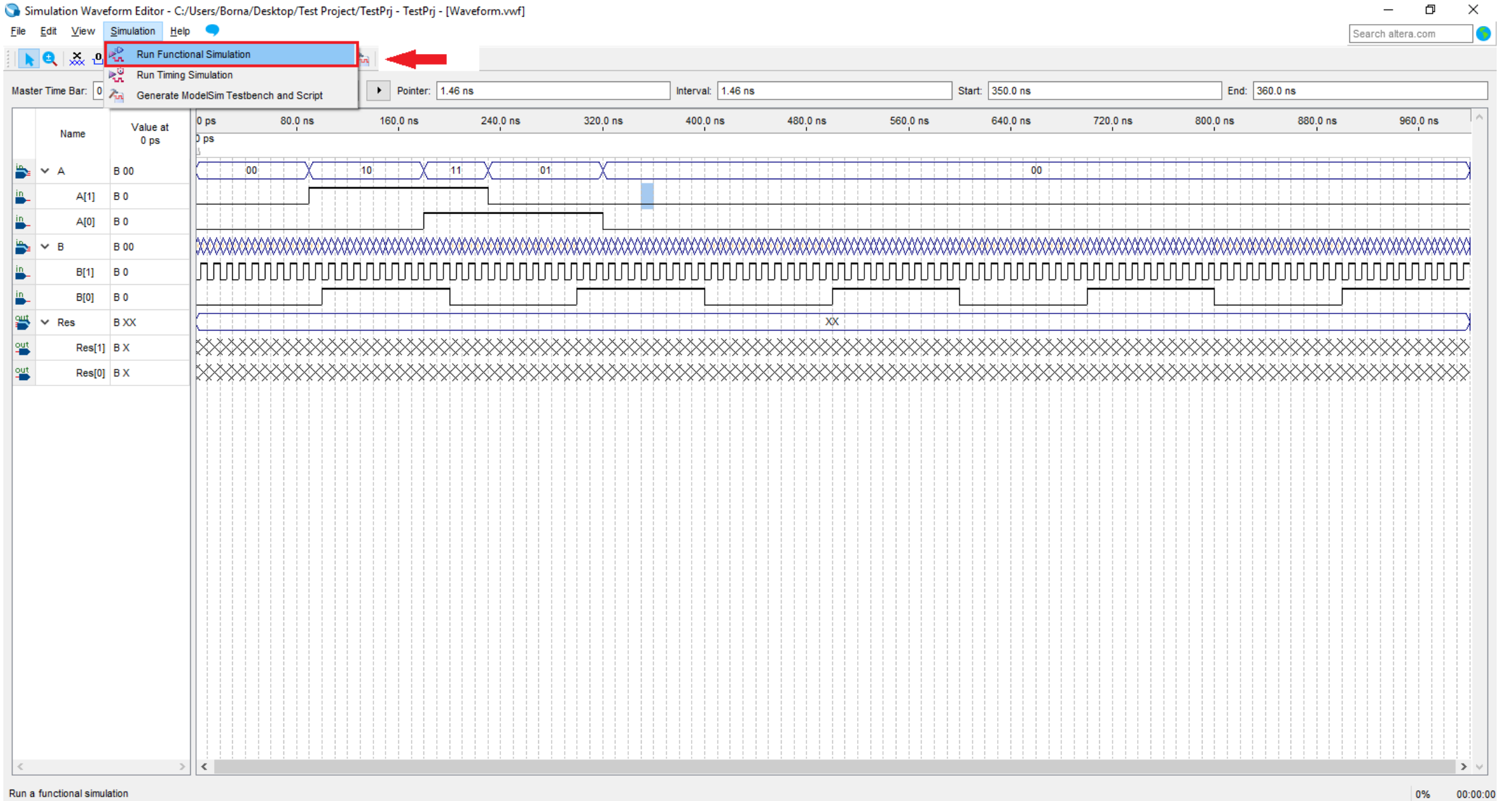
- Assign Value: 1, 0, High Z, Oscillating Signal, Clock, ...



# Save Waveform (.vwf file)



# Simulate Waveform (Functional Simulation)

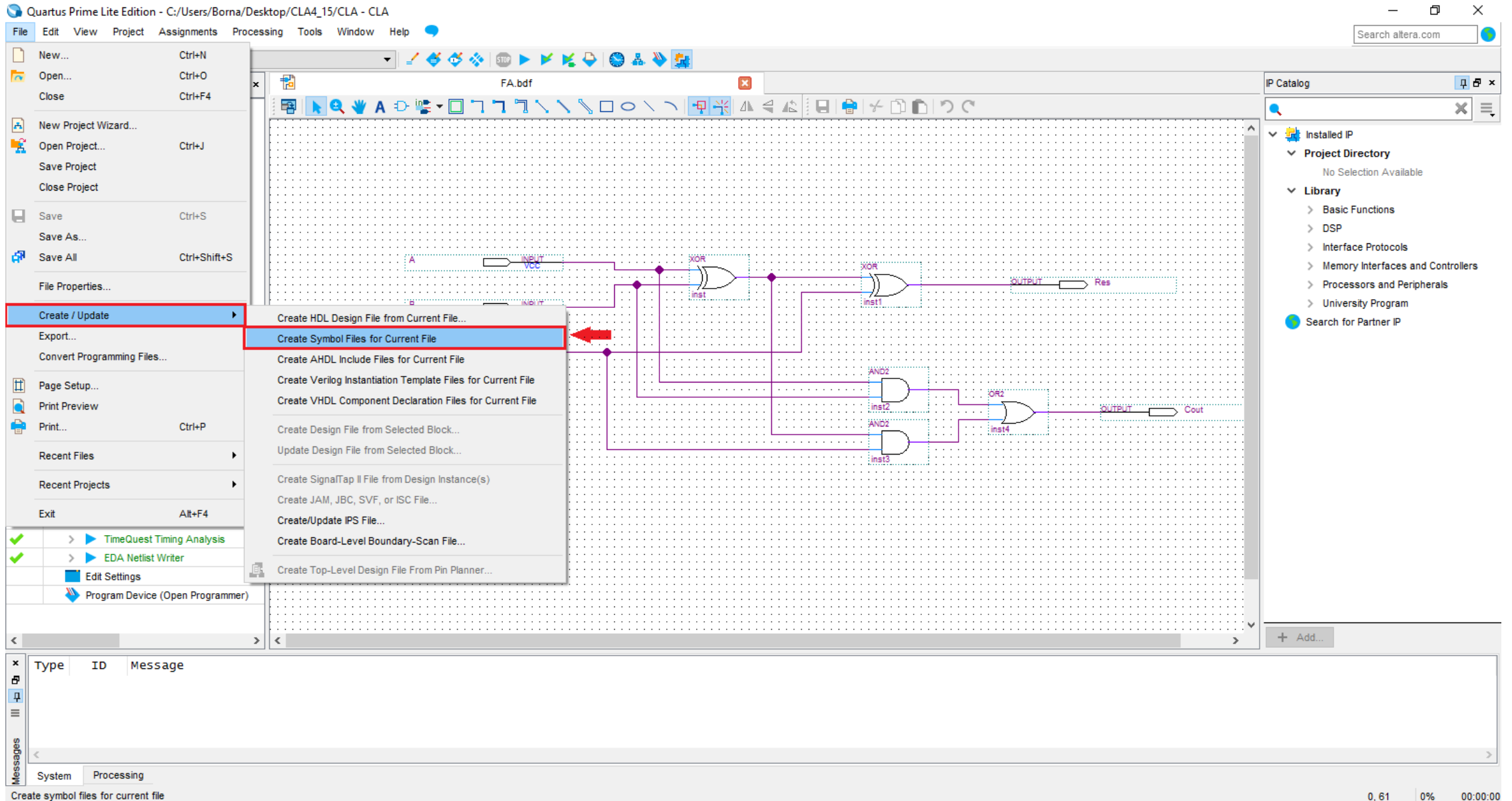


# Simulation Results

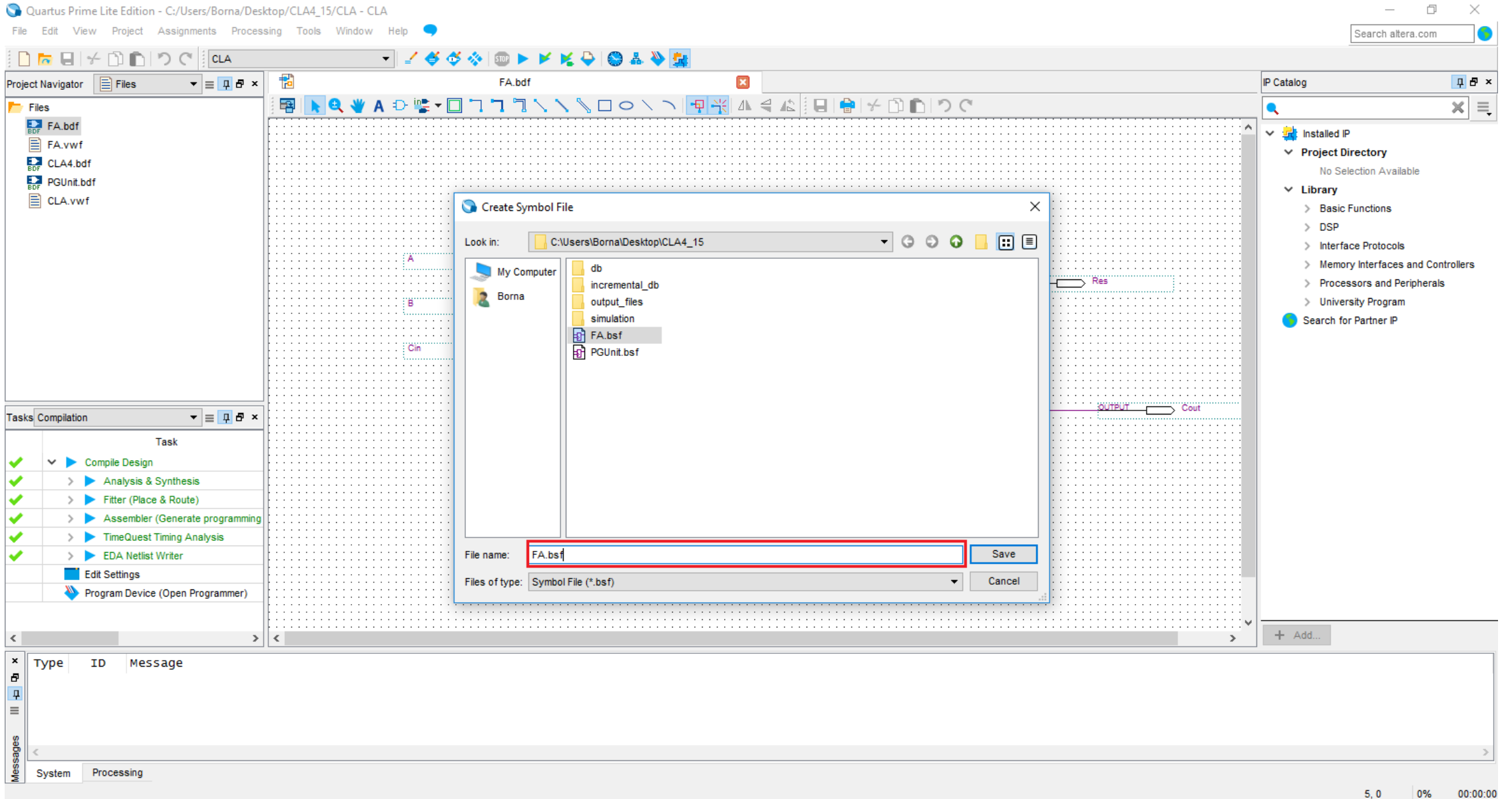




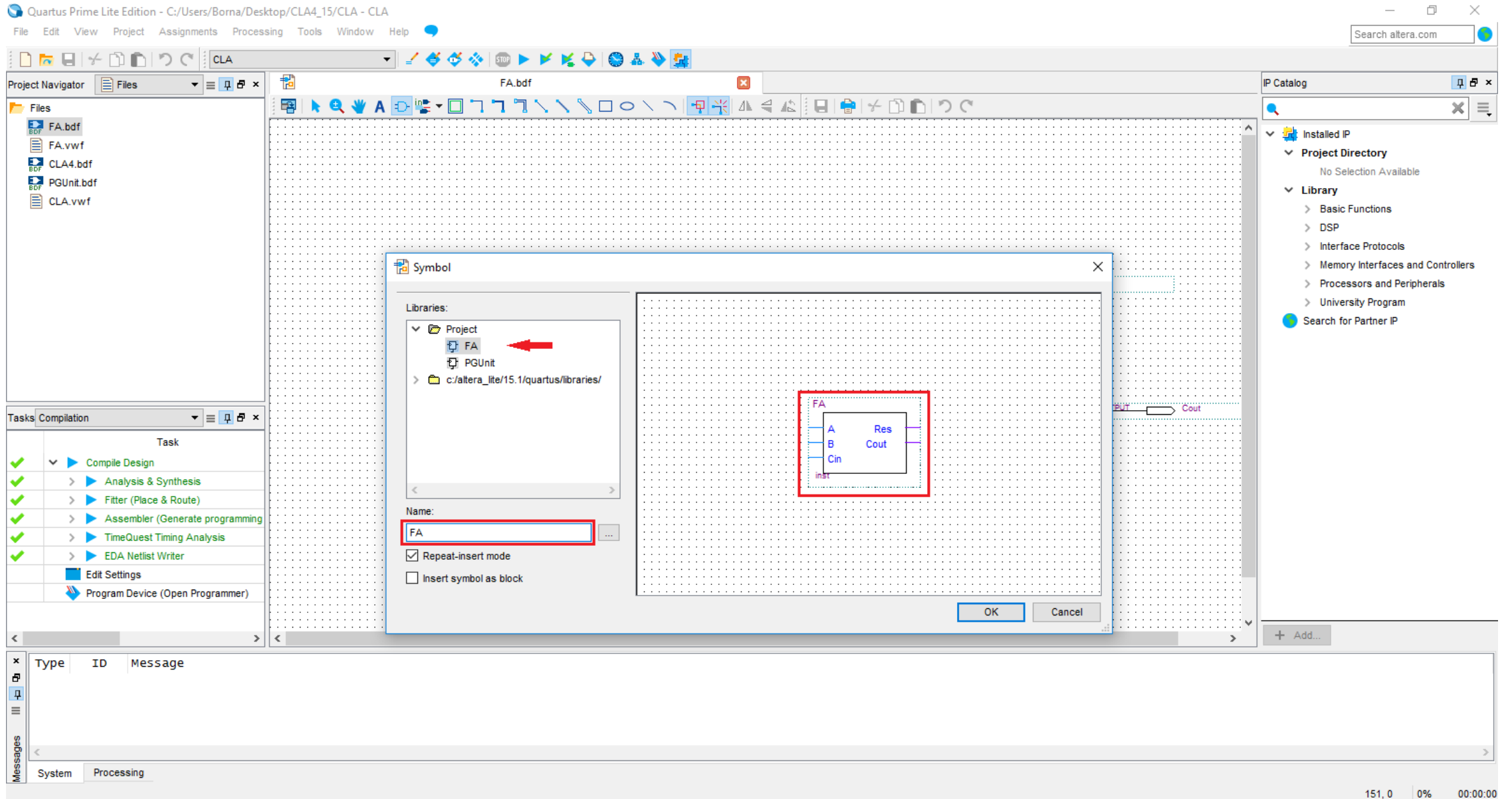
# Build an Instance of Your Own



# Save It As a .bsf File



# Use It As a Regular Module



An Example of 4bit Carry  
Look Ahead Adder Is Included

*Any Questions?*