Sharif University of Technology
Computer Architecture

Quartus II Tutorial

Prof. Asadi

Spring 2017

Download

- Windows:

  Quartus: ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/QuartusLiteSetup15.1.0.185-windows.exe

  Modelsim: ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/ModelSimSetup-15.1.0.185-windows.exe

  Devices: ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclone-15.1.0.185.qdz

  or ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclonev-15.1.0.185.qdz

- Linux:

  All Files: ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/Quartus-lite-15.1.0.185-linux.tar

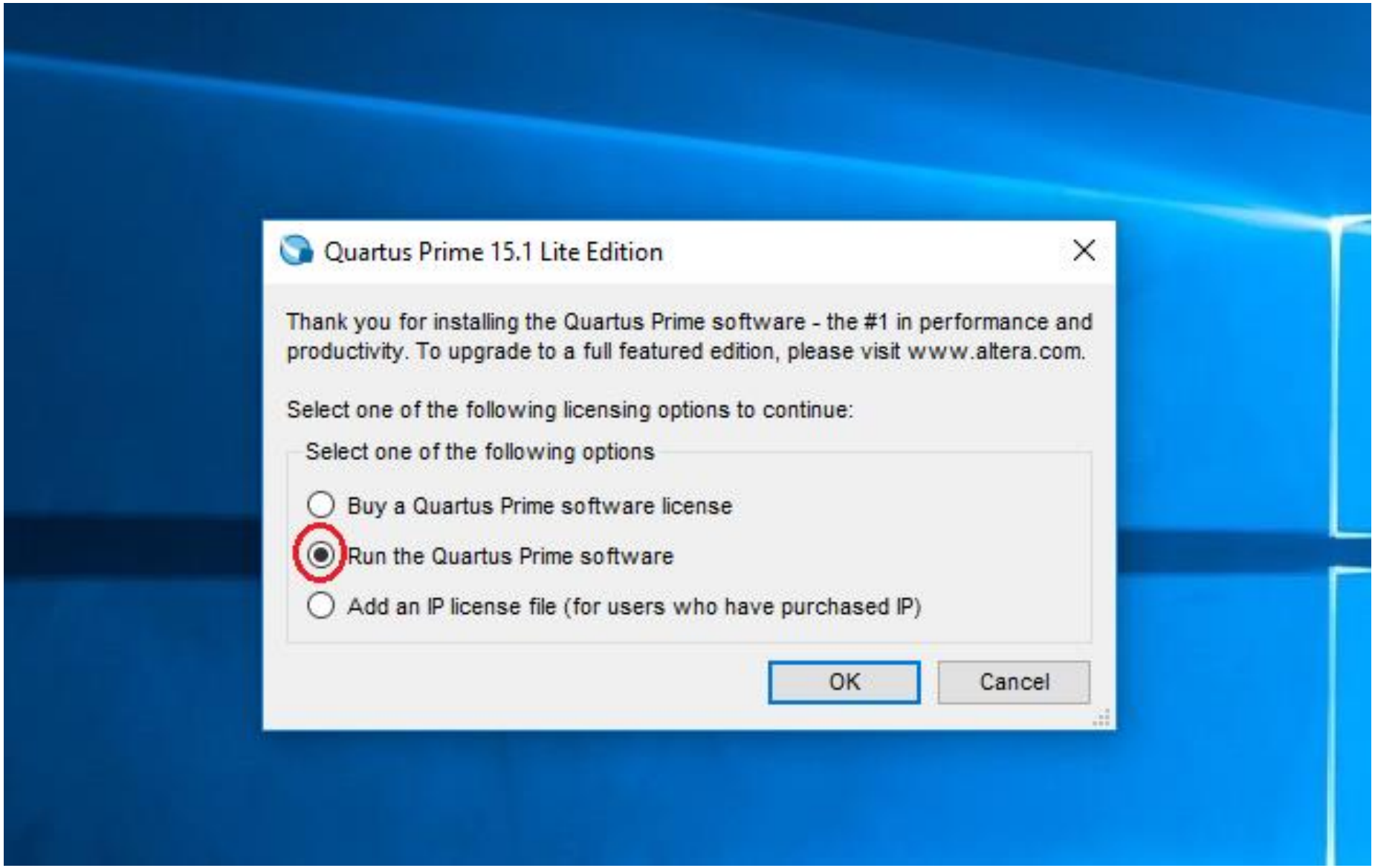
- Mac:

  Run the windows version in Parallel Windows

Install

- Put all files in the same folder and run Quartus install
- Do NOT change any of the default install settings

After Install



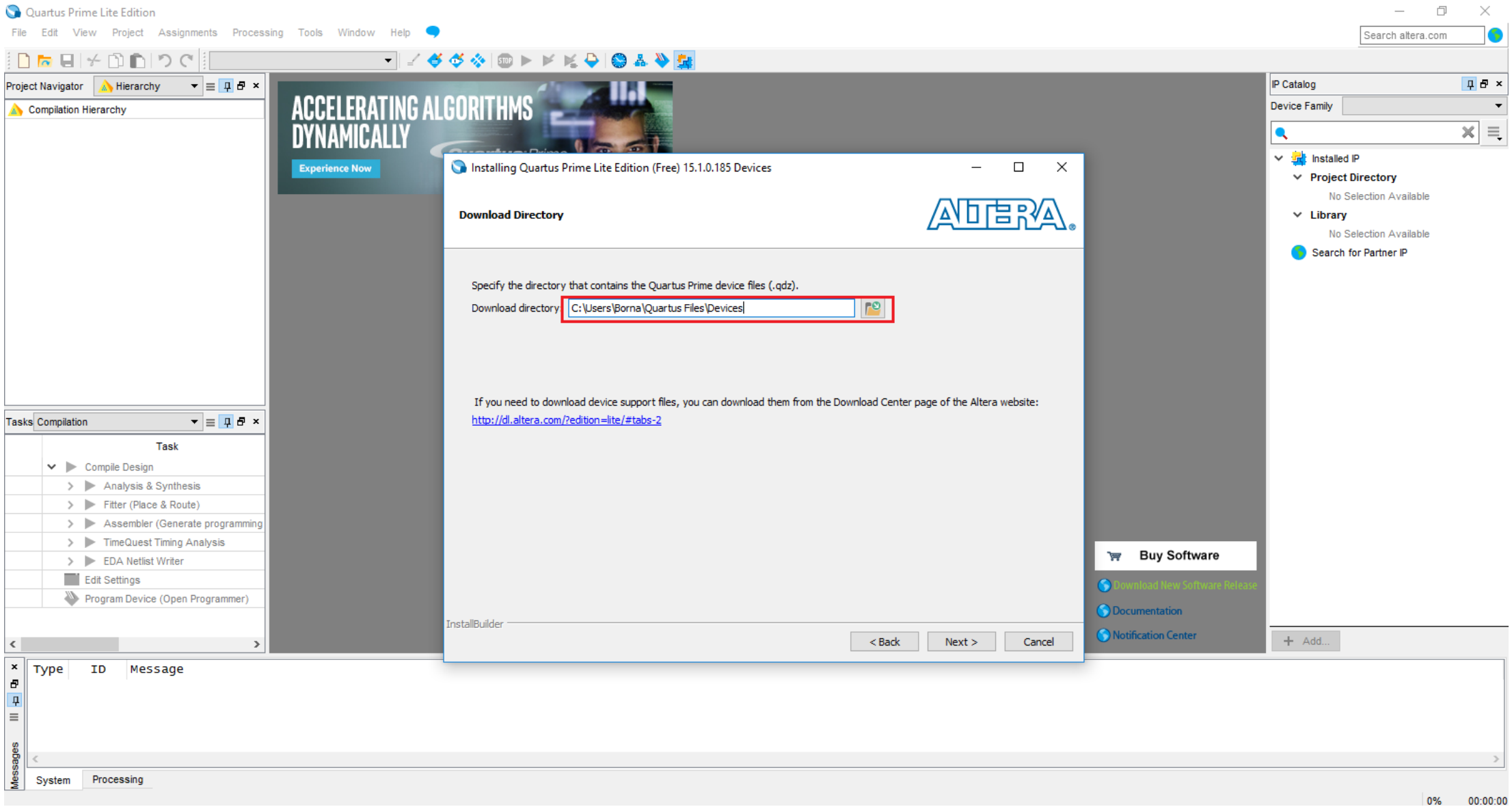
Install Devices (Manual)

- Download .qdz file
  - Windows

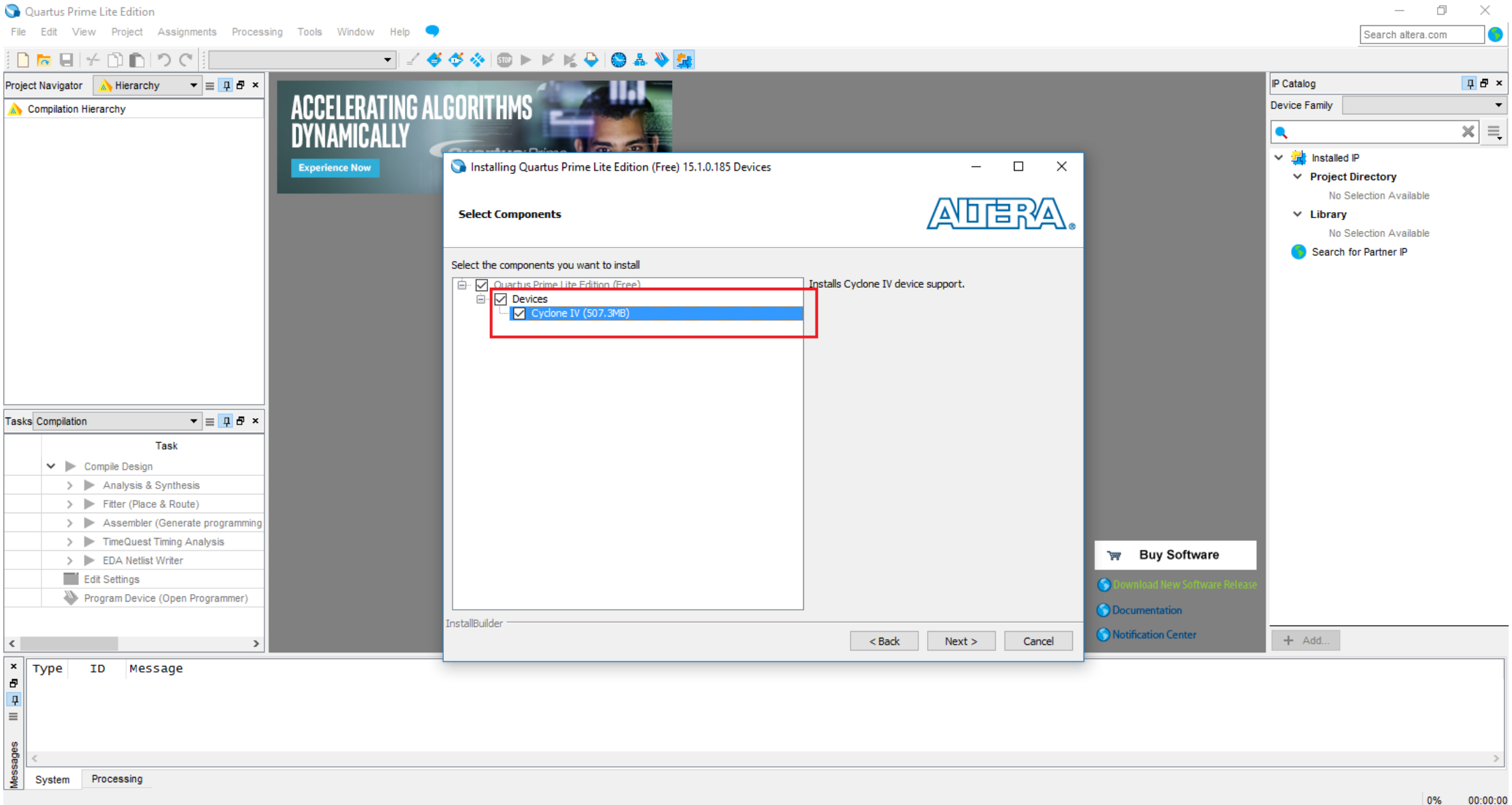
    ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/cyclone-15.1.0.185.qdz
  - Linux

    In the same zip folder as quartus
- Install .qdz file as devices

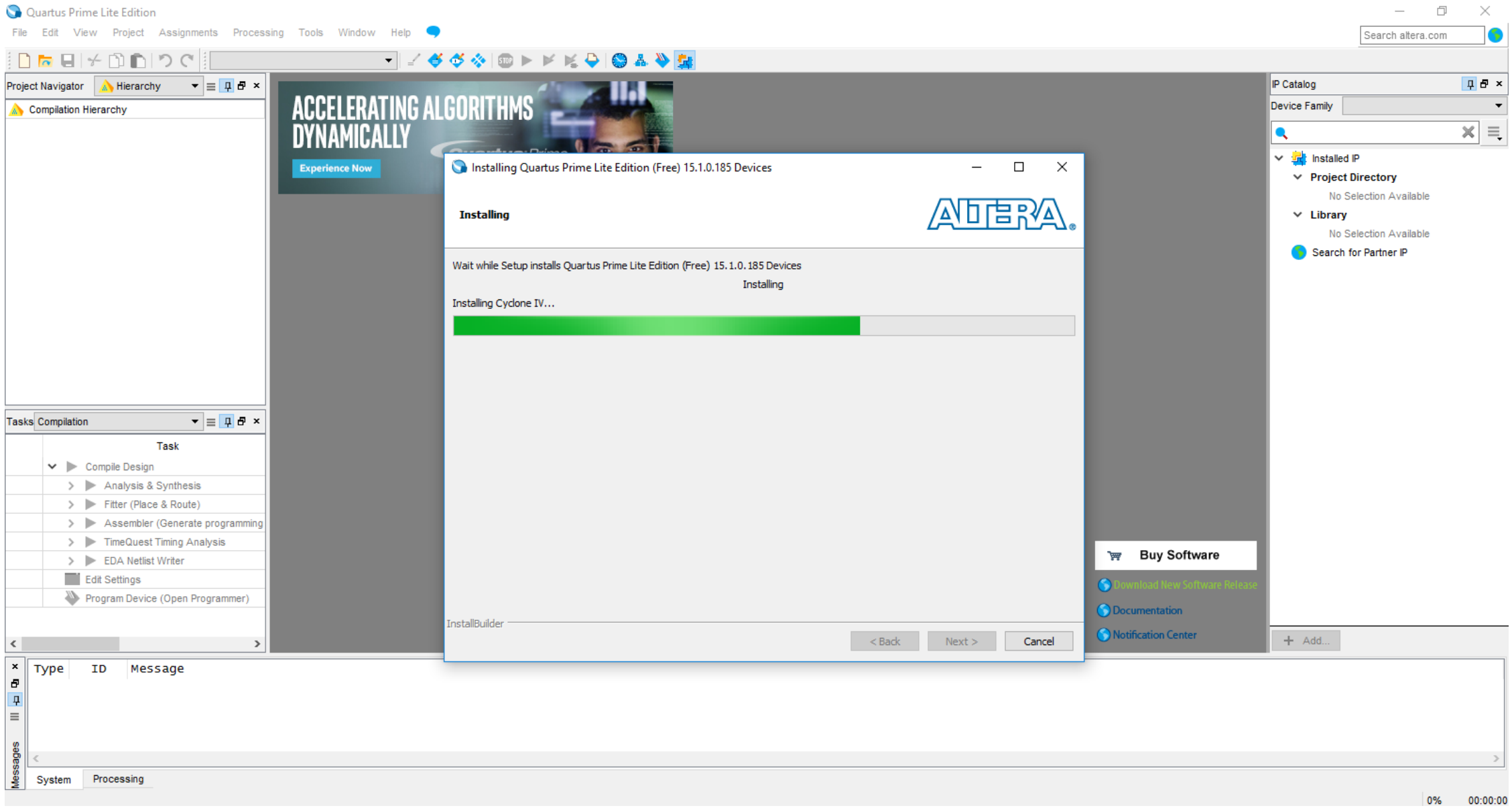
Install .qdz file as devices (Manual)



Install .qdz file as devices (Manual)



Install .qdz file as devices (Manual)



Install Modelsim (Manual)

- Download
  - Windows

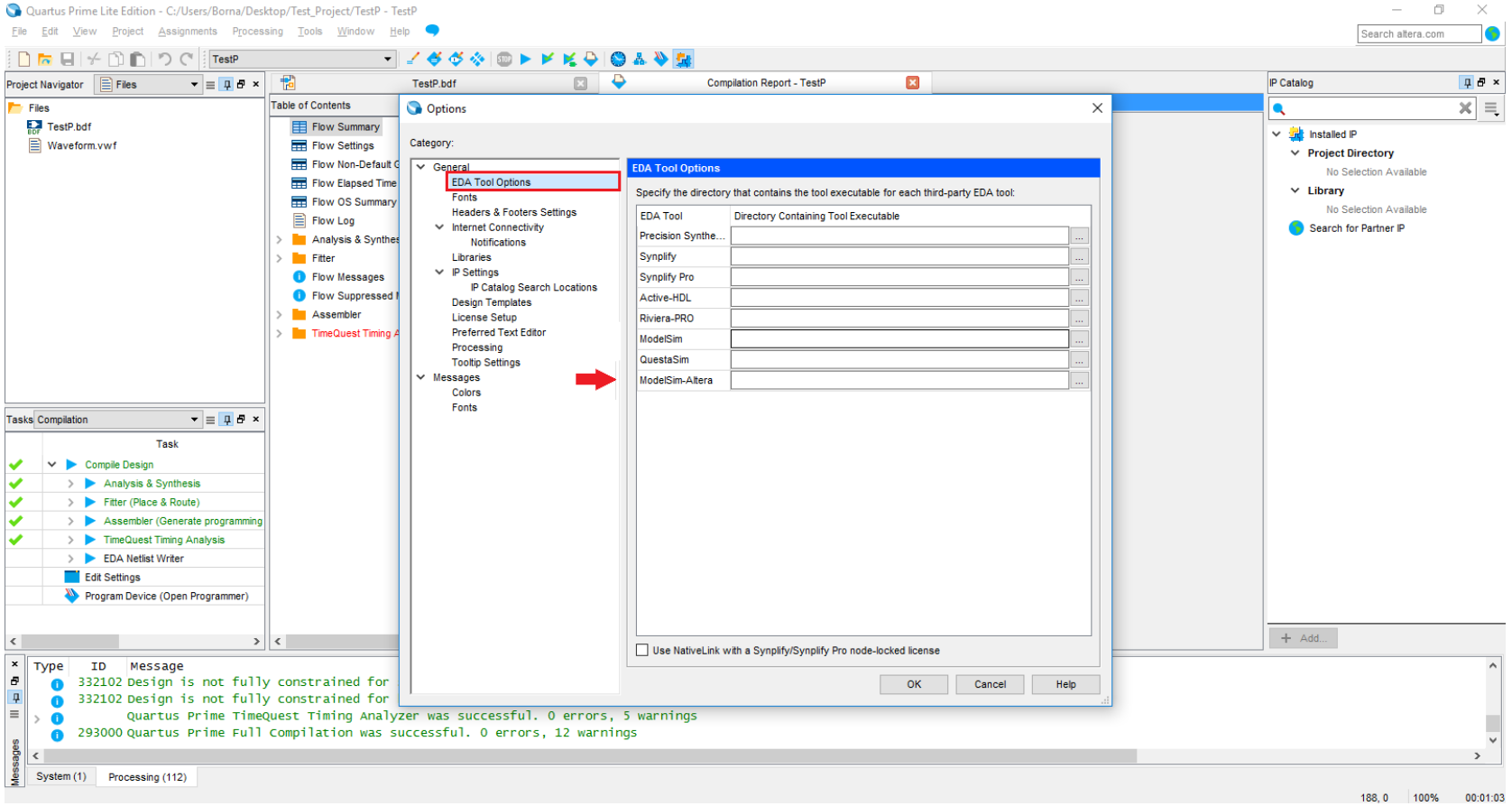
    ftp://cabinet.ce.sharif.edu/Courses/computer%20architecture/misc/ModelSimSetup-15.1.0.185-windows.exe
  - Linux

    In the same zip folder as quartus

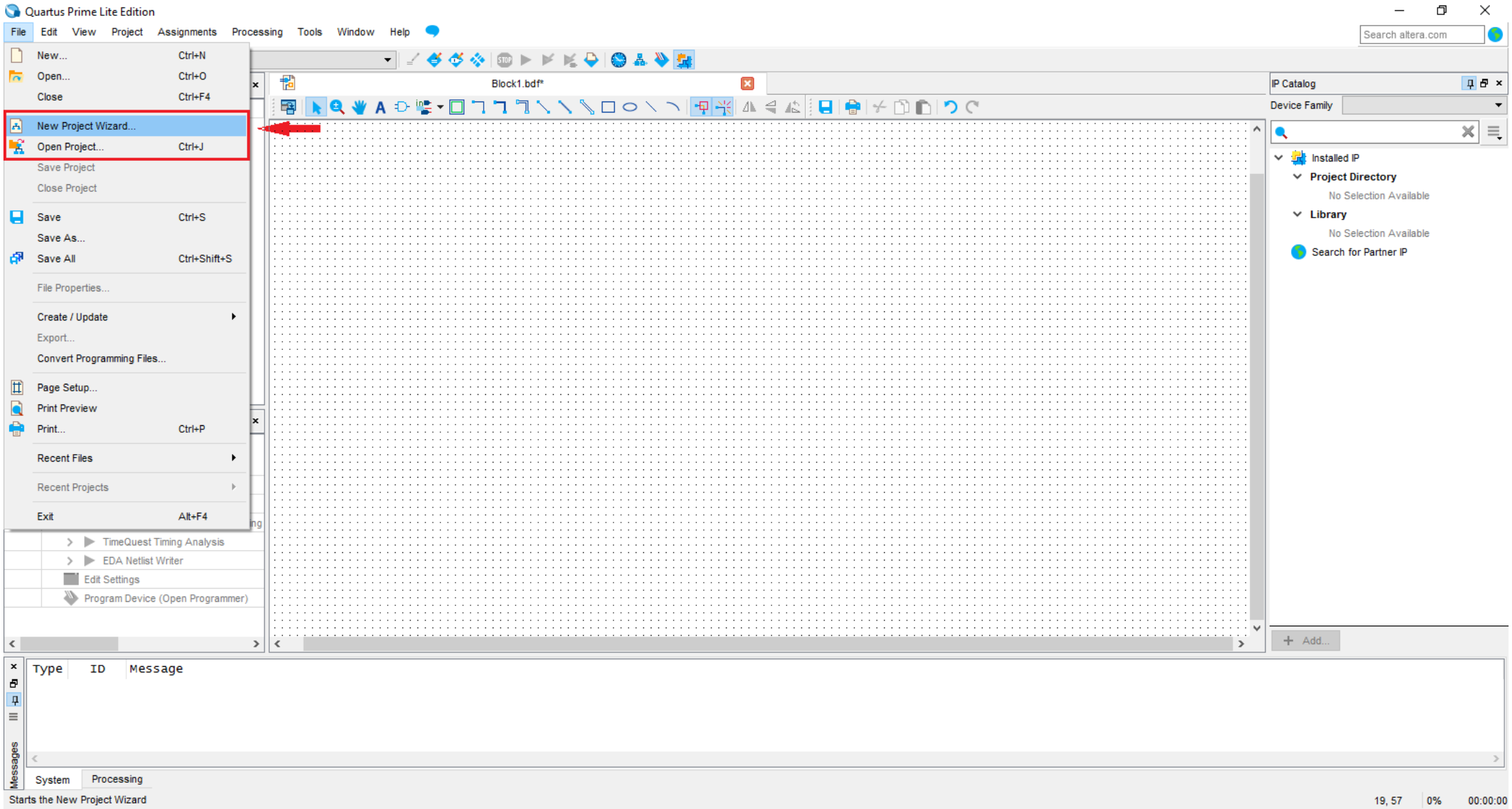
- Add To Executables

Add Modelsim To Executables (Manual)

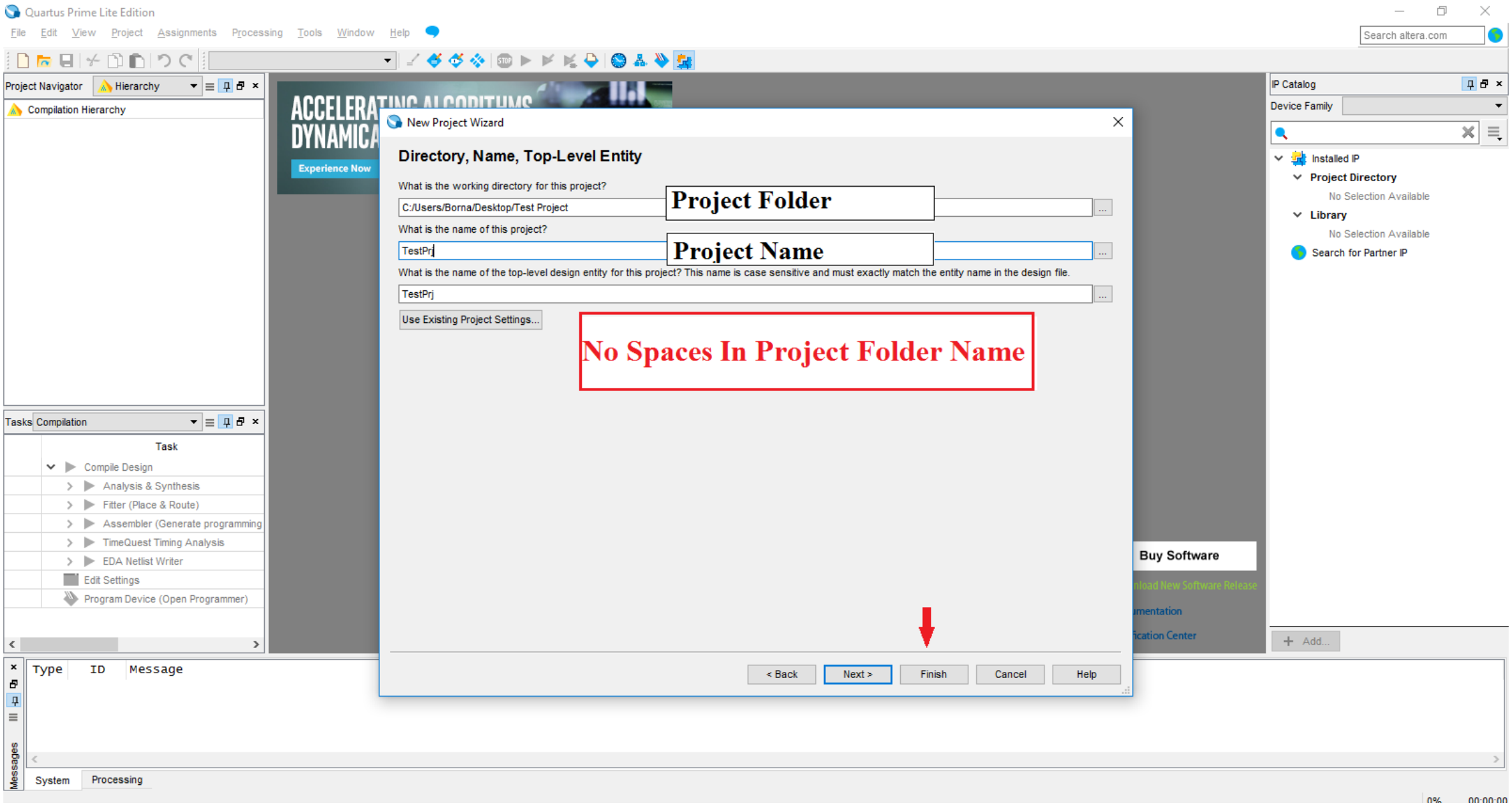
- Tools => Options => EDA Tool Options
- Add ModelSim-Installation-Path/bin to Modelsim-Altera



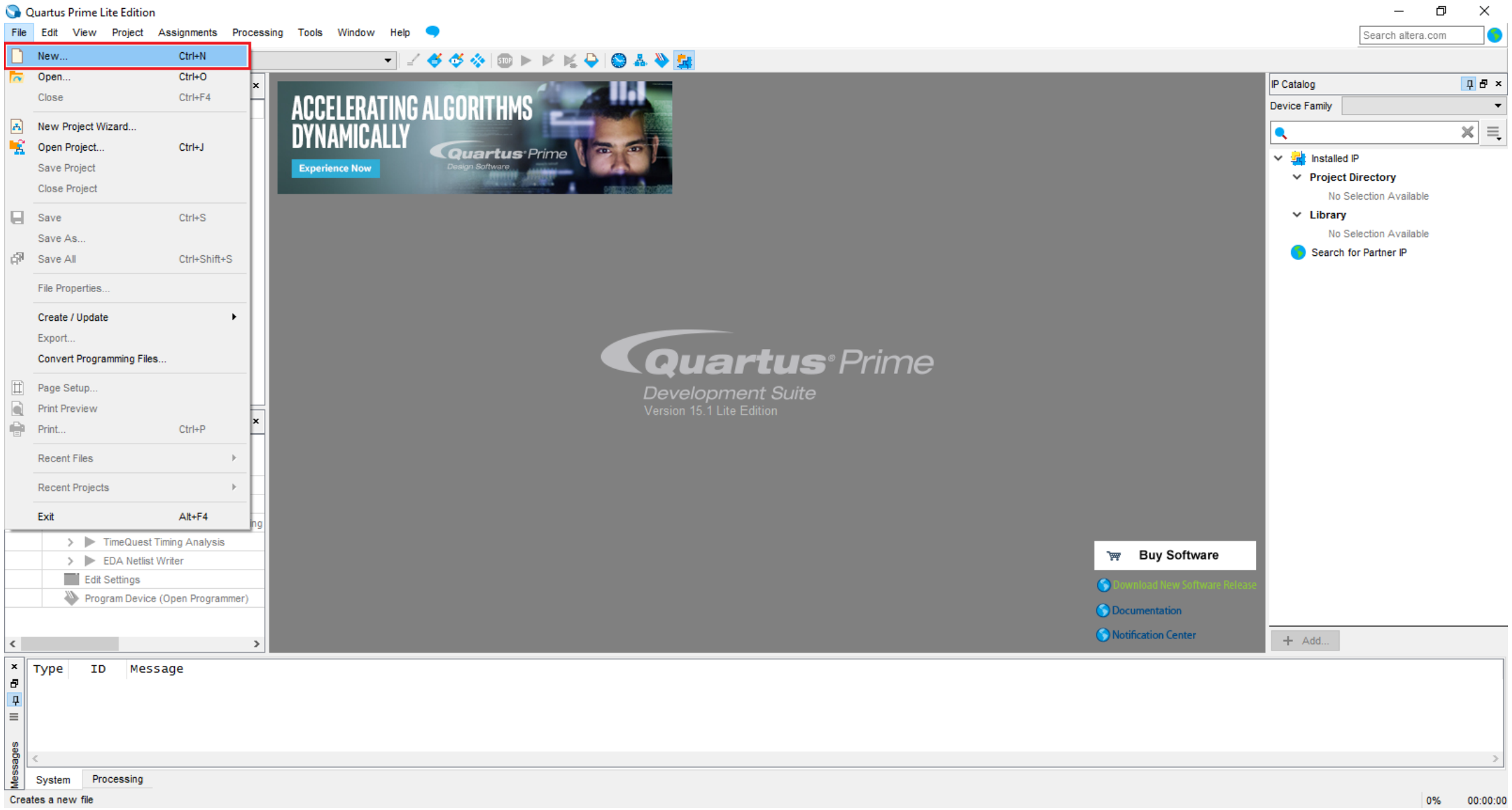
Open A Project



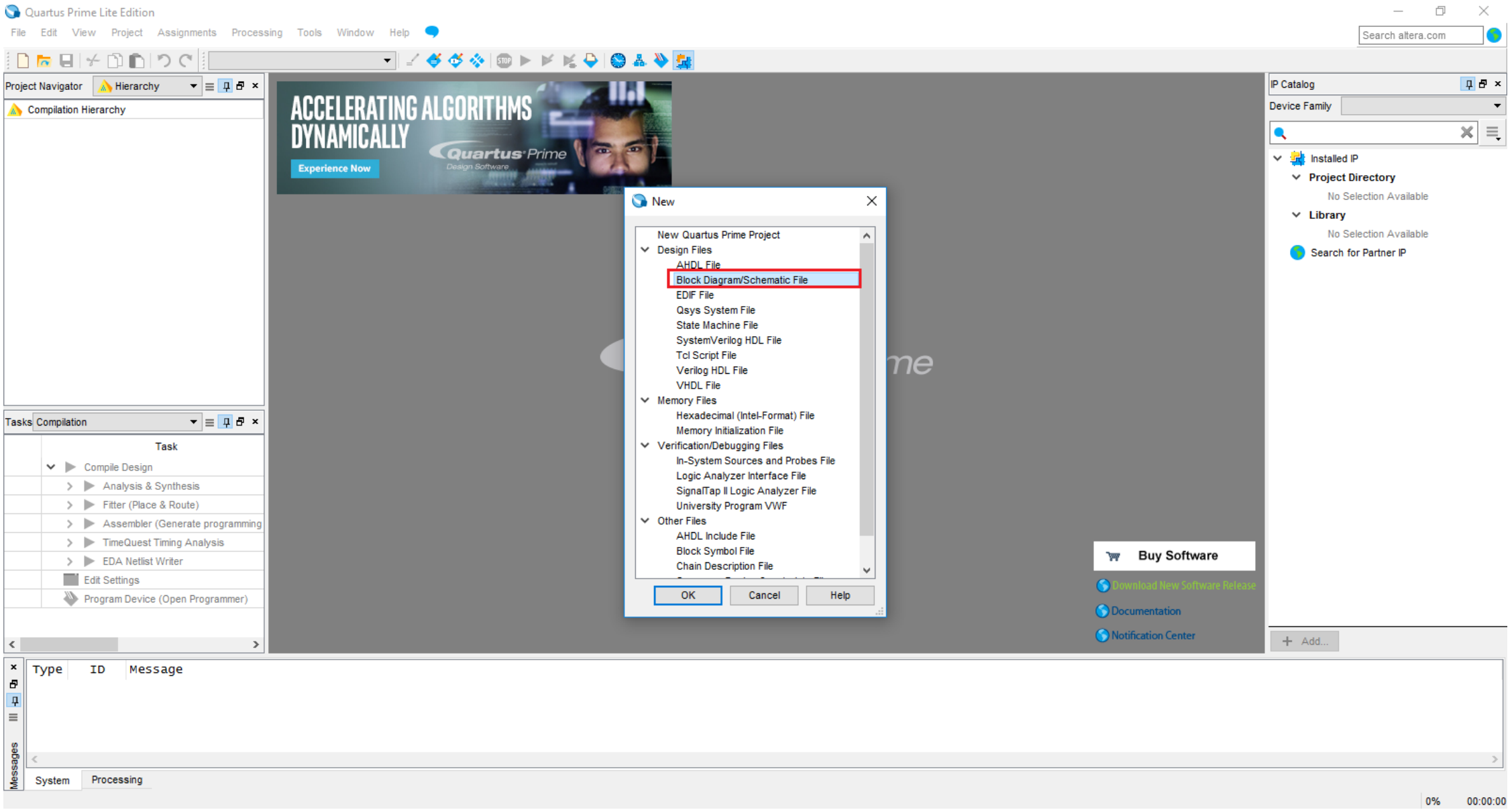
Project Wizard



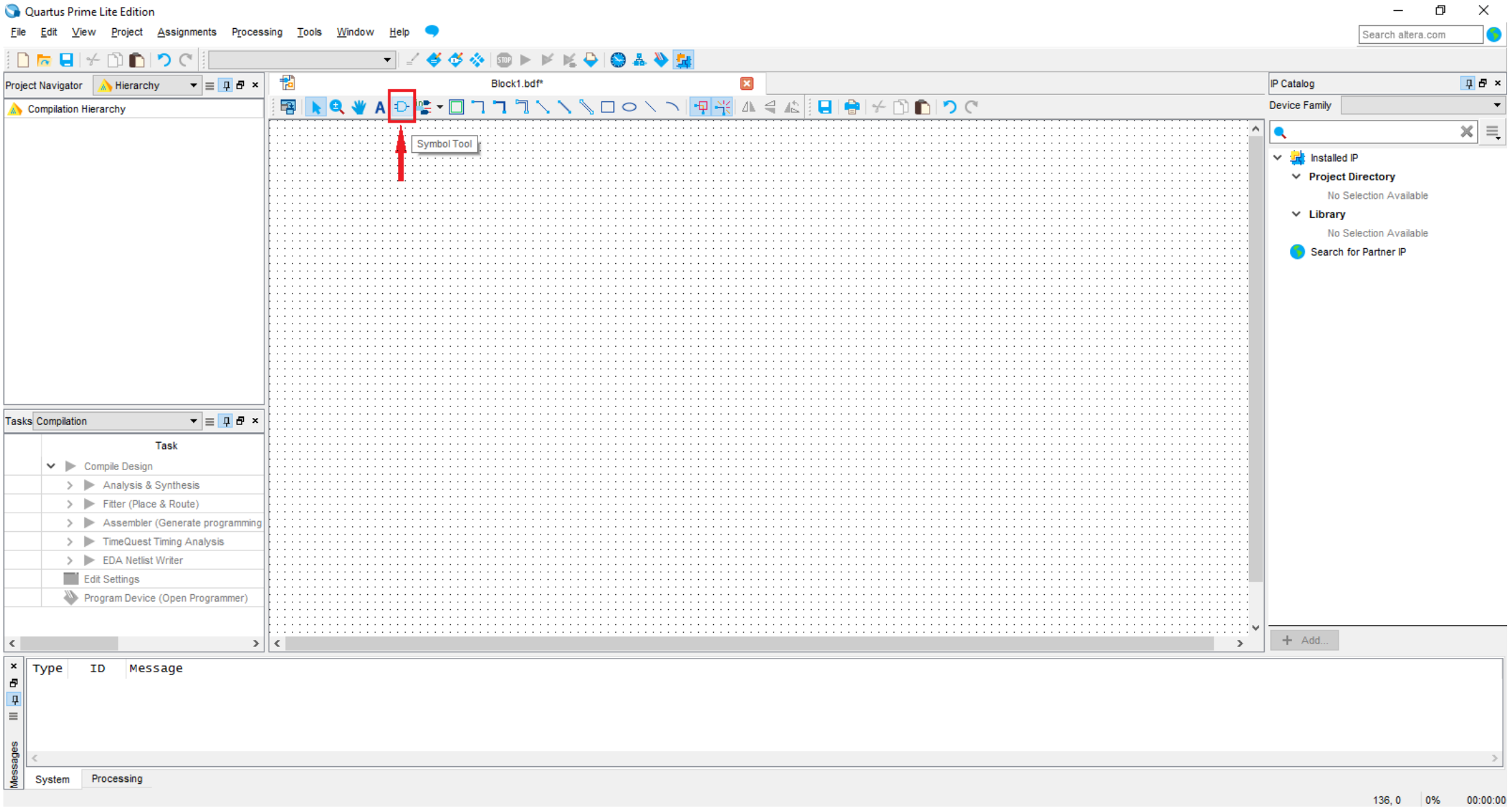
Open Block Diagram / Schematic File



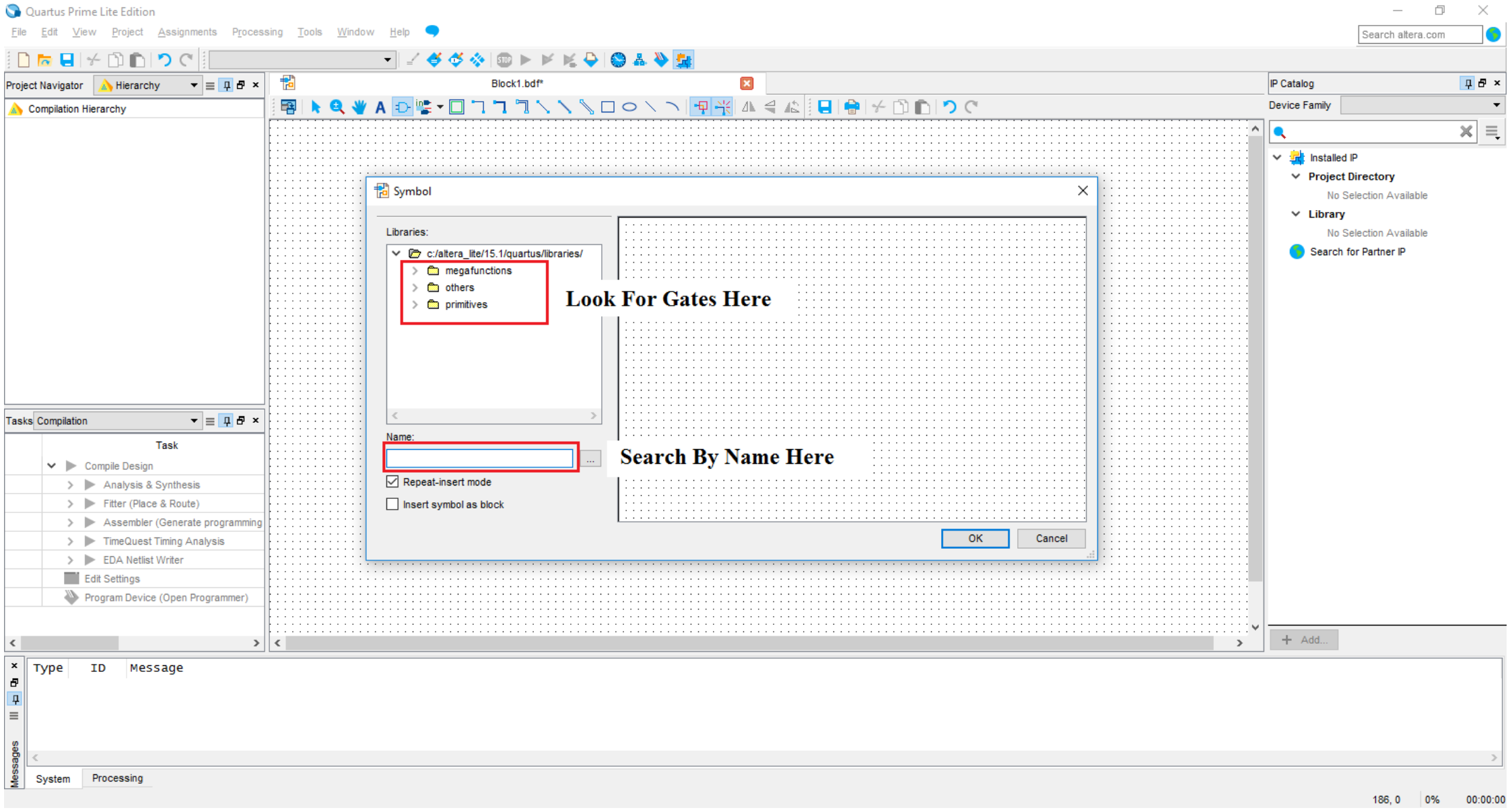
Open Block Diagram / Schematic File



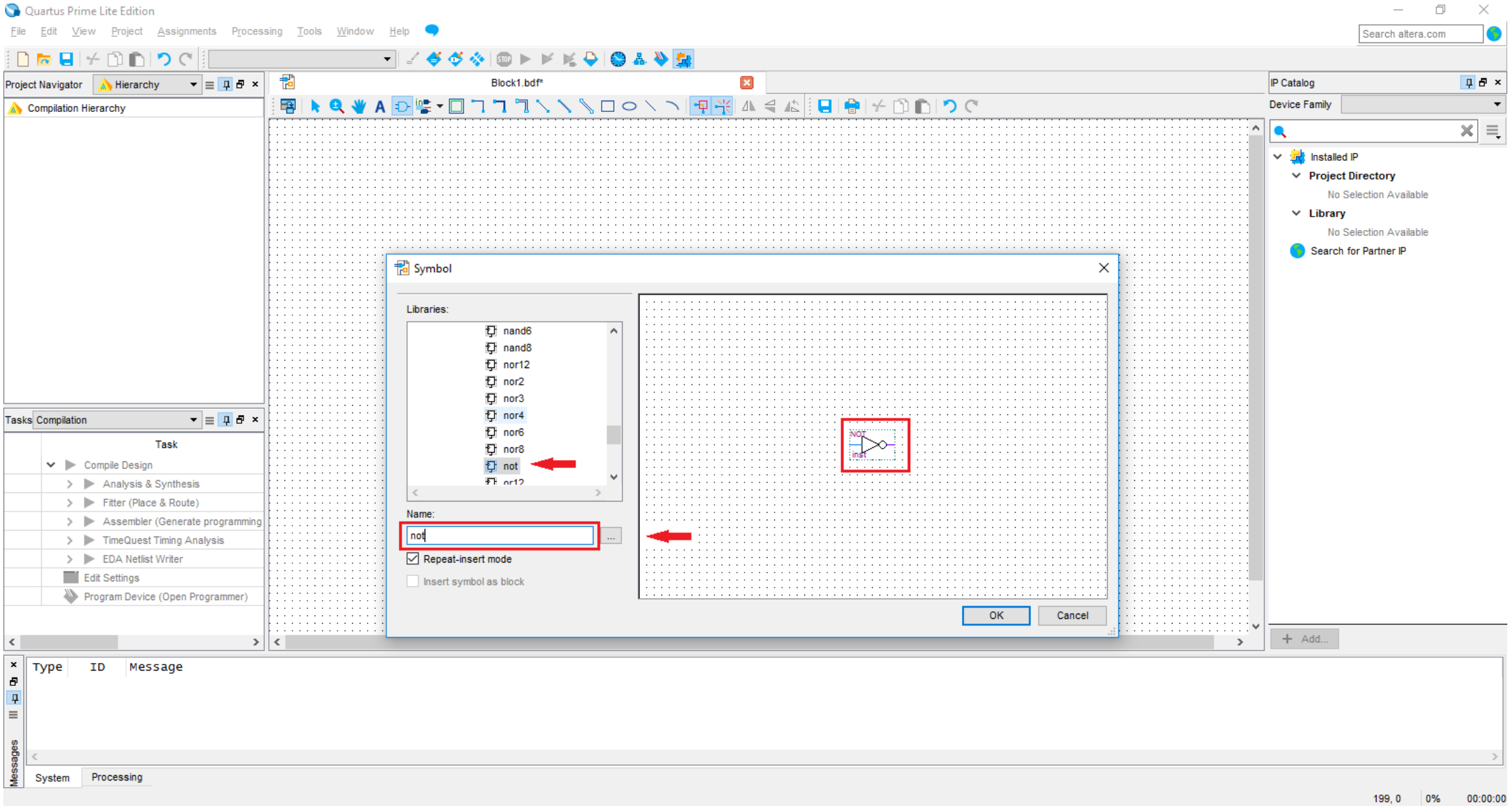
Insert Modules & Symbols



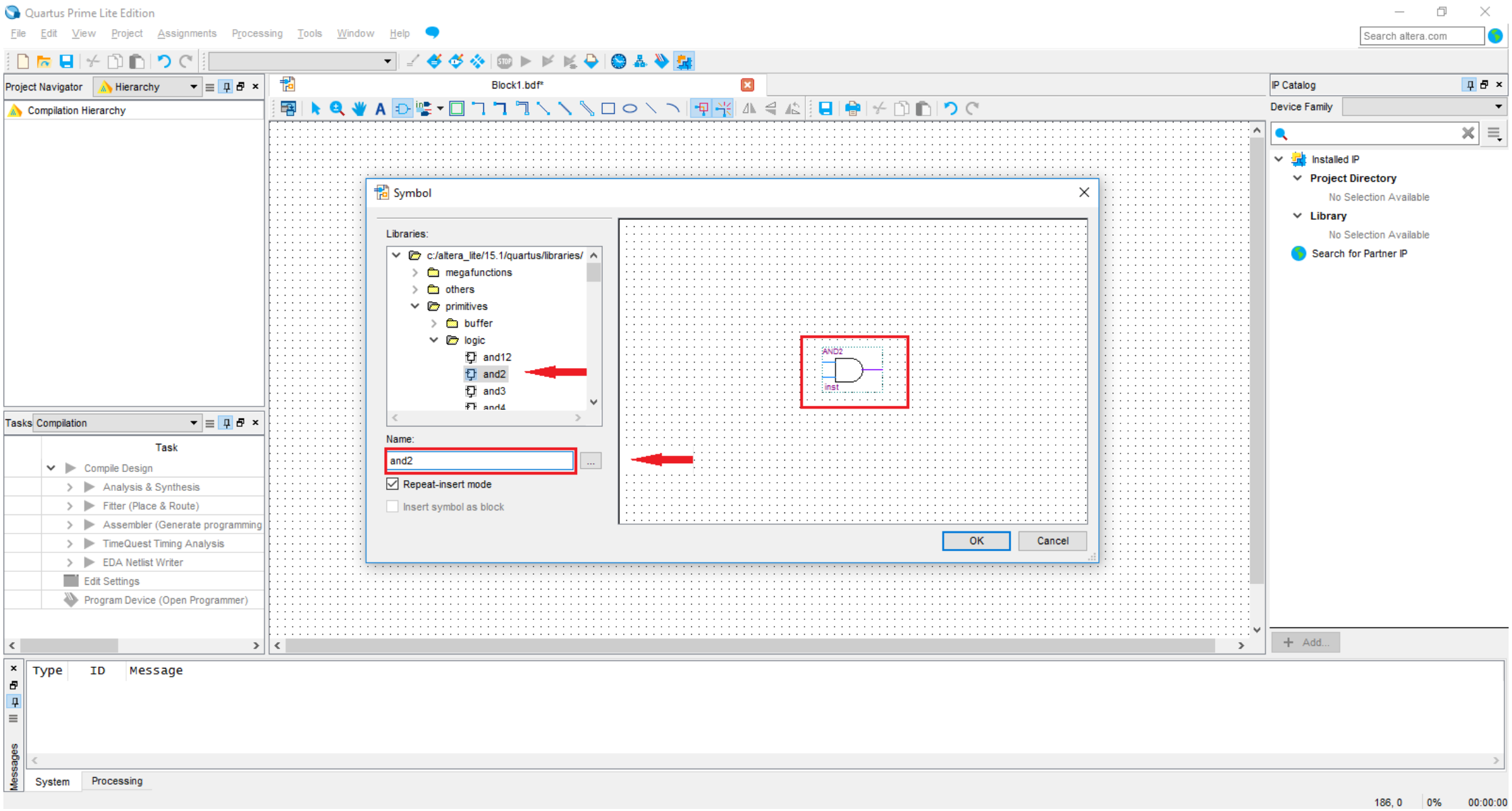
Insert Modules & Symbols



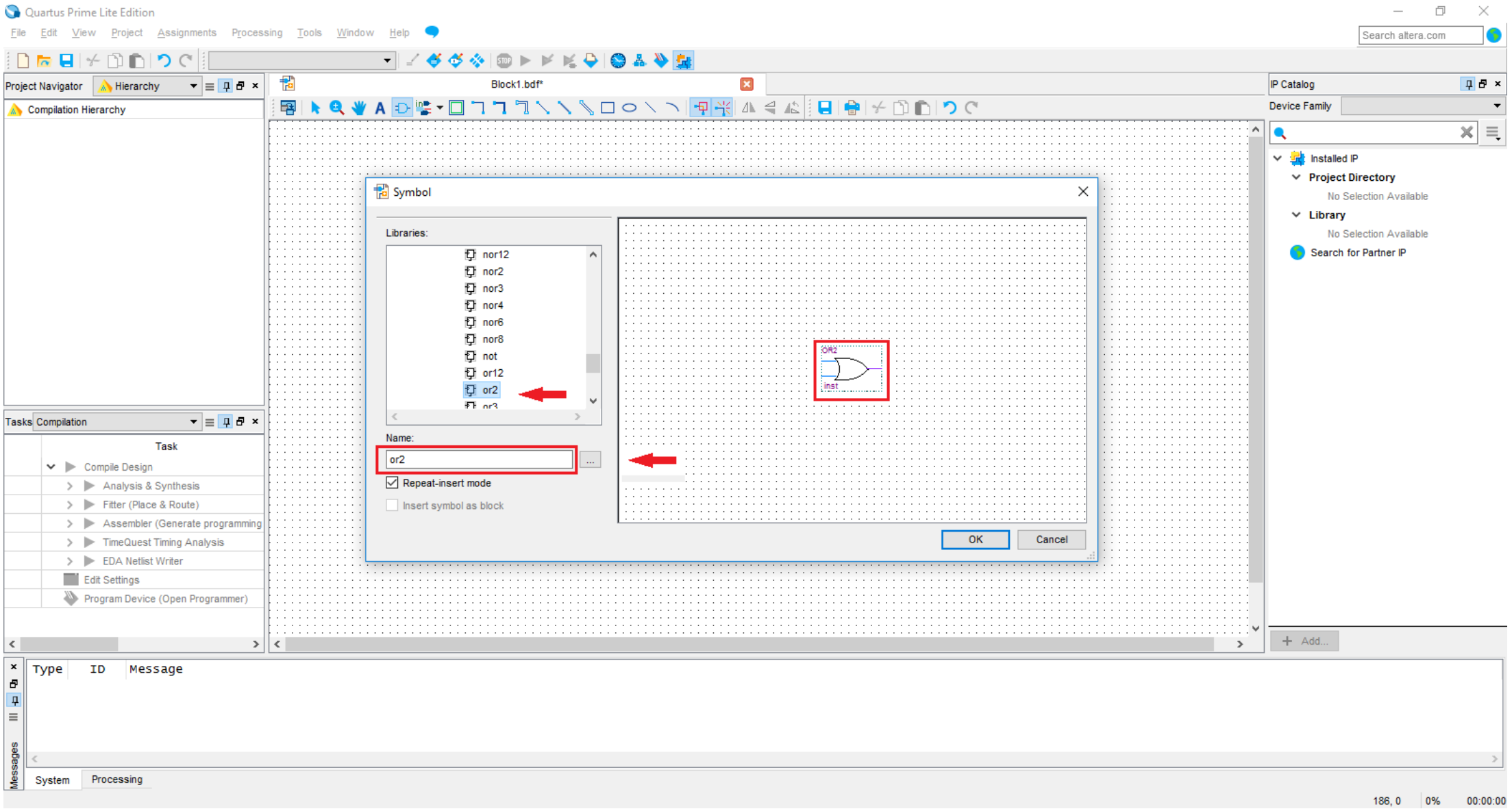
Example: Not


Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator Hierarchy
Compilation Hierarchy
Block1.bdf*
IP Catalog
Device Family
Installed IP
Project Directory
No Selection Available
Library
No Selection Available
Search for Partner IP
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
TimeQuest Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Symbol
Libraries:
nand6
nand8
nor12
nor2
nor3
nor4
nor6
nor8
not
Name:
not
Repeat-insert mode
Insert symbol as block
OK
Cancel
Add...
Type ID Message
Messages
System
Processing
199, 0
0%
00:00:00

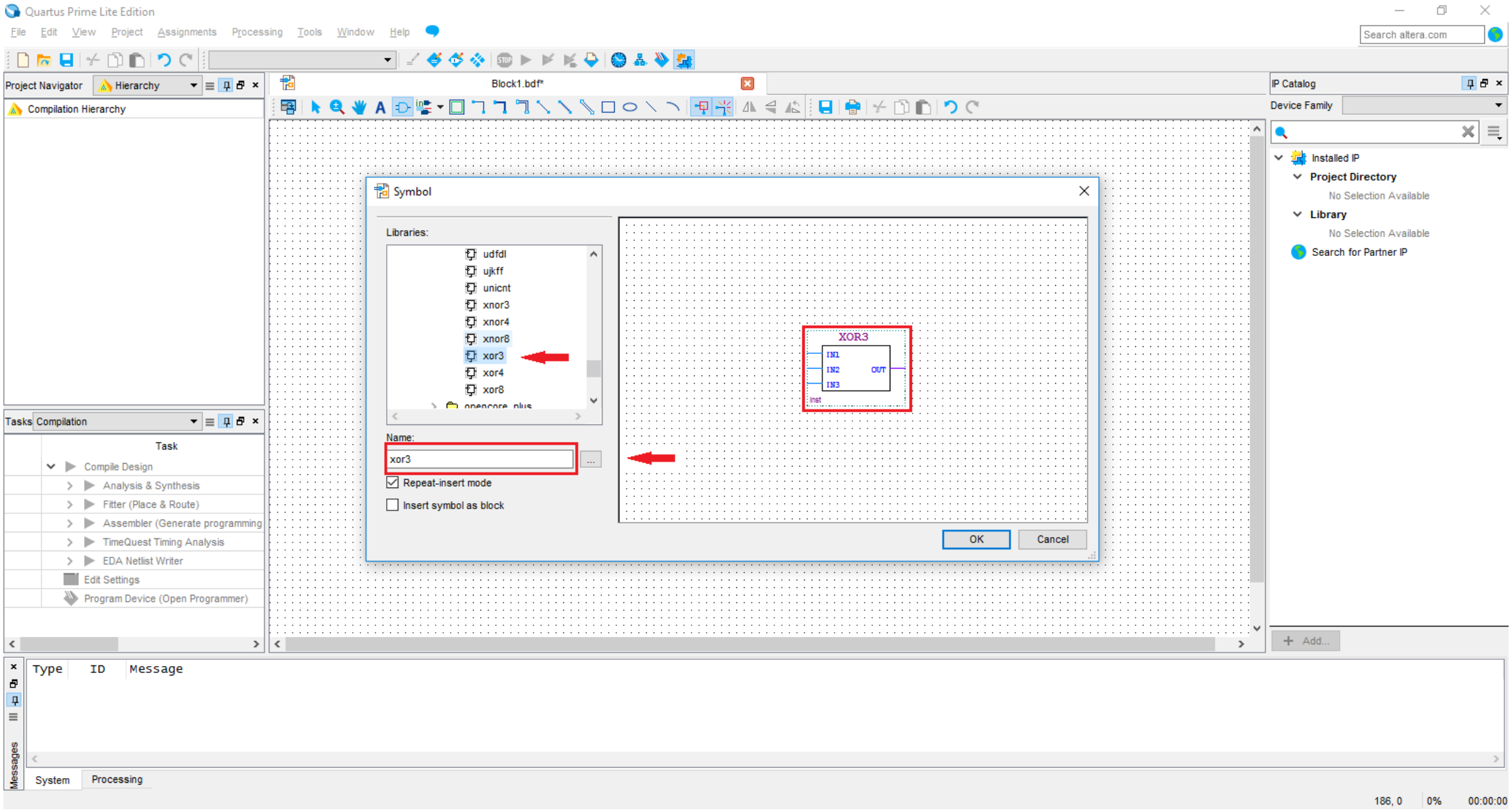
Example: 2 Input AND (and2)



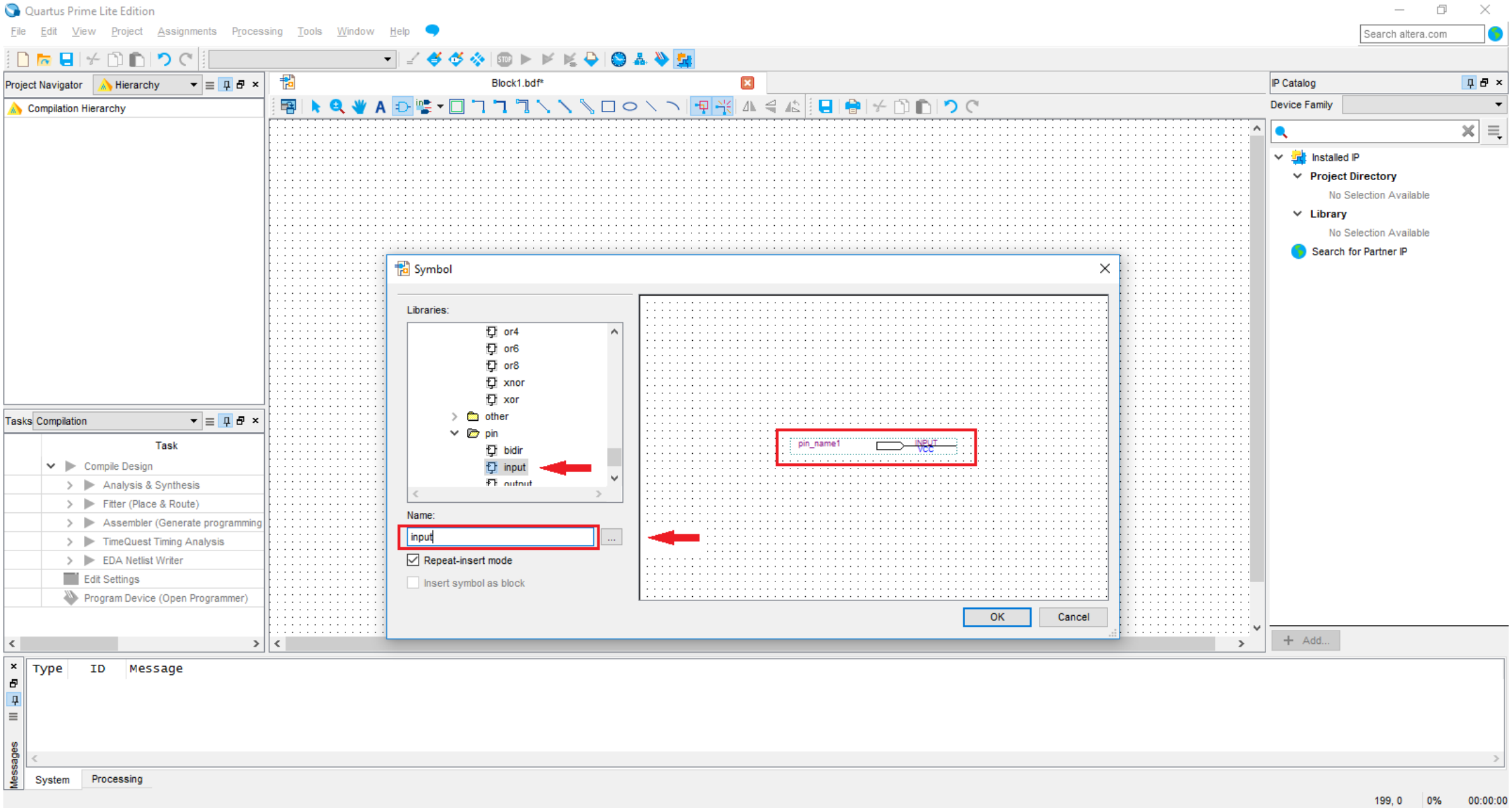
Example: 2 Input OR (or2)



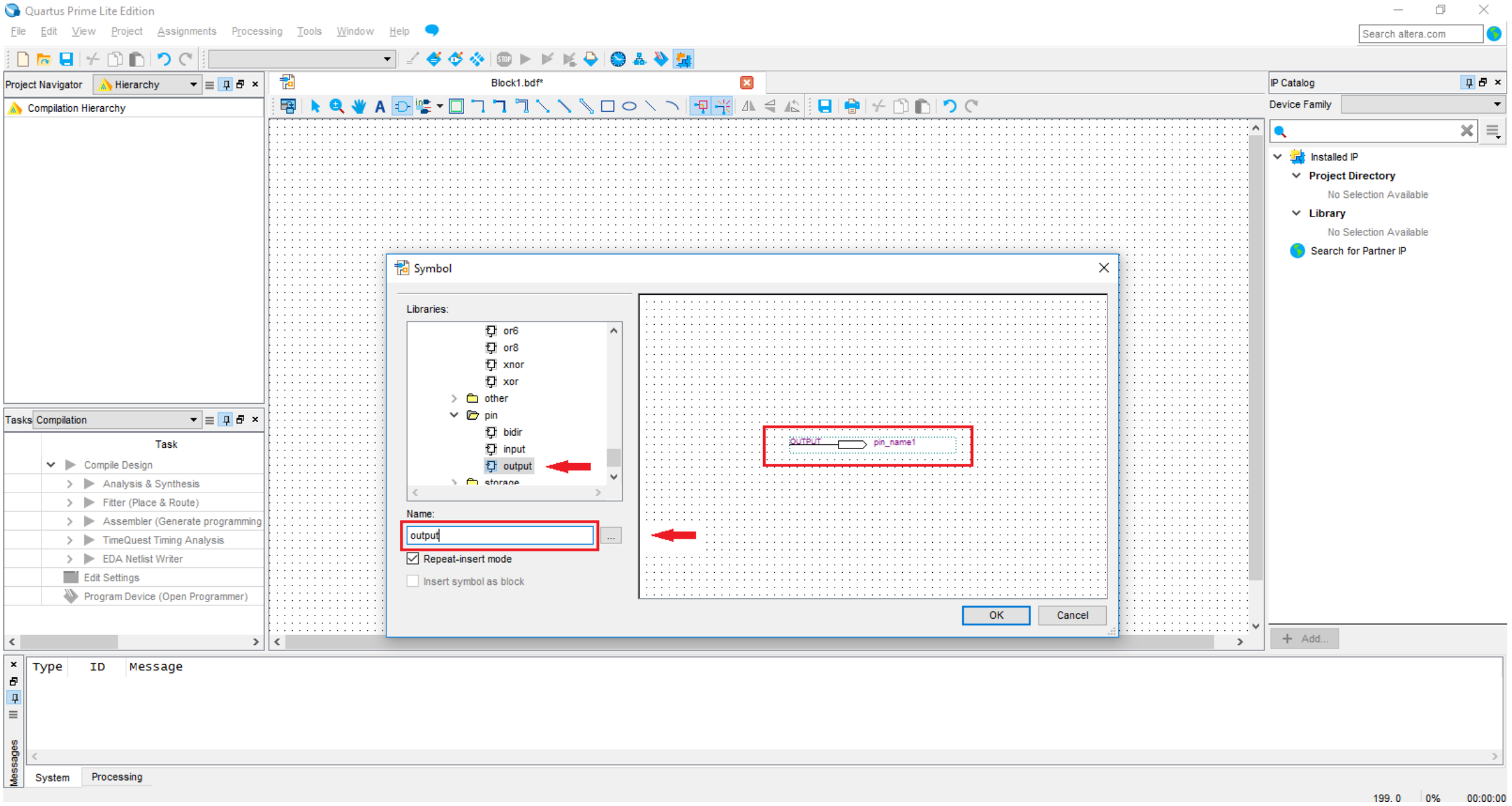
Example: 3 Input XOR (xor3)



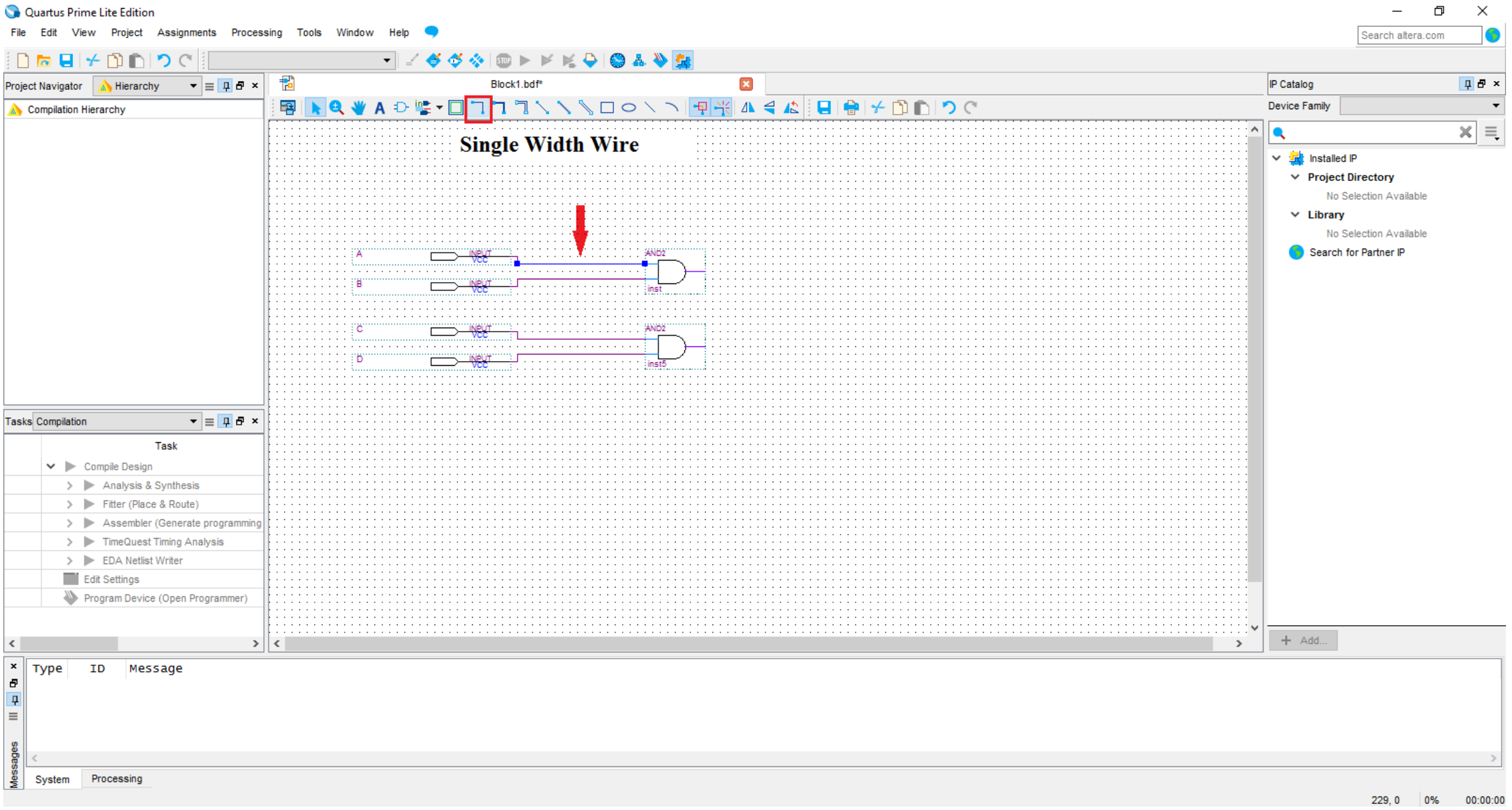
Example: Input



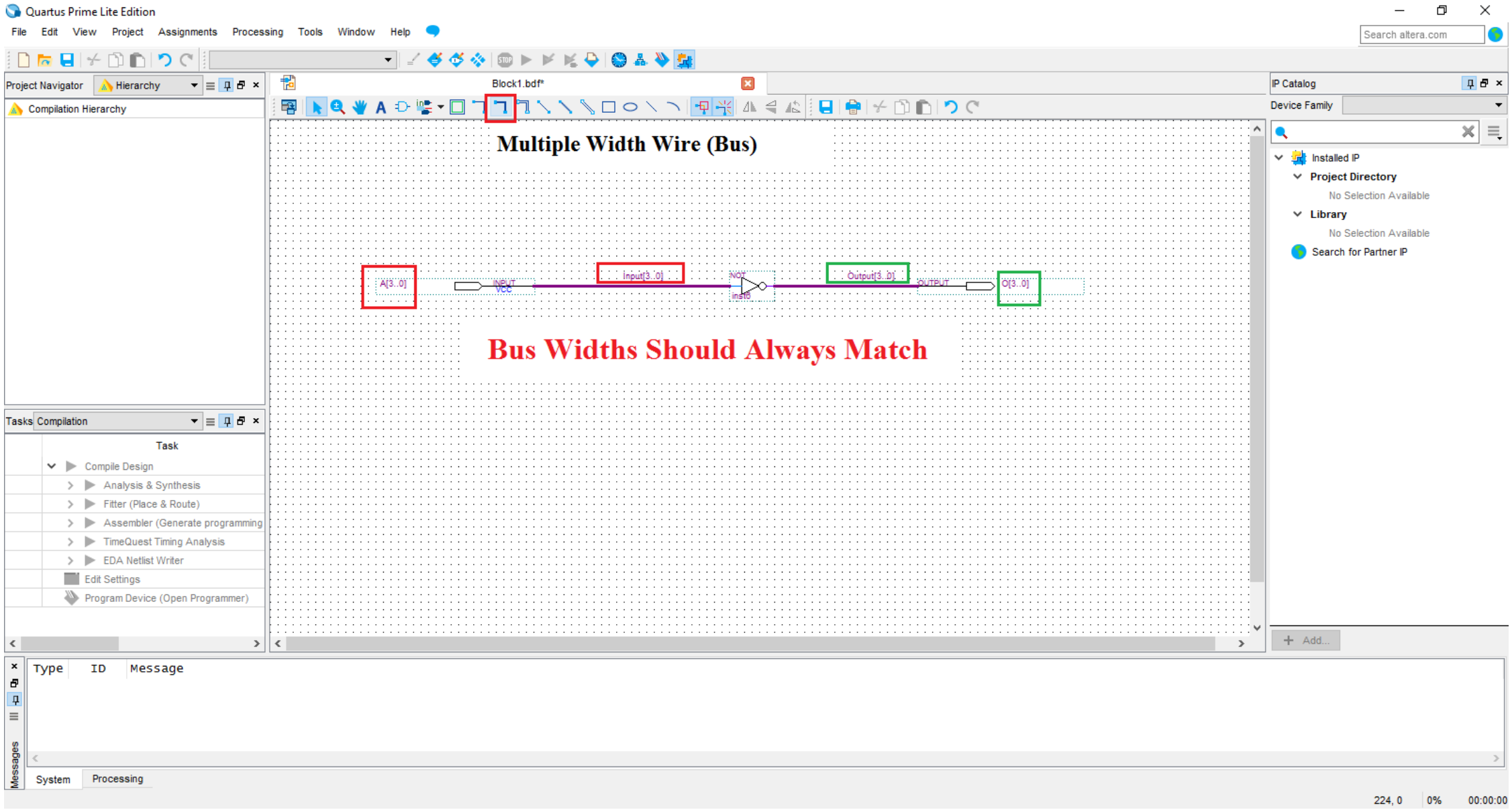
Example: Output



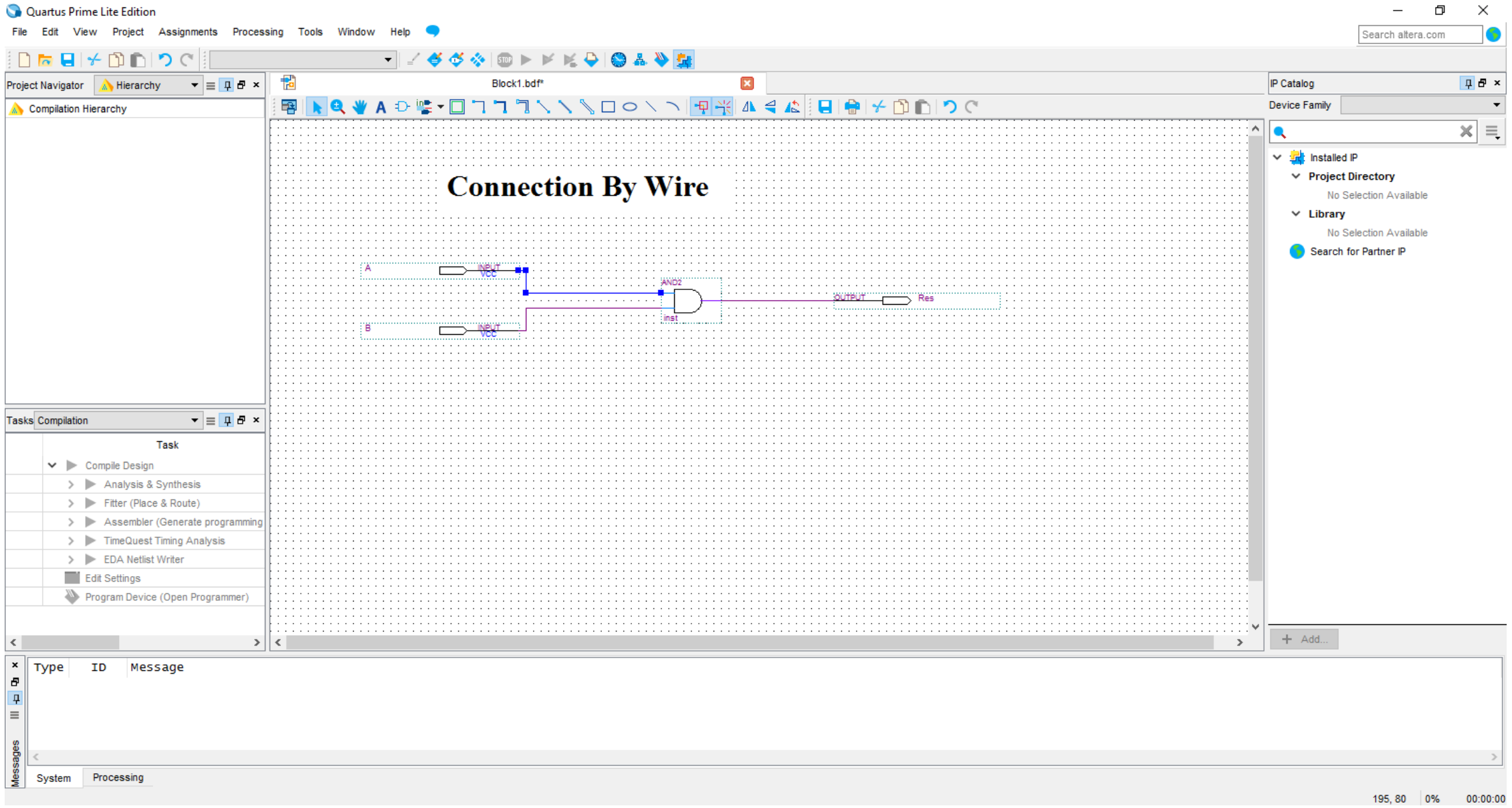
Example: Wiring



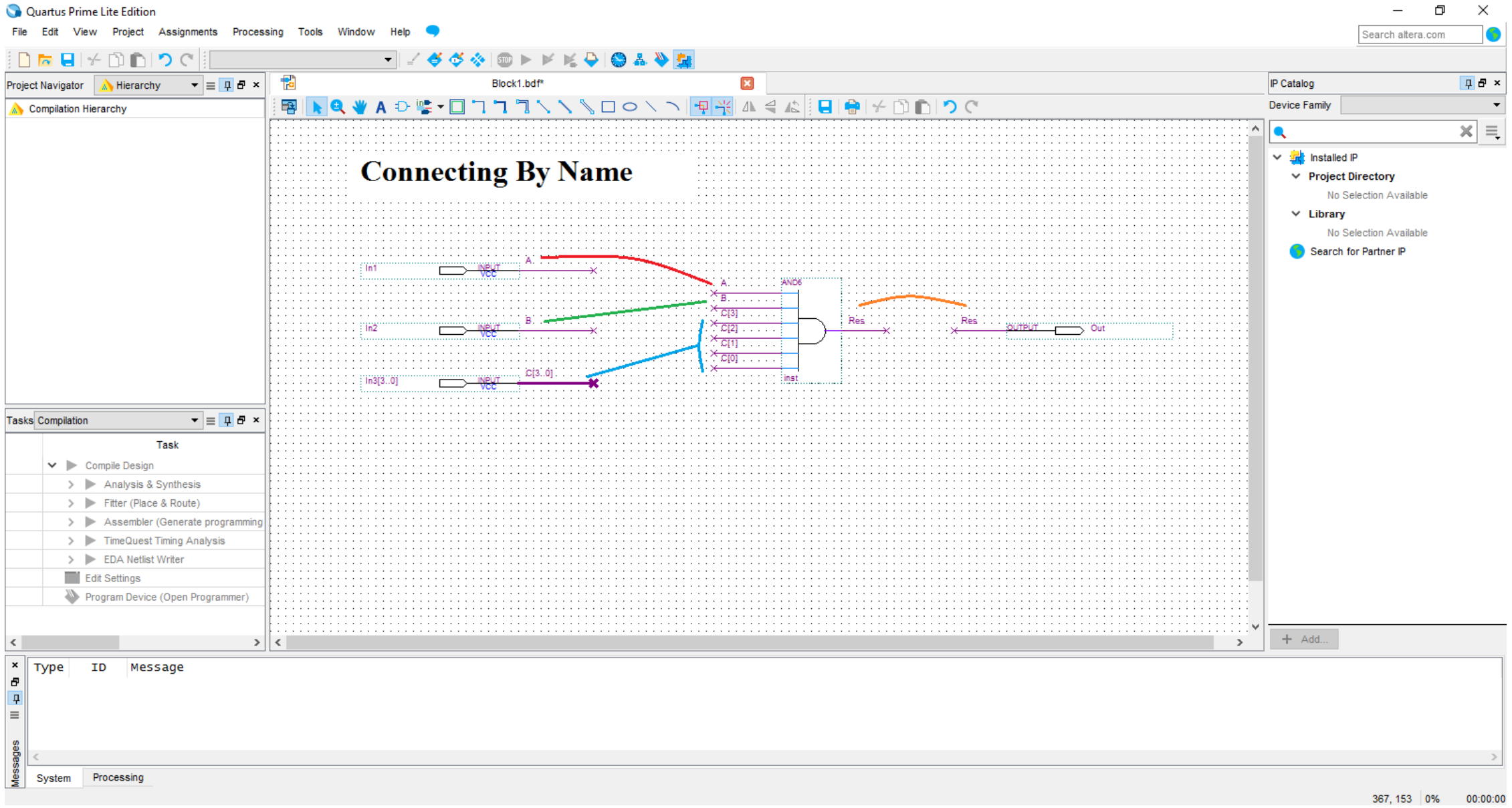
Example: Wiring (Bus)



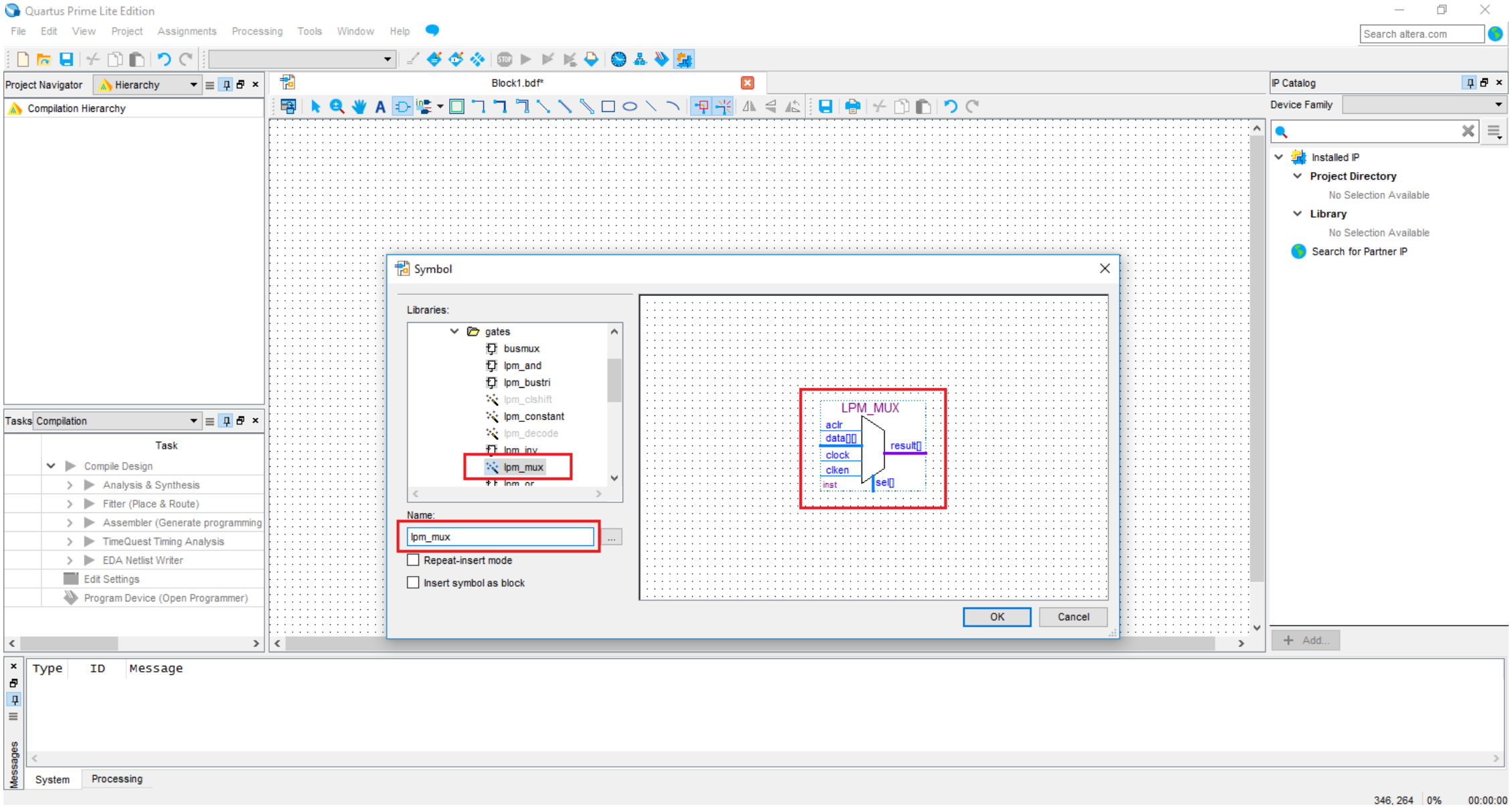
Example: Connecting By Wire



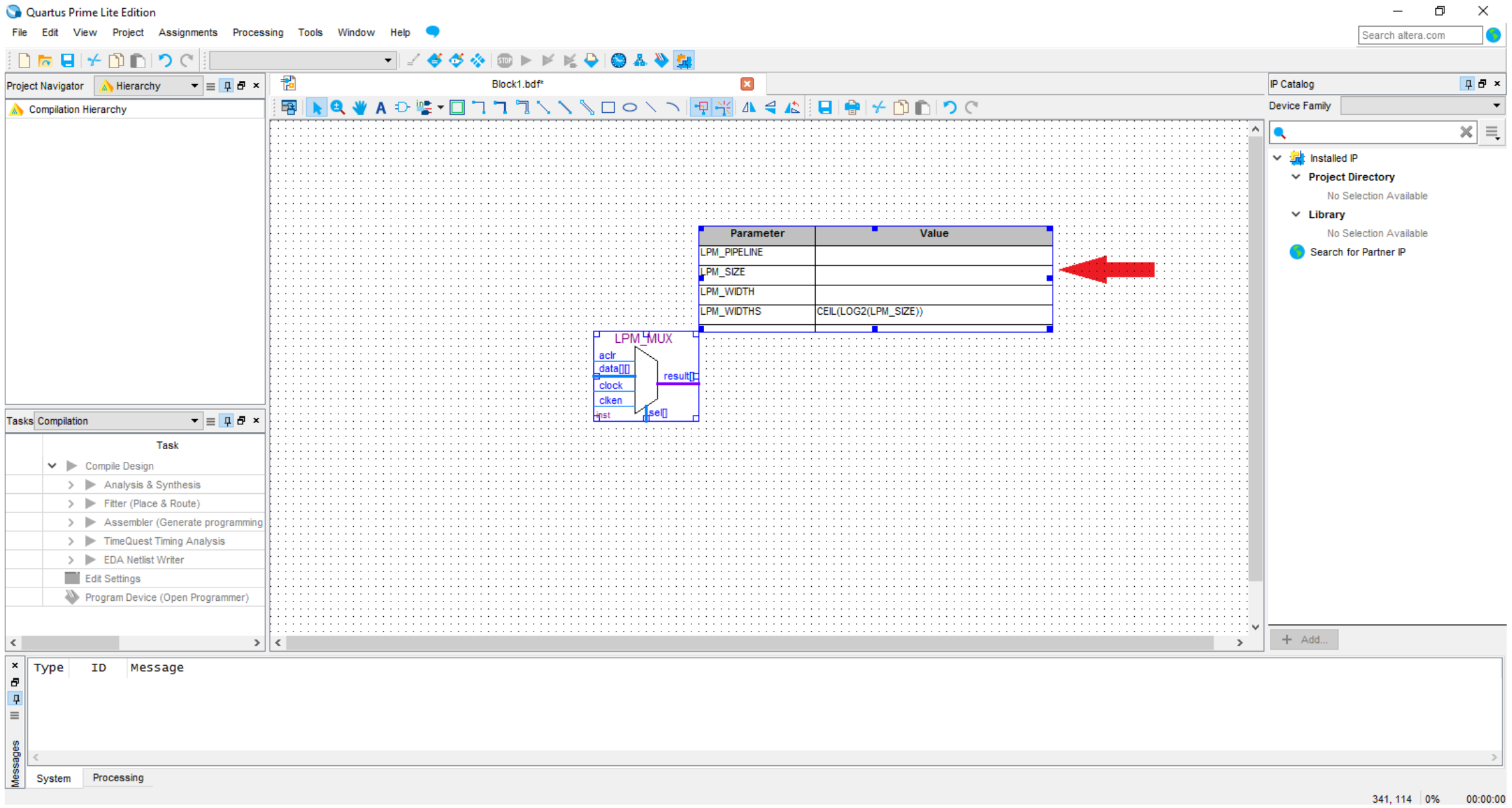
Example: Connecting By Name



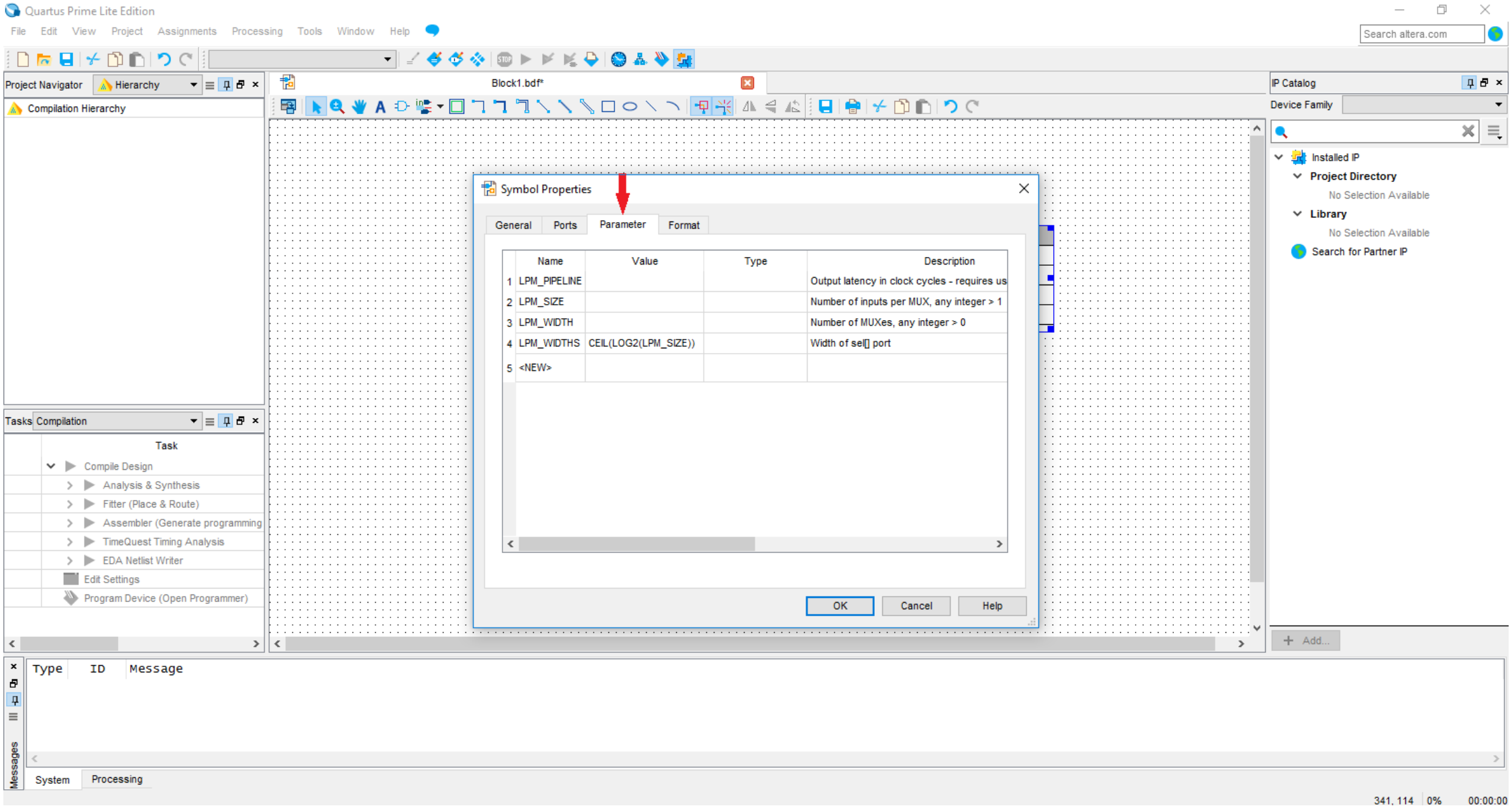
Example: Multiplexer (lpm Family)



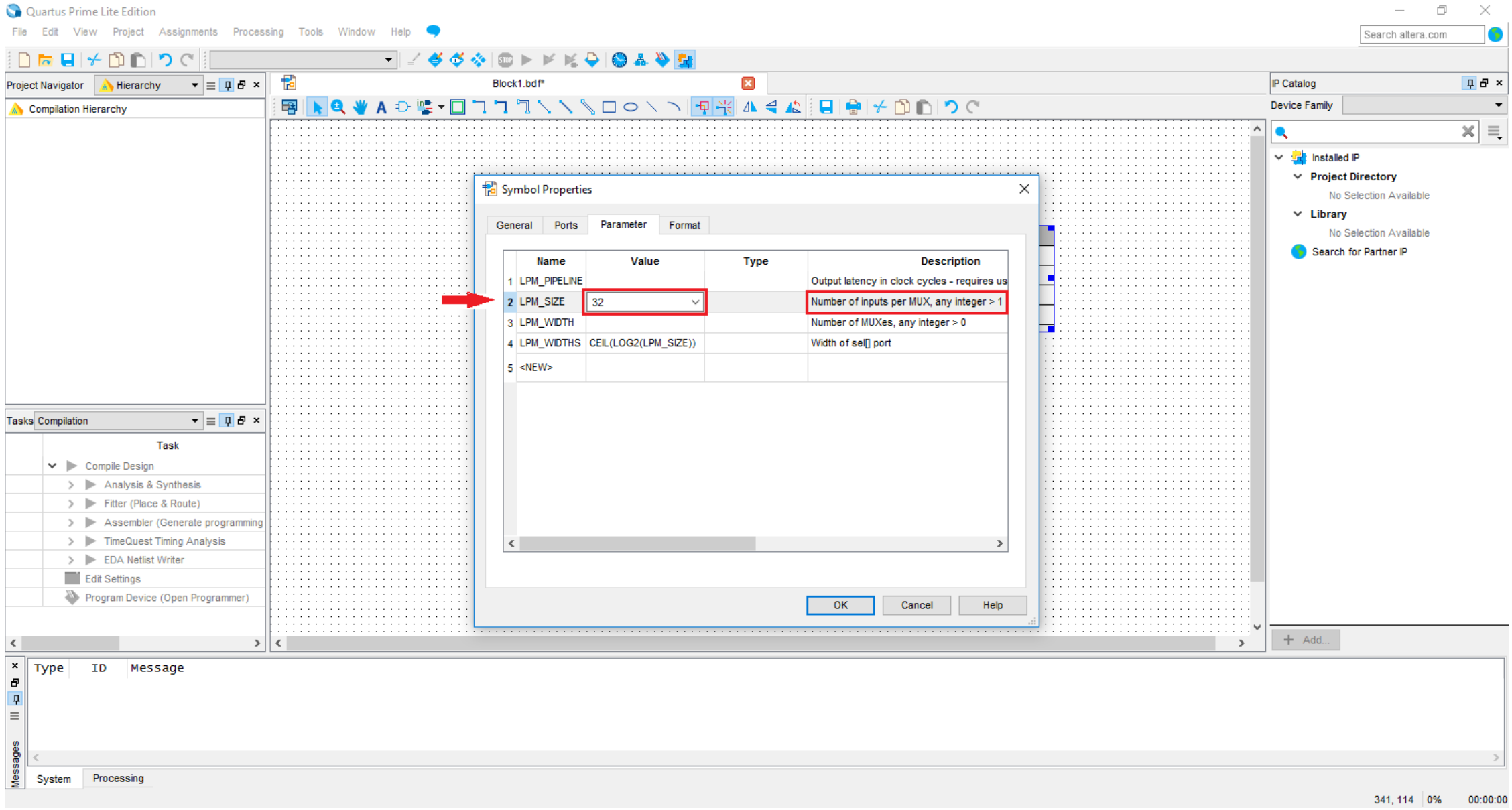
Example: Multiplexer (lpm Family)



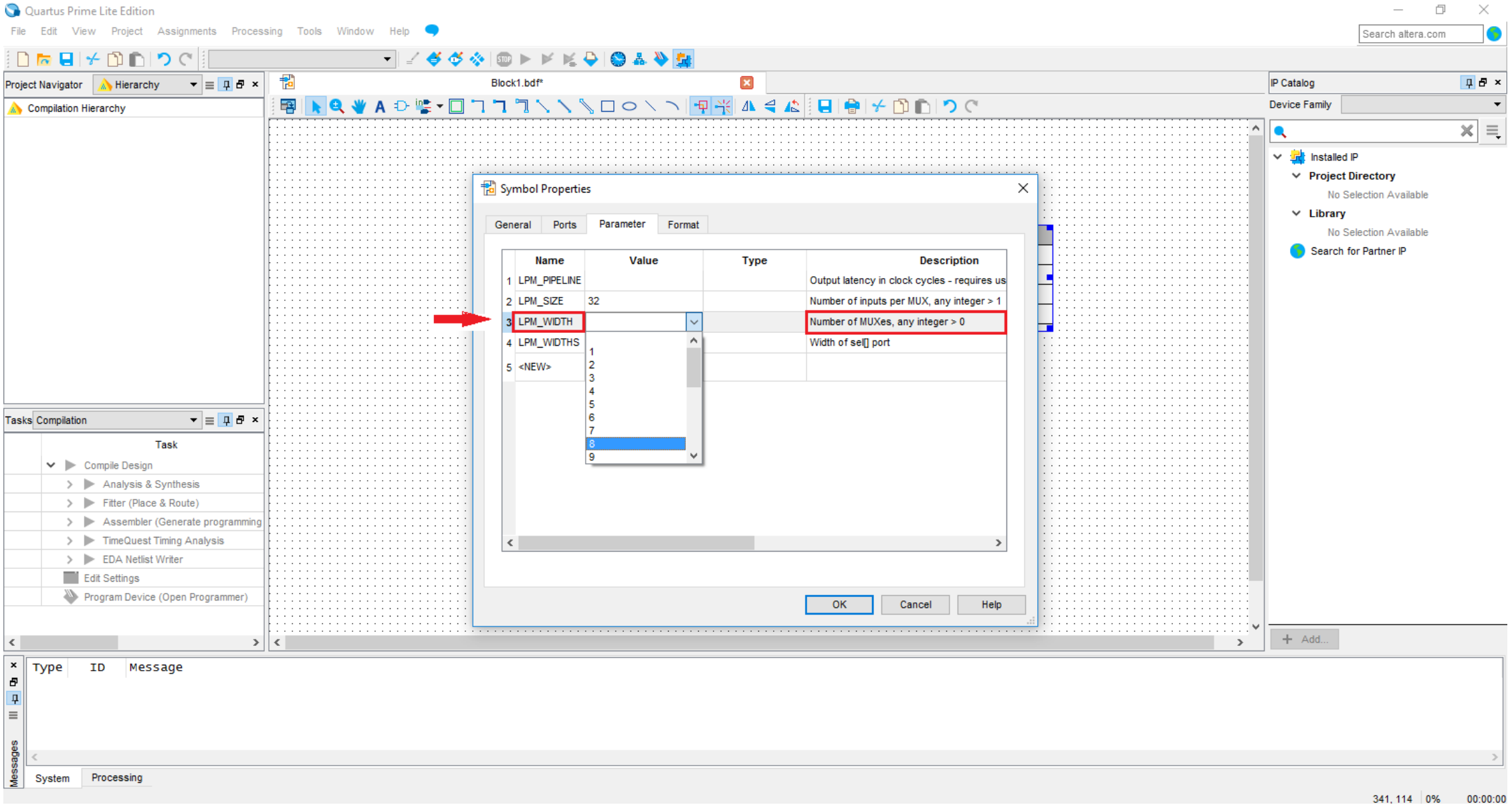
Example: Multiplexer (lpm Family)



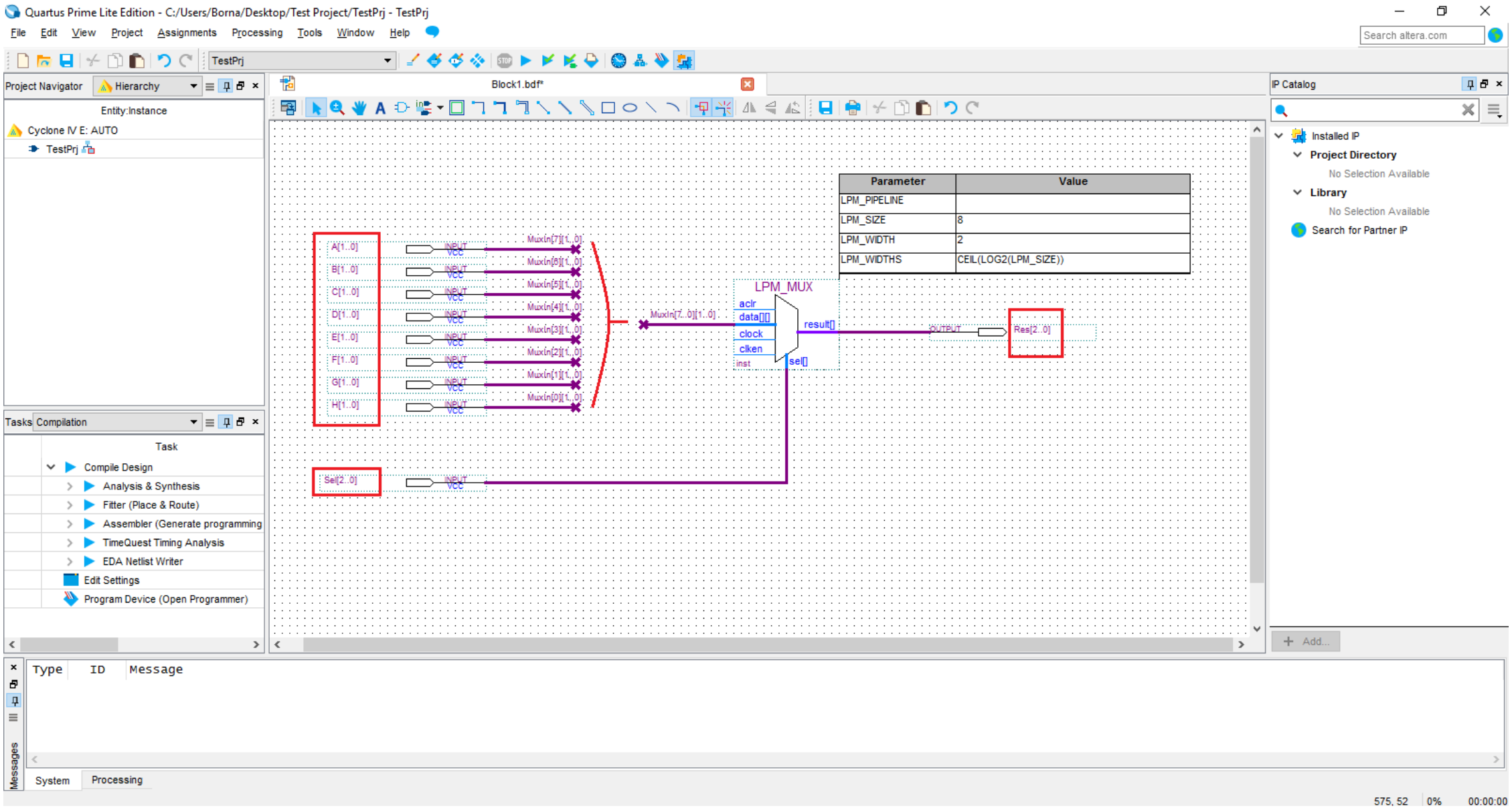
Example: Multiplexer (lpm Family)



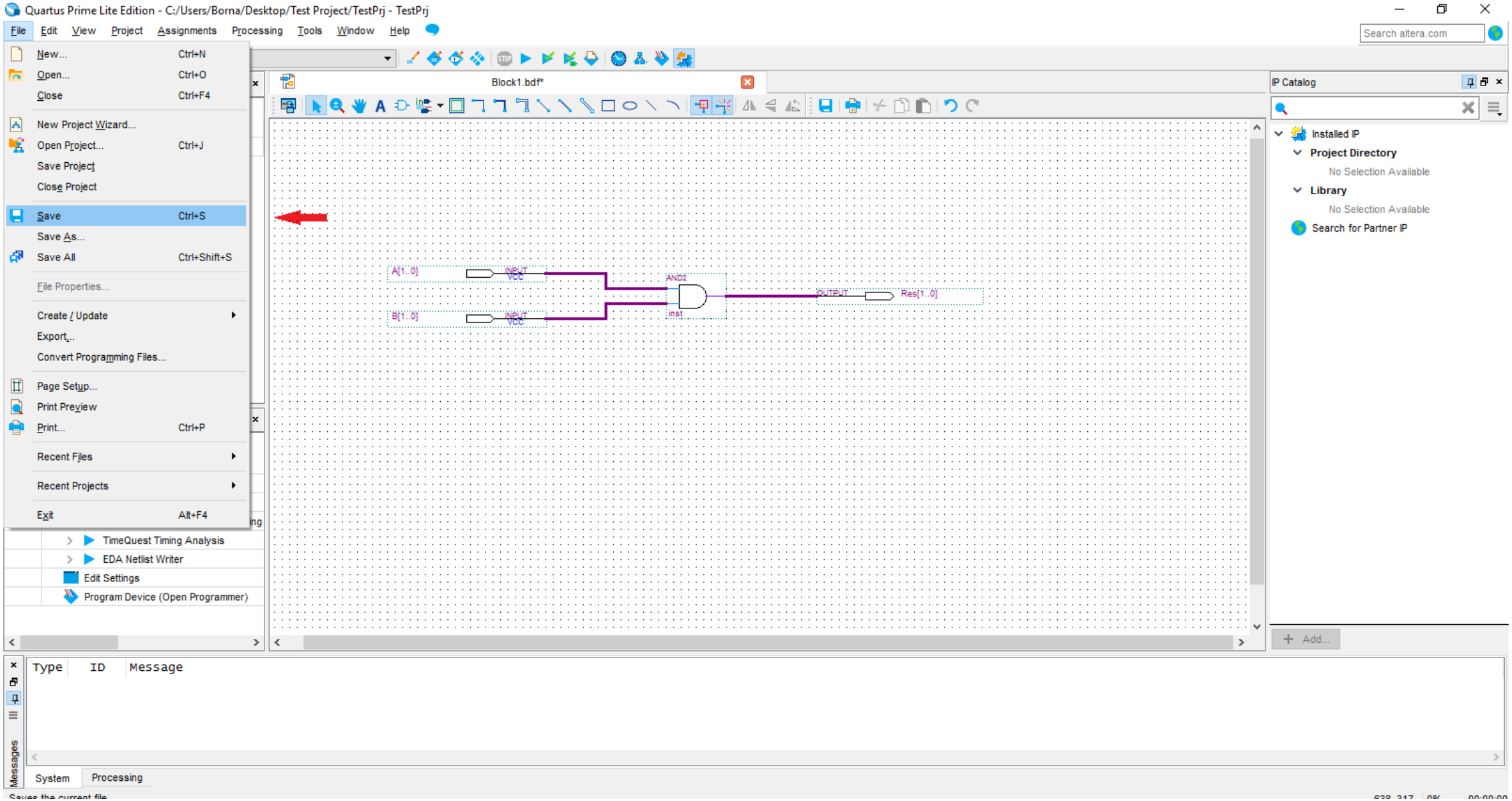
Example: Multiplexer (lpm Family)



Example: Multiplexer (lpm Family)

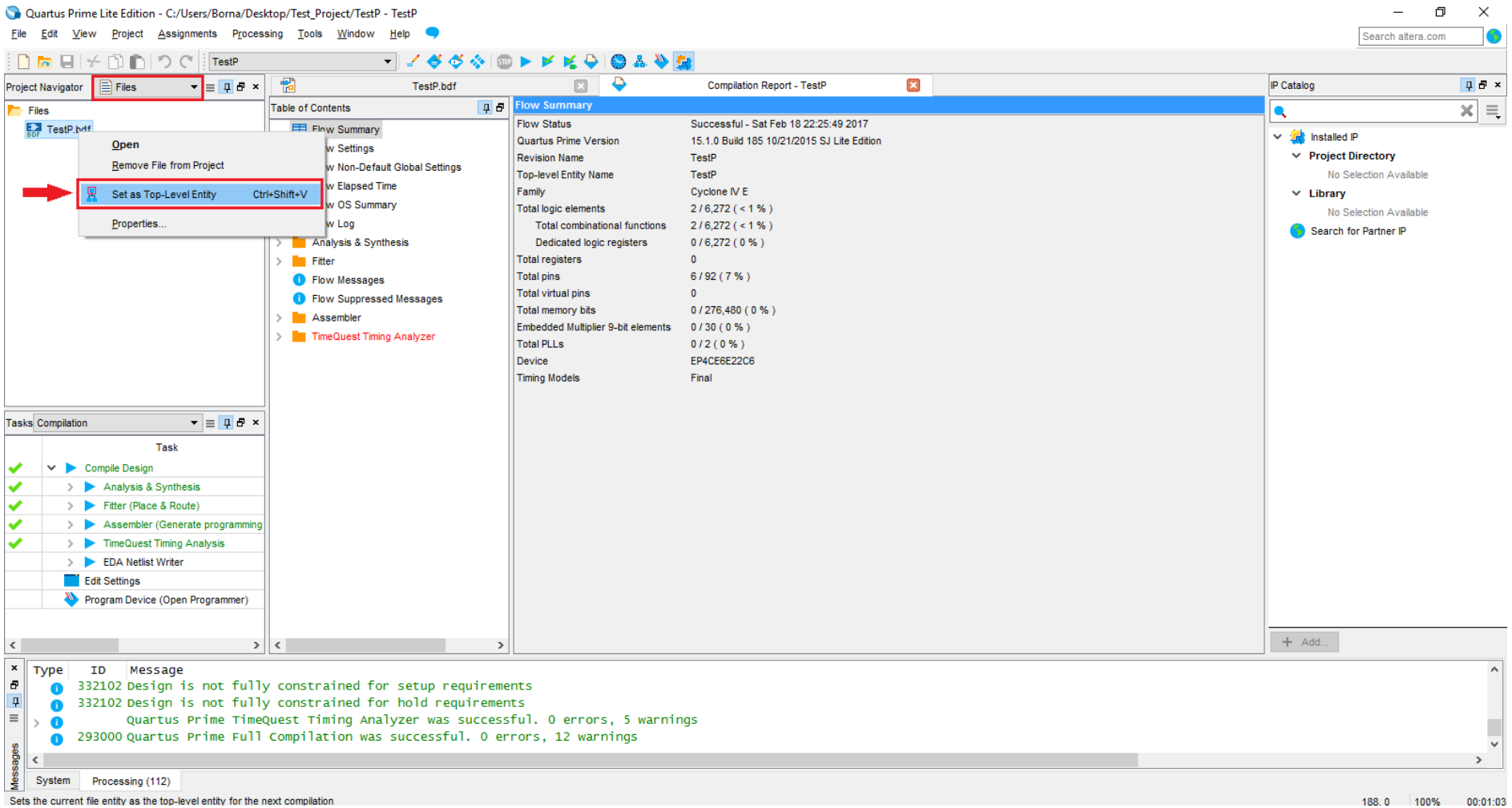


Save Your Design (.bdf file)

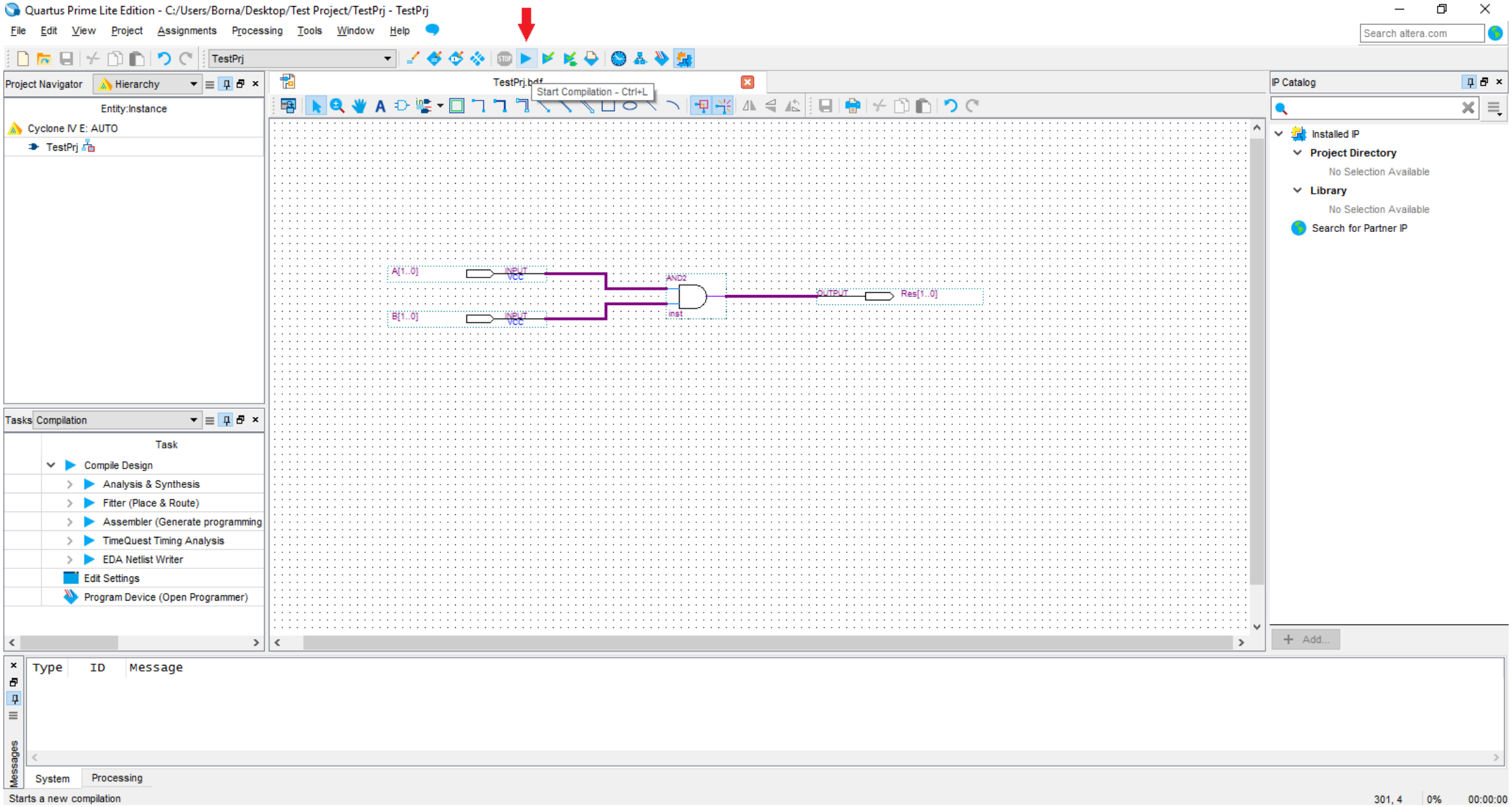


Compile Your Design

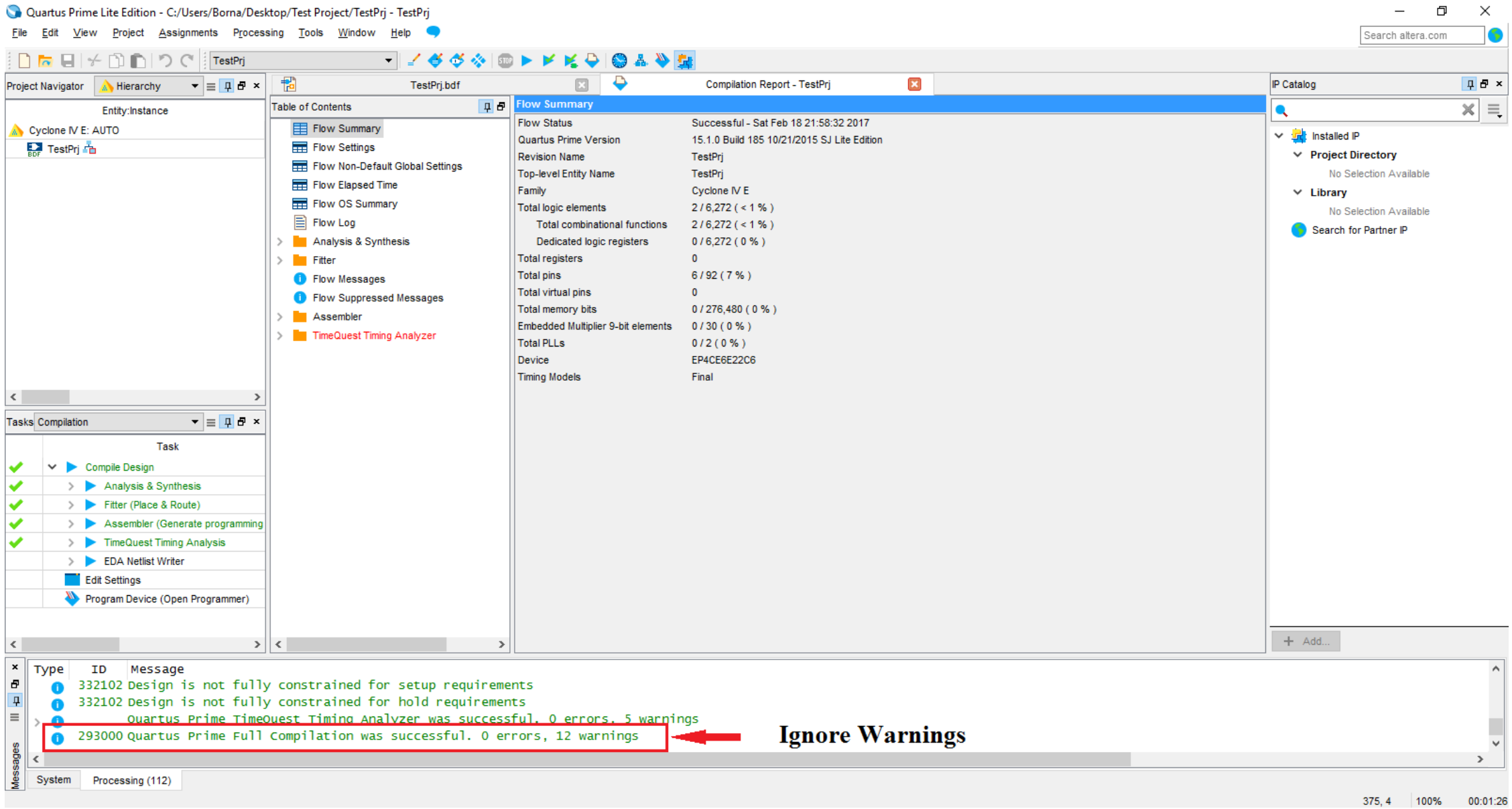
- Set Your Design as Top Level Entity



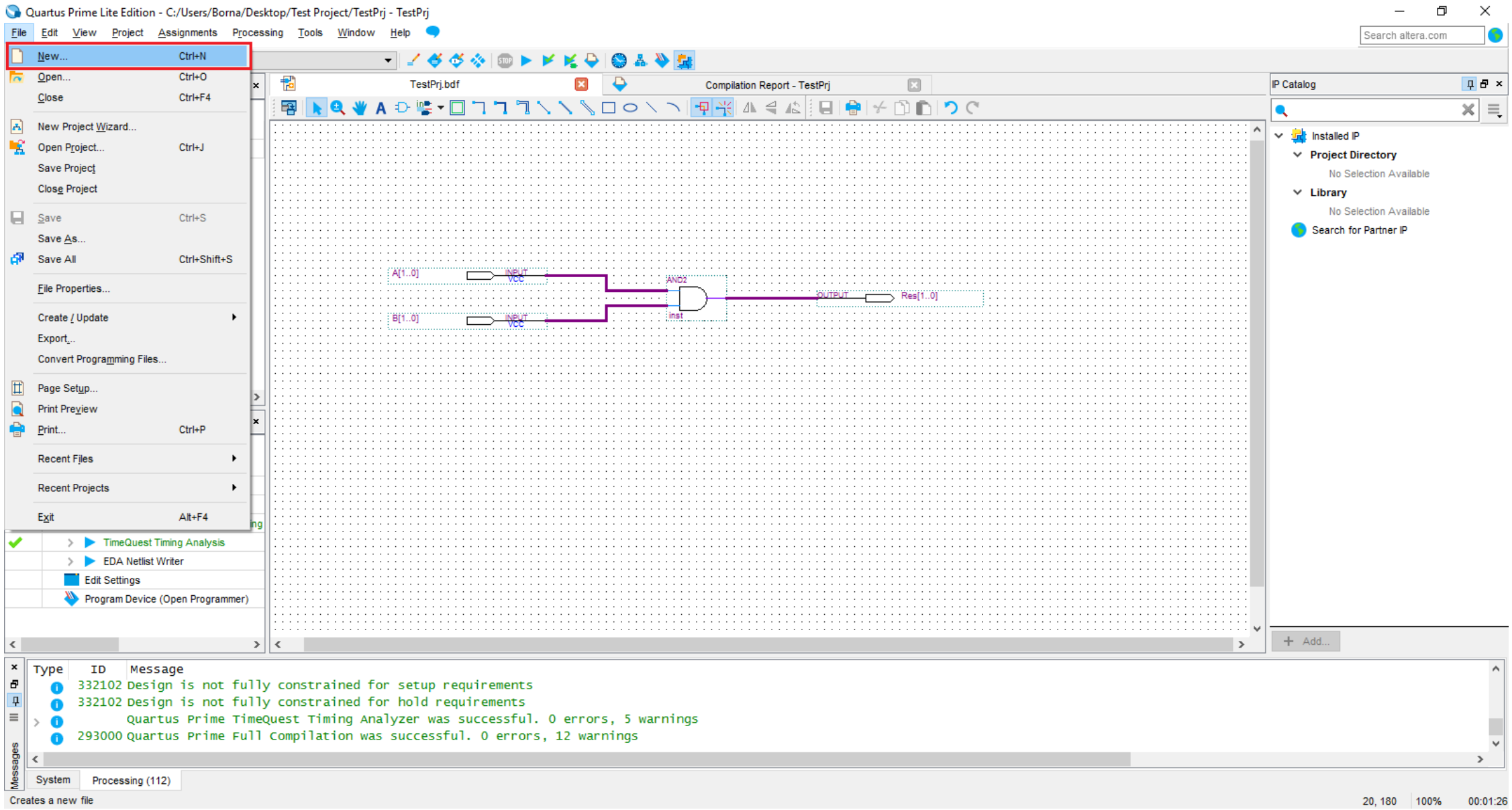
Compile Your Design



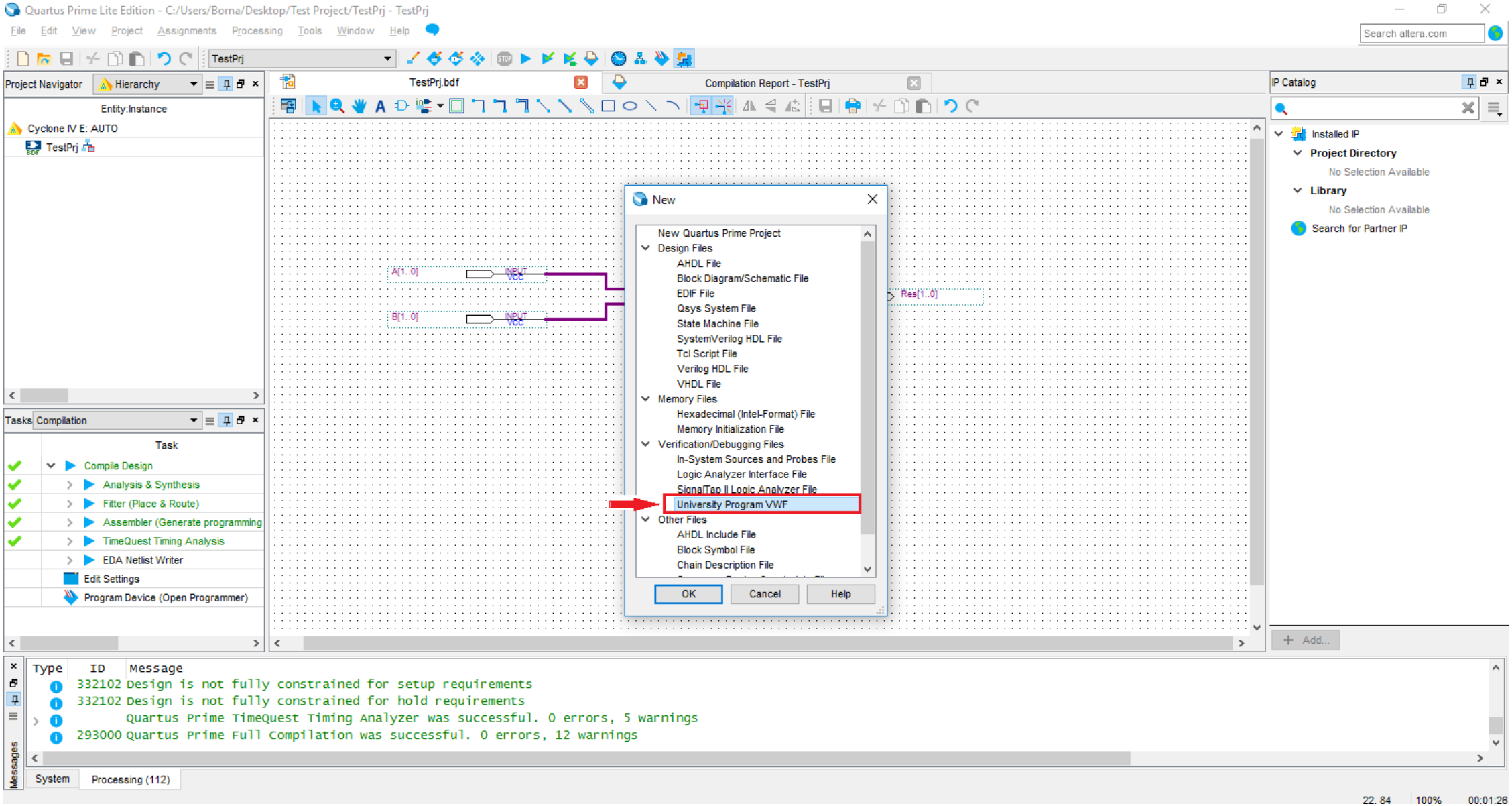
Compile Your Design, After a While …



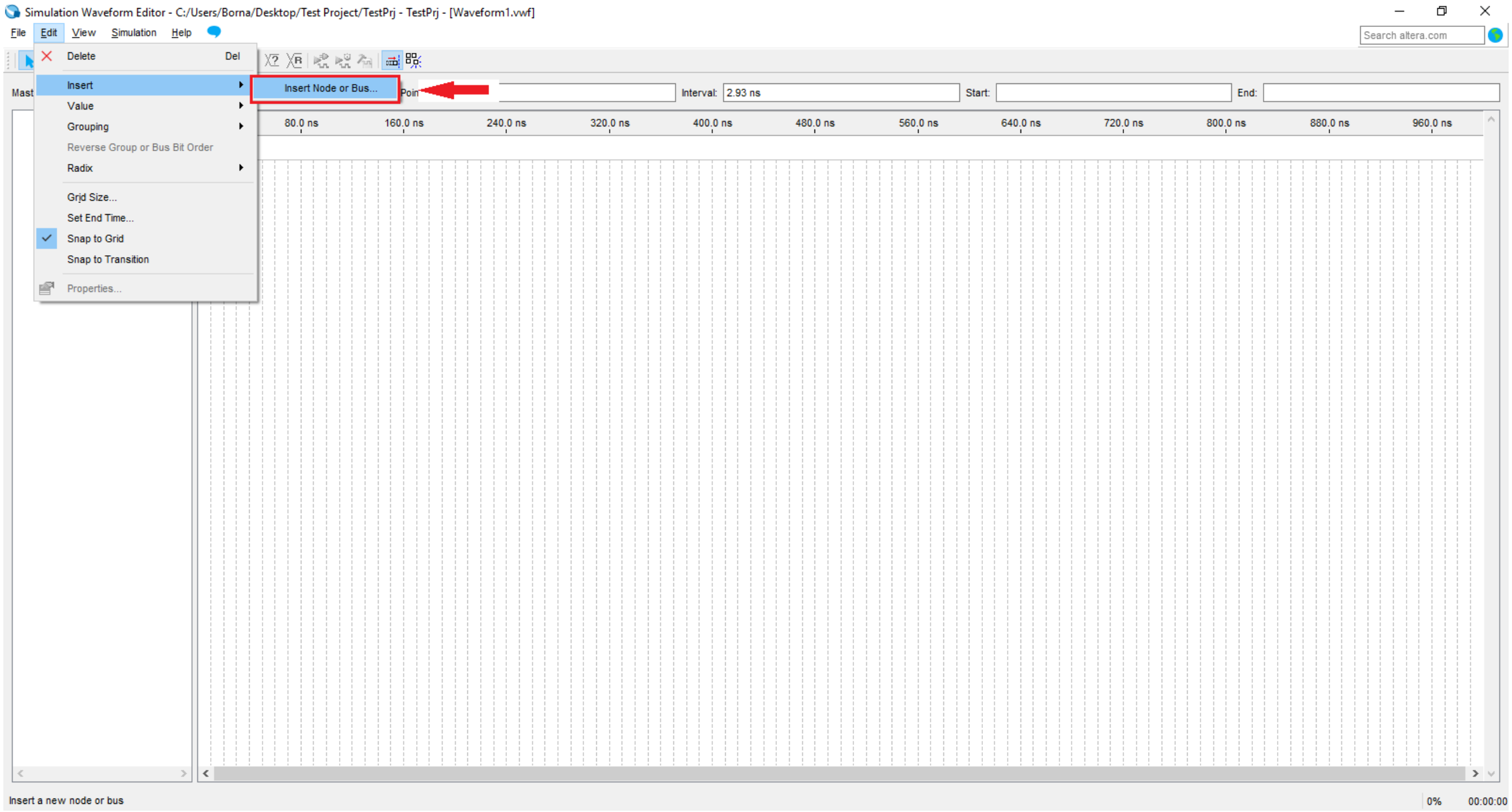
Create a Waveform



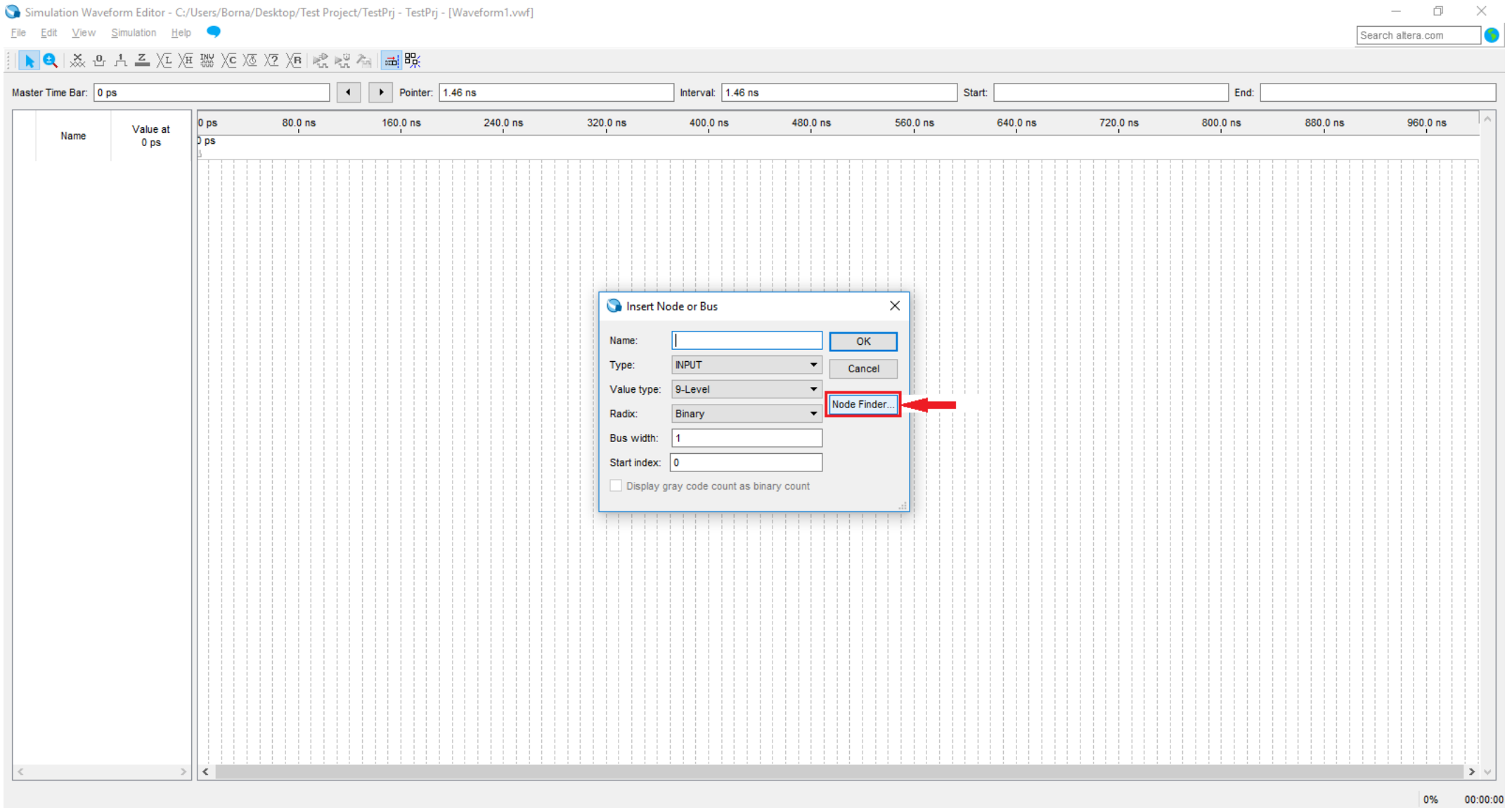
Create a Waveform



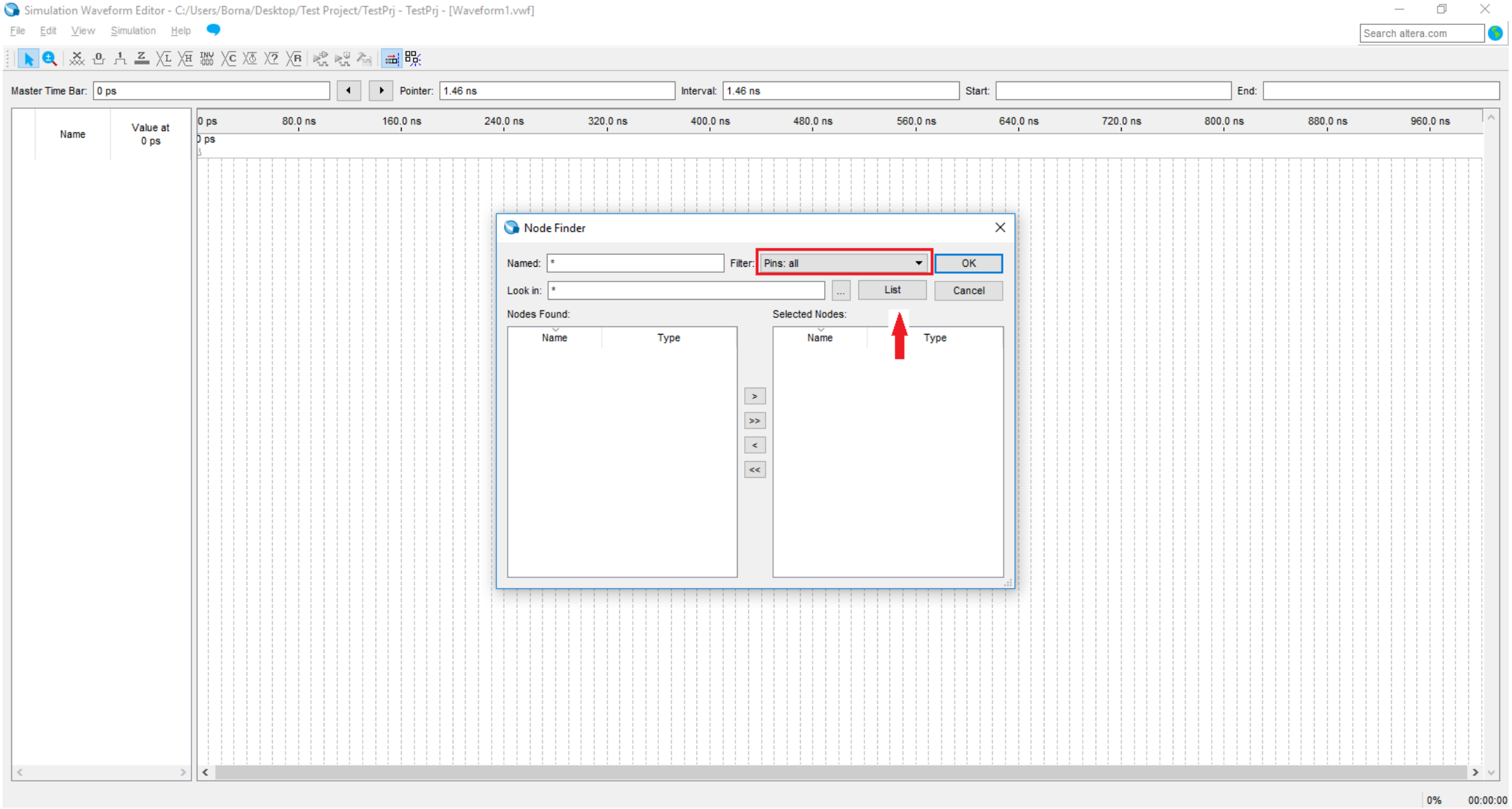
Add Signals & Buses



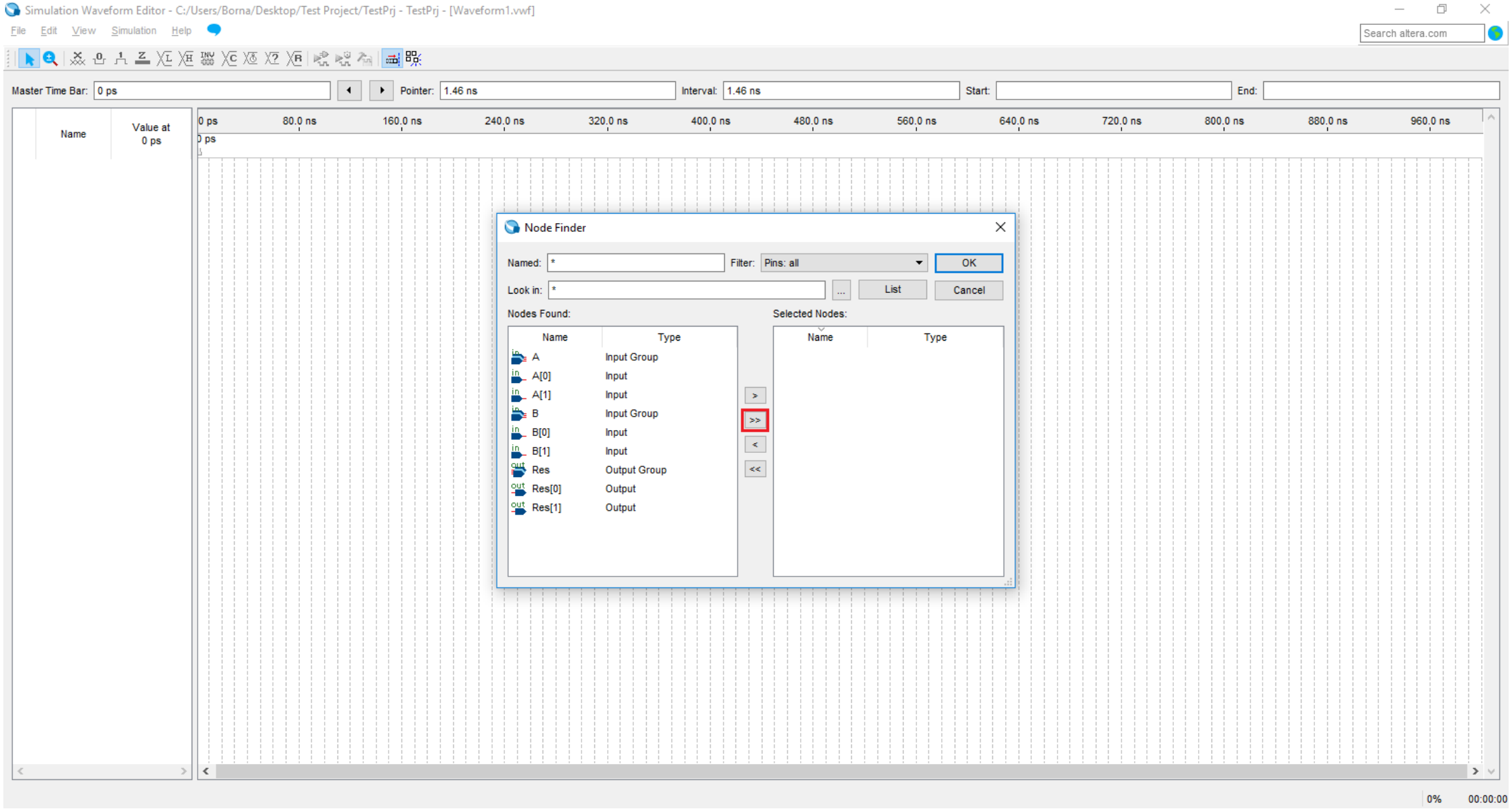
Add Signals & Buses



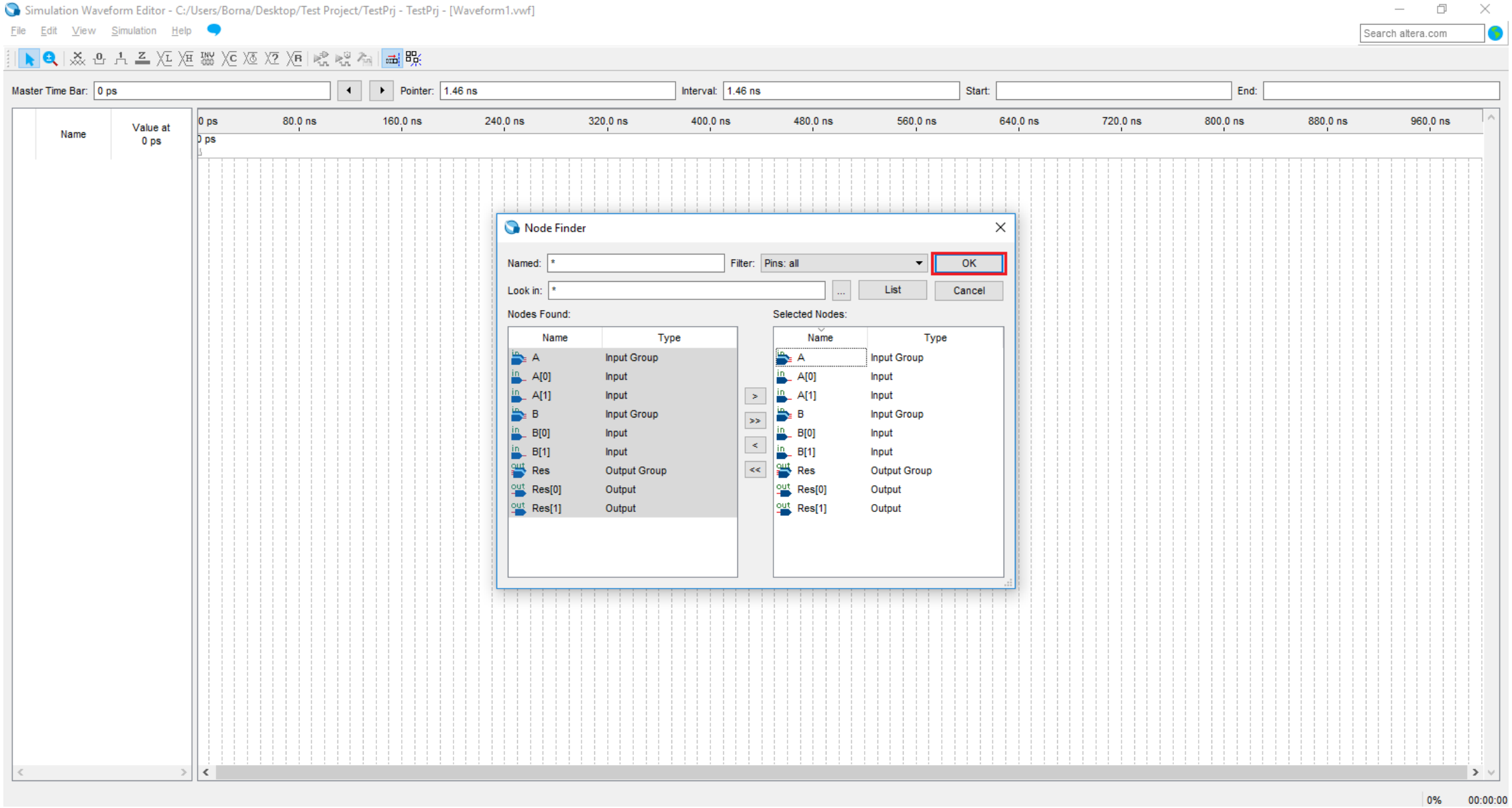
Add Signals & Buses



Add Signals & Buses

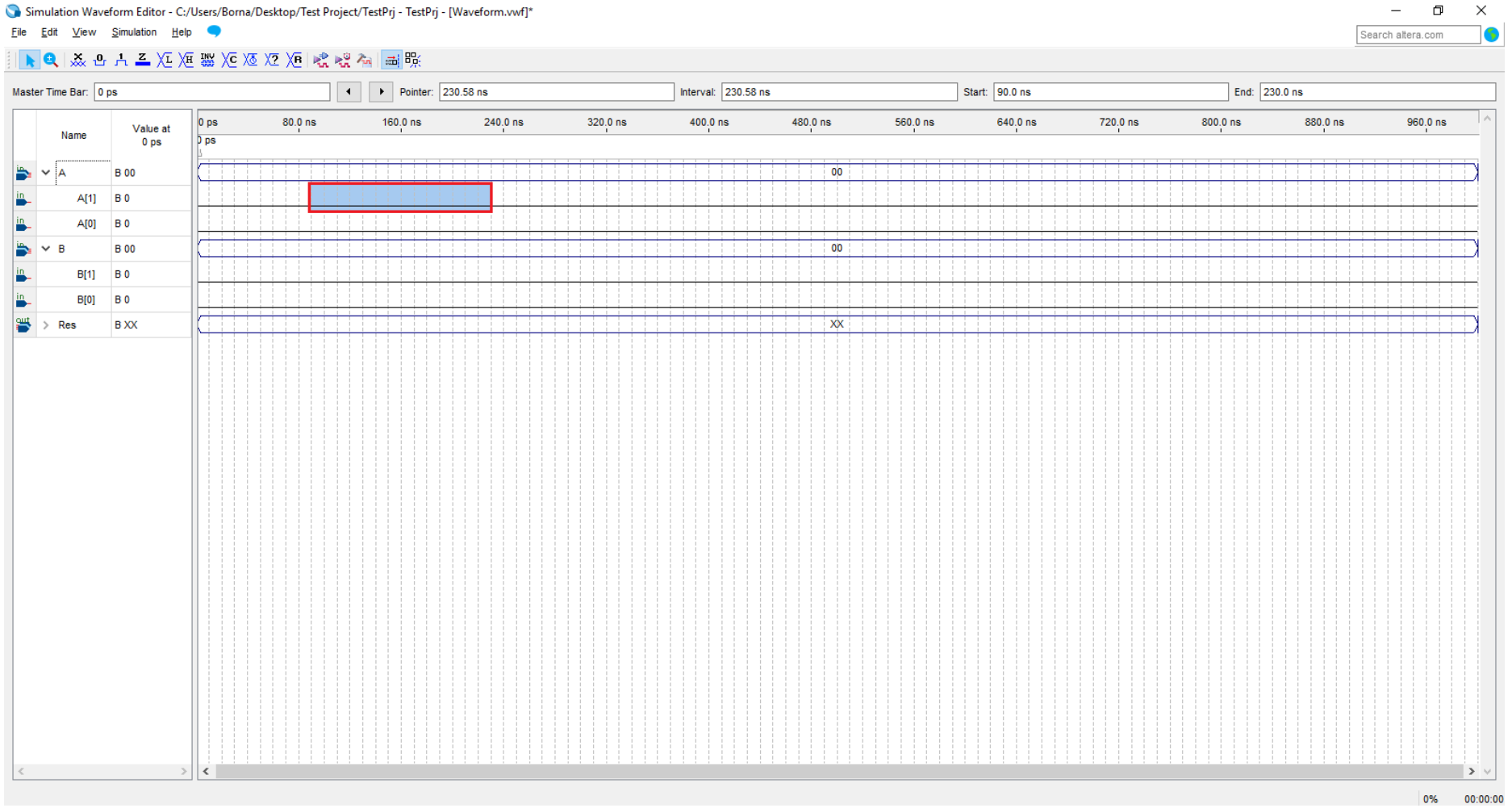


Add Signals & Buses



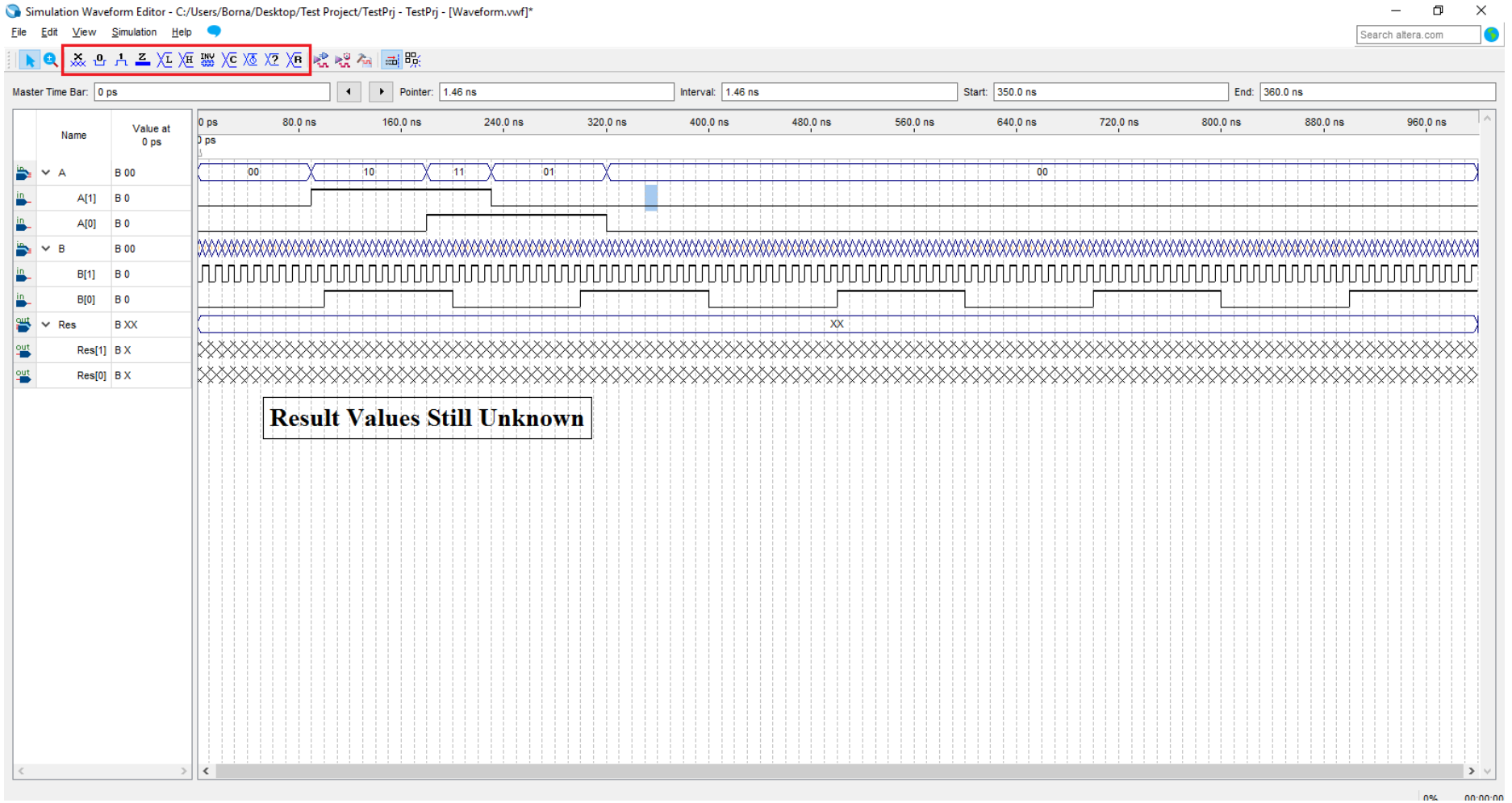
Assign Value to Input Signals

- Select Signal and Radius

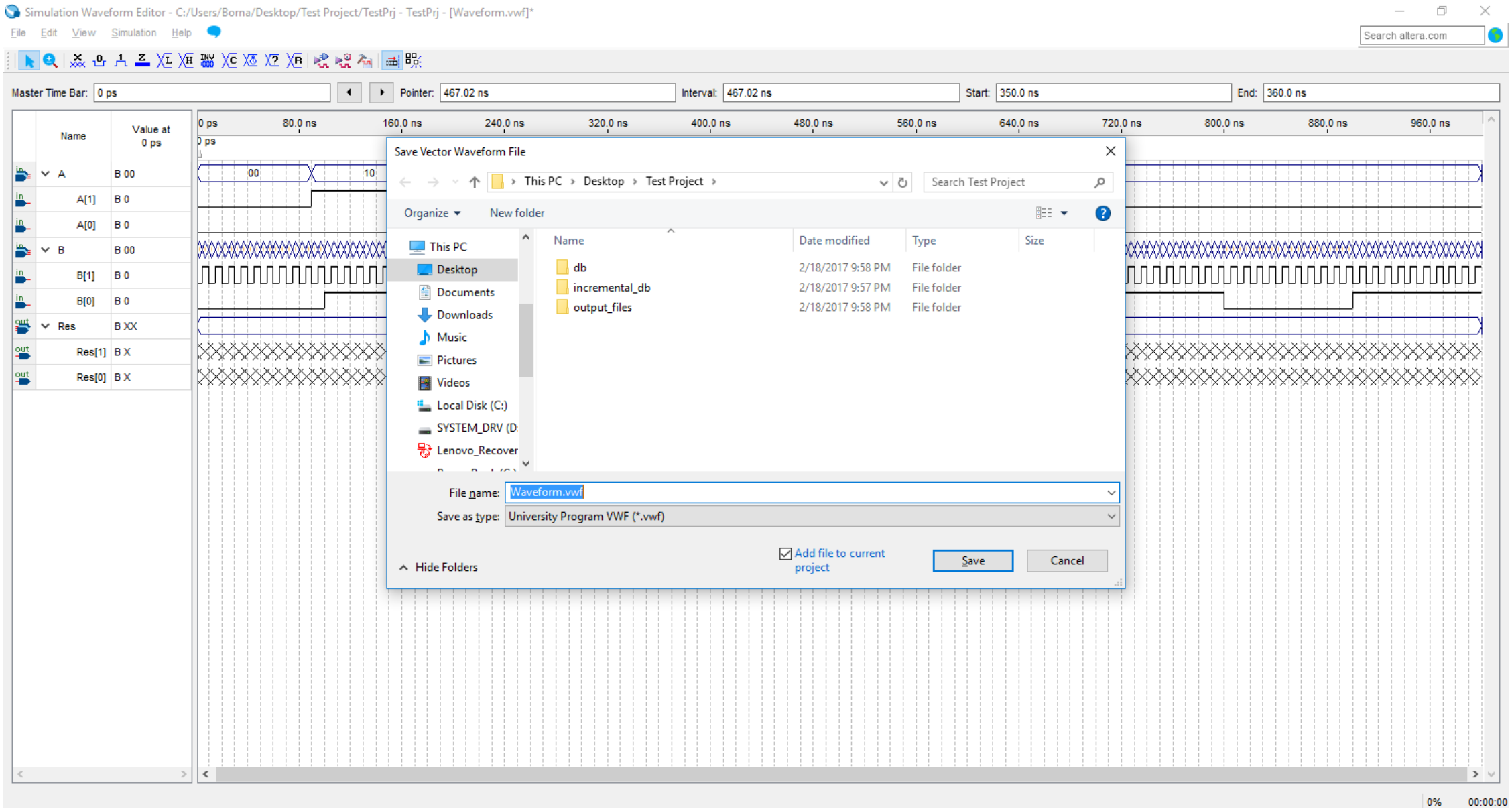


Assign Value to Input Signals

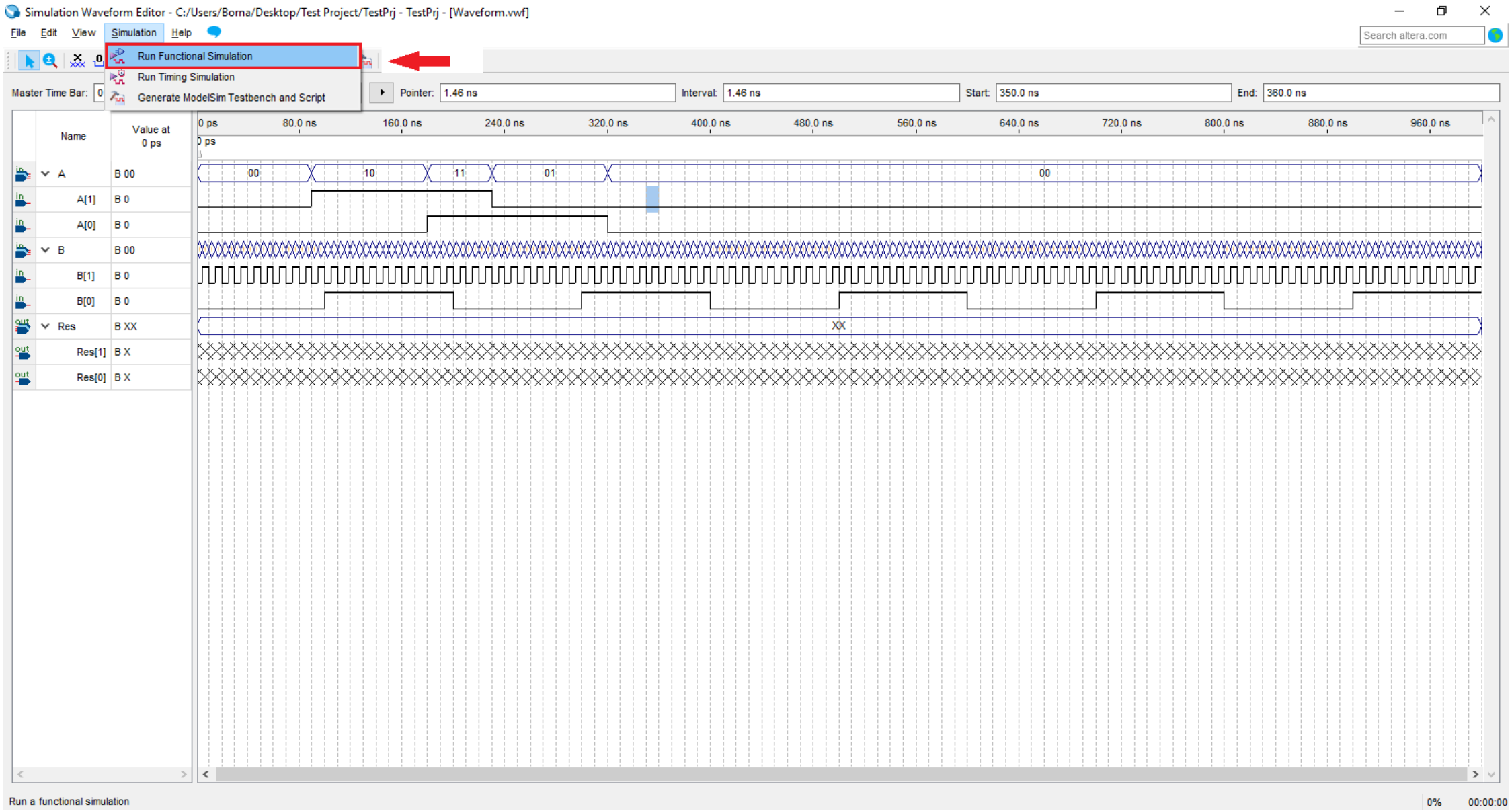
- Assign Value: 1, 0, High Z, Oscillating Signal, Clock, …



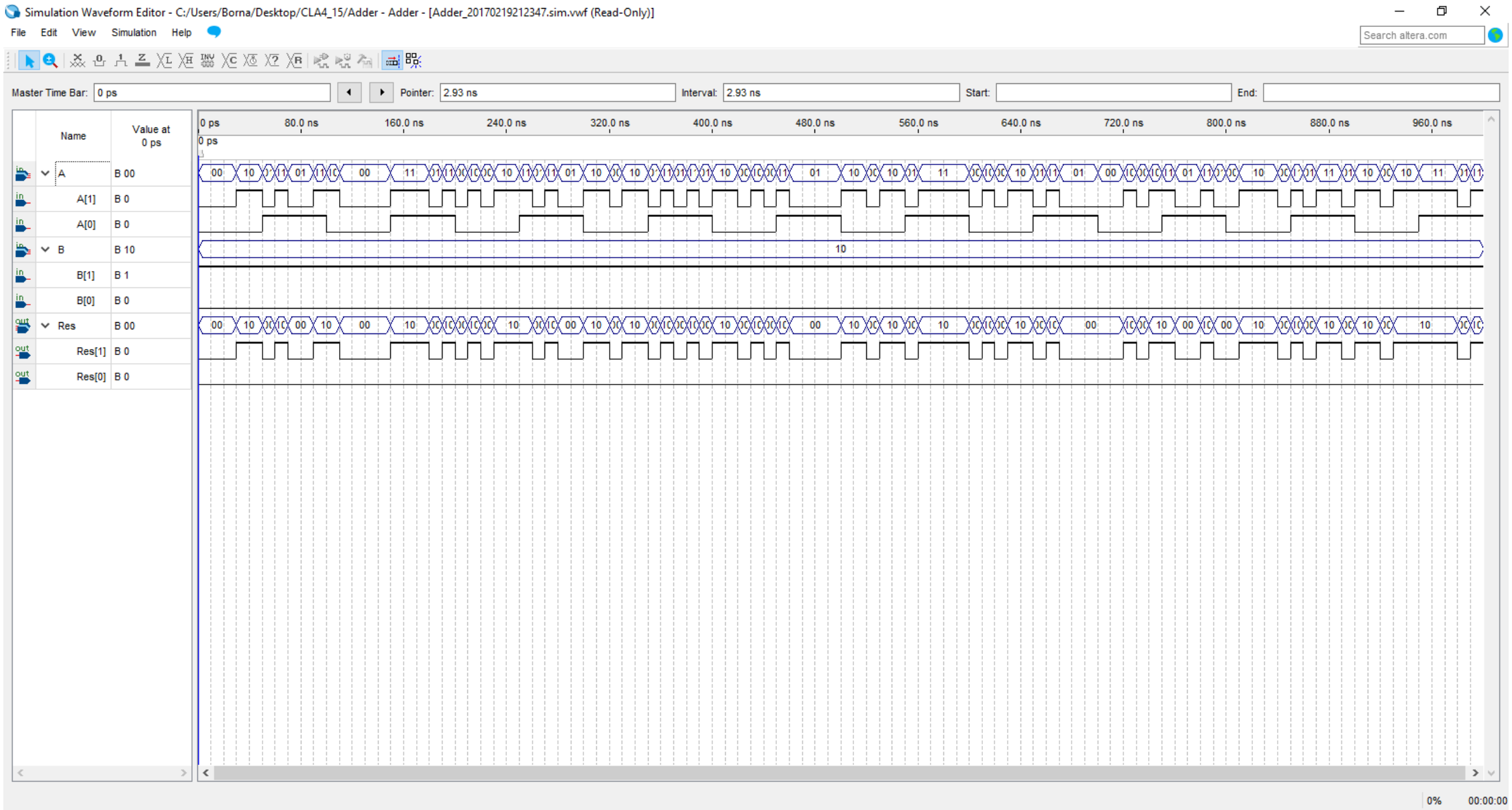
Save Waveform (.vwf file)



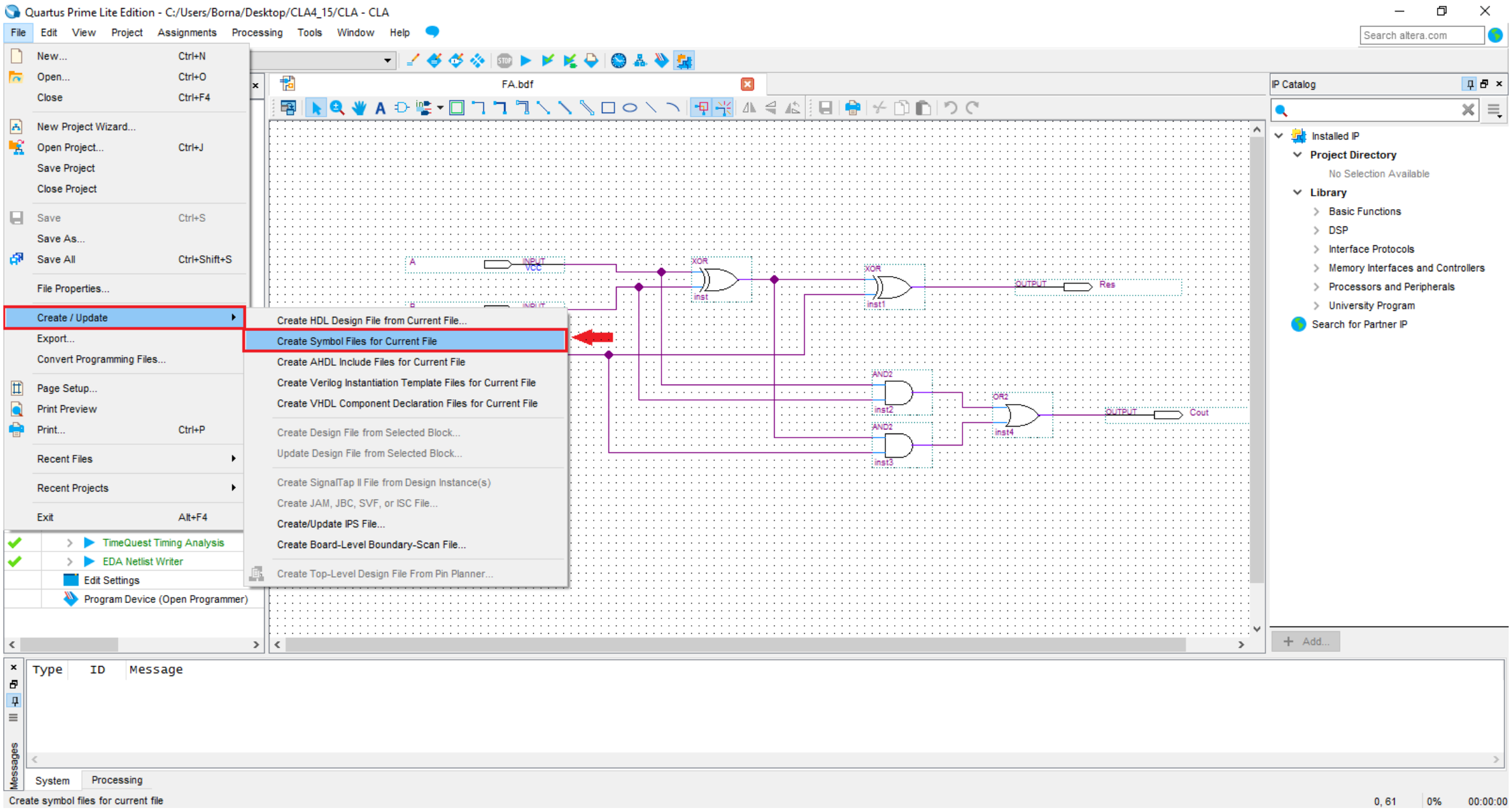
Simulate Waveform (Functional Simulation)



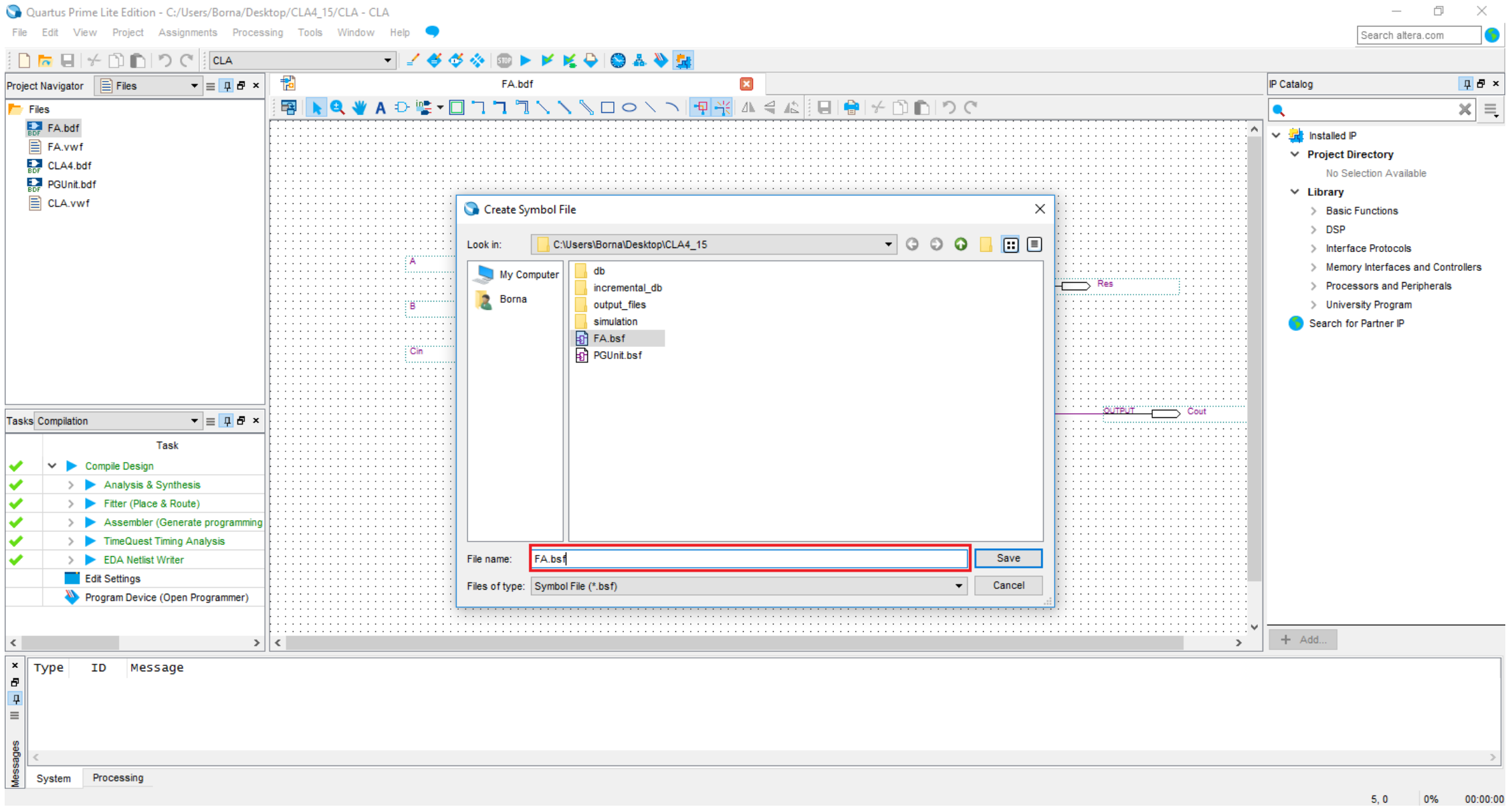
Simulation Results



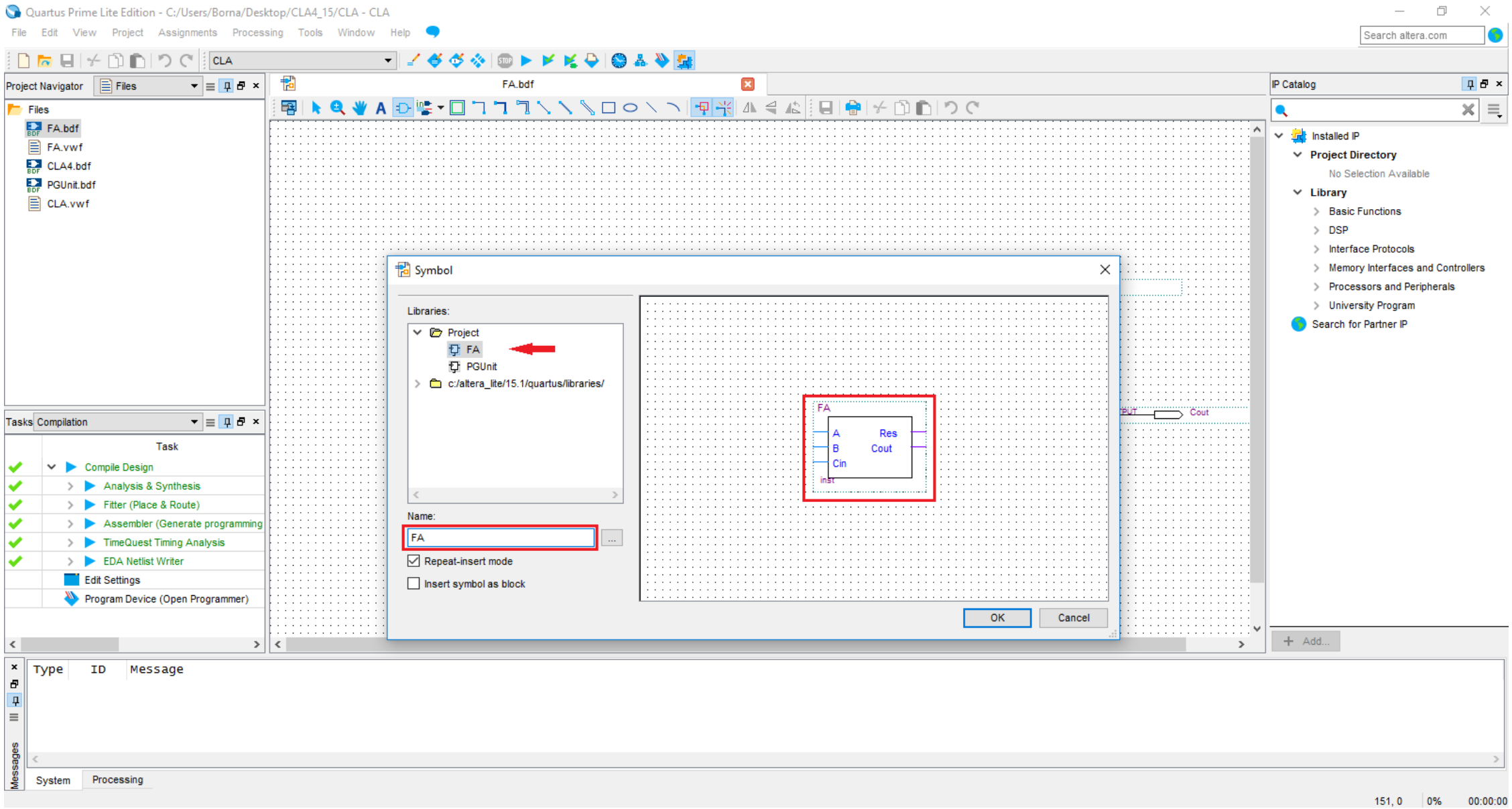
Build an Instance of Your Own



Save It As a .bsf File



Use It As a Regular Module



An Example of 4bit Carry Look Ahead Adder Is Included

Any Questions?