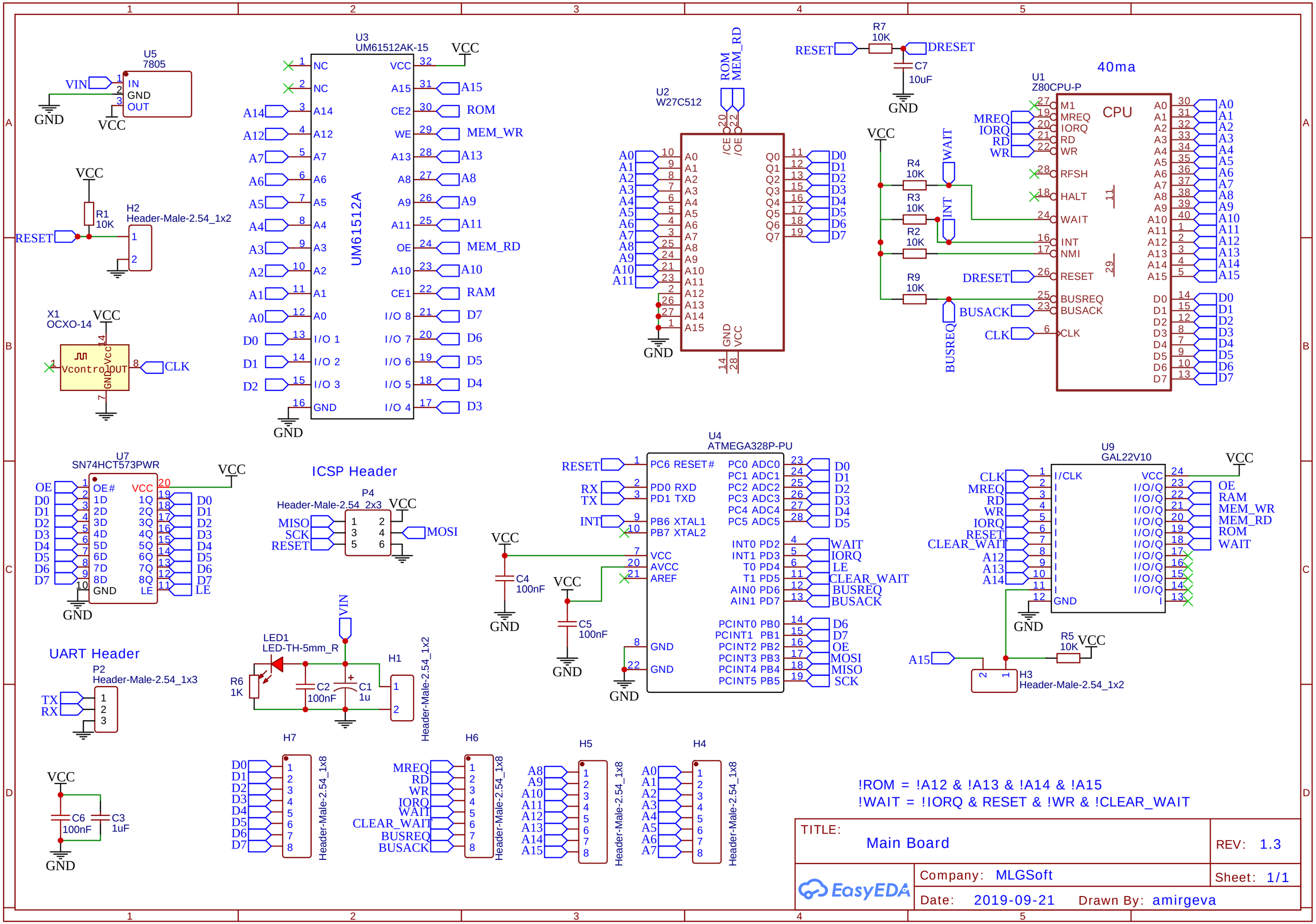
U5
7805
VIN
IN
GND
OUT
GND
VCC
U3
UM61512AK-15
UM61512A
NC
A14
A12
A7
A6
A5
A4
A3
A2
A1
A0
D0
D1
D2
GND
VCC
A15
CE2
WE
A13
A8
A9
A11
OE
A10
CE1
I/O 8
I/O 7
I/O 6
I/O 5
I/O 4
I/O 1
I/O 2
I/O 3
ROM
MEM_WR
MEM_RD
RAM
D7
D6
D5
D4
D3
R1
10K
H2
Header-Male-2.54_1x2
RESET
X1
OCXO-14
Vcontrol
OUT
CLK
U2
W27C512
/CE
/OE
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
R7
10K
DRESET
C7
10uF
U1
Z80CPU-P
40ma
CPU
M1
MREQ
IORQ
RD
WR
RFSH
HALT
WAIT
INT
NMI
RESET
BUSREQ
BUSACK
CLK
R4
10K
R3
10K
R2
10K
R9
10K
U7
SN74HCT573PWR
OE#
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
LE
ICSP Header
P4
Header-Male-2.54_2x3
MISO
SCK
MOSI
U4
ATMEGA328P-PU
PC6 RESET#
PD0 RXD
PD1 TXD
PB6 XTAL1
PB7 XTAL2
AVCC
AREF
PC0 ADC0
PC1 ADC1
PC2 ADC2
PC3 ADC3
PC4 ADC4
PC5 ADC5
INT0 PD2
INT1 PD3
T0 PD4
T1 PD5
AIN0 PD6
AIN1 PD7
PCINT0 PB0
PCINT1 PB1
PCINT2 PB2
PCINT3 PB3
PCINT4 PB4
PCINT5 PB5
C4
100nF
C5
100nF
U9
GAL22V10
I/CLK
I/O/Q
CLEAR_WAIT
R5
10K
H3
Header-Male-2.54_1x2
UART Header
P2
Header-Male-2.54_1x3
TX
RX
LED1
LED-TH-5mm_R
R6
1K
C2
100nF
C1
1u
H1
C6
100nF
C3
1uF
H7
H6
H5
H4
!ROM = !A12 & !A13 & !A14 & !A15
!WAIT = !IORQ & RESET & !WR & !CLEAR_WAIT
TITLE:
Main Board
REV: 1.3
Company: MLGSoft
Sheet: 1/1
Date: 2019-09-21
Drawn By: amirgeva
EasyEDA