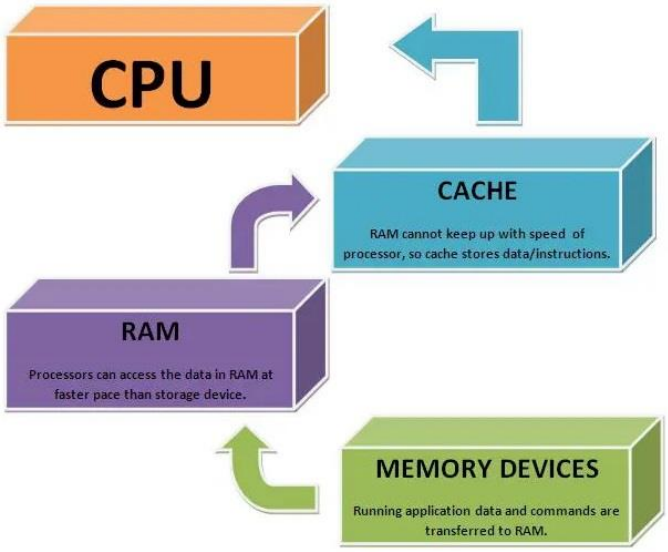
ساختار و زبان کامپیوتر

فصل هفت

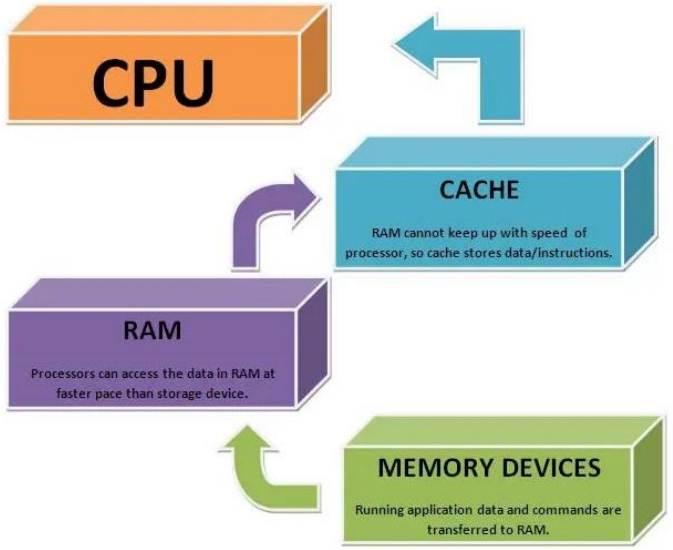
سازمان حافظه



Computer Structure & Machine Computer

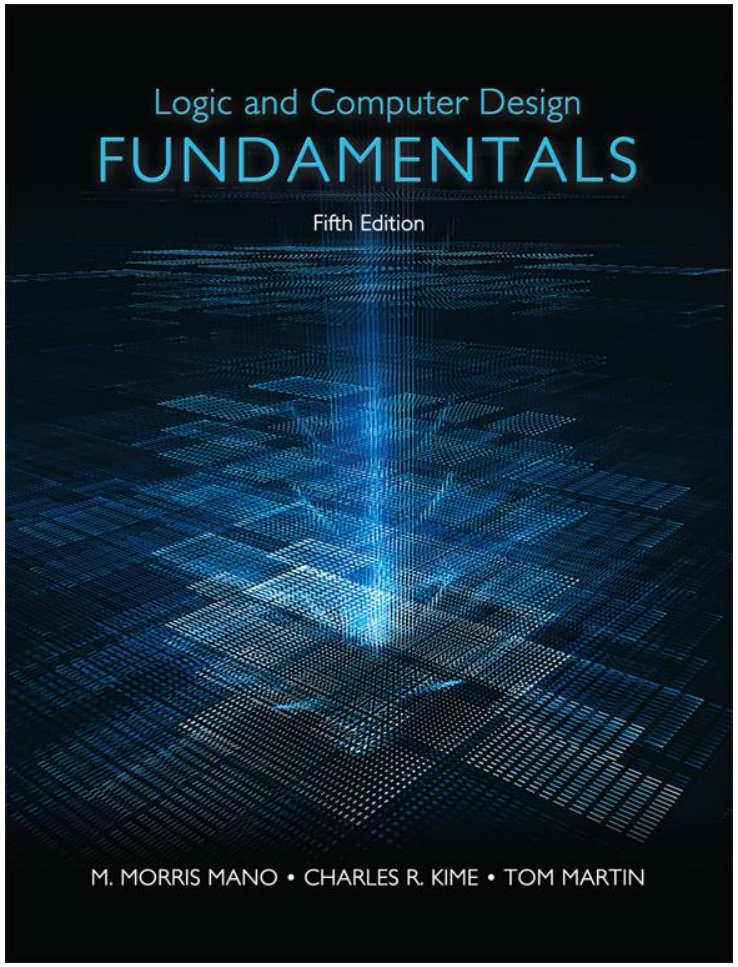
Chapter Seven

Memory Organization



Logic and Computer Design Fundamentals

Fifth Edition



Chapter 7:

Memory Basics

Contents

- Memory Definitions
- Random Access Memory
  - SRAM Integrated Circuits
  - Array of SRAM ICs
  - DRAM Integrated Circuits
- Read Only Memory

Memory

- A collection of cells capable of storing binary information
- Contains electronic circuits for storing and retrieving the information
- Used in many different parts of a computer, providing temporary or permanent storage for substantial amounts of binary information

Key Characteristics

Location
- Internal (e.g., processor registers, cache, main memory)
- External (e.g., optical disks, magnetic disks, tapes)

Capacity
- Number of words
- Number of bytes

Unit of Transfer
- Word
- Block

Access Method
- Sequential
- Direct
- Random
- Associative

Performance
- Access time
- Cycle time
- Transfer rate

Physical Type
- Semiconductor
- Magnetic
- Optical
- Magneto-optical

Physical Characteristics
- Volatile/nonvolatile
- Erasable/nonerasable

Organization
- Memory modules

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Internat vs. External Memory

- Internal
  - Semiconductor
  - Register, Cache, Main Memory

- External
  - Magnetic, Optical, Semiconductor
  - Hard disks, Optical disks, SSD

RAM vs. ROM

- Read Write Memory (RAM)
  - Misnamed as all semiconductor memory is random access
  - Read/Write
  - Volatile
  - Temporary storage
- Read Only Memory (ROM)
  - Nonvolatile
  - Permanent storage

Figure 7-2: Contents of a 1024 × 16 Memory

Memory Address		Memory Contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Contents

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Figure 7-1: Block Diagram of Memory

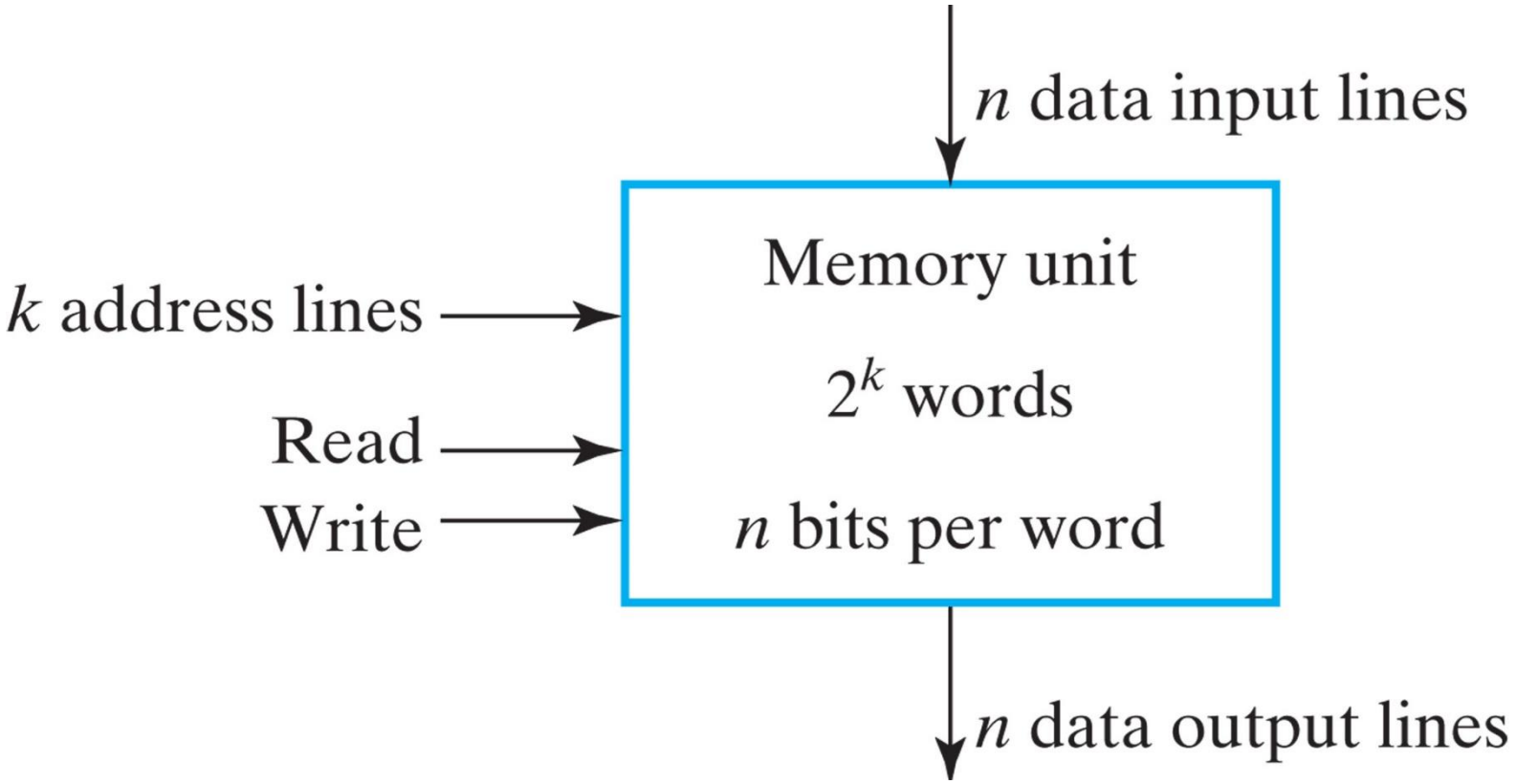

Table 7.1: Control Inputs to a Memory Chip

Chip Select CS	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	Memory Operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

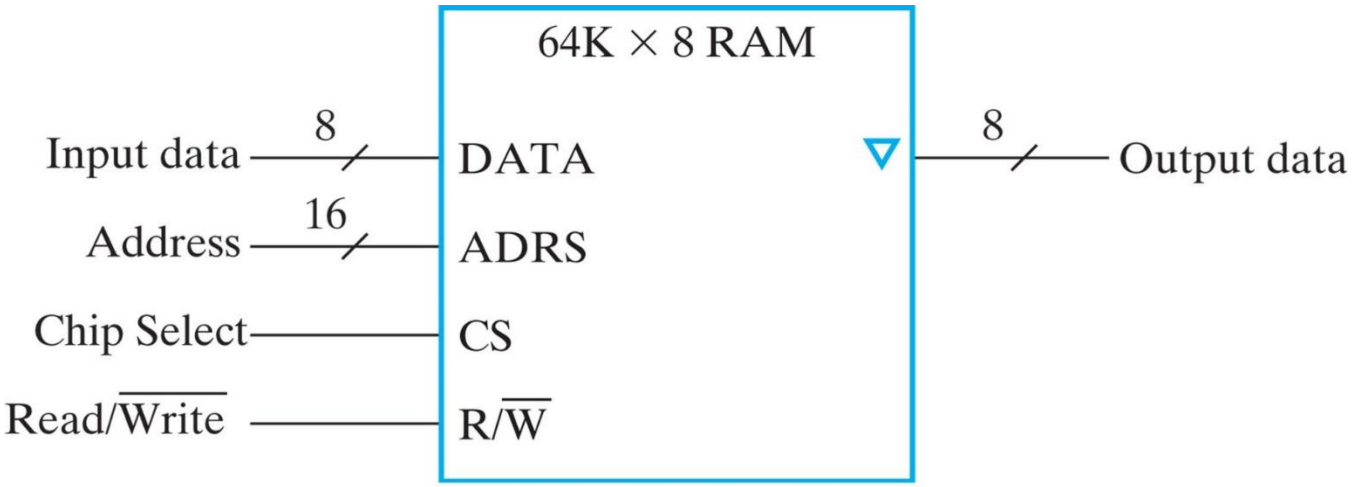

Figure 7-3: Memory Cycle Timing Waveforms

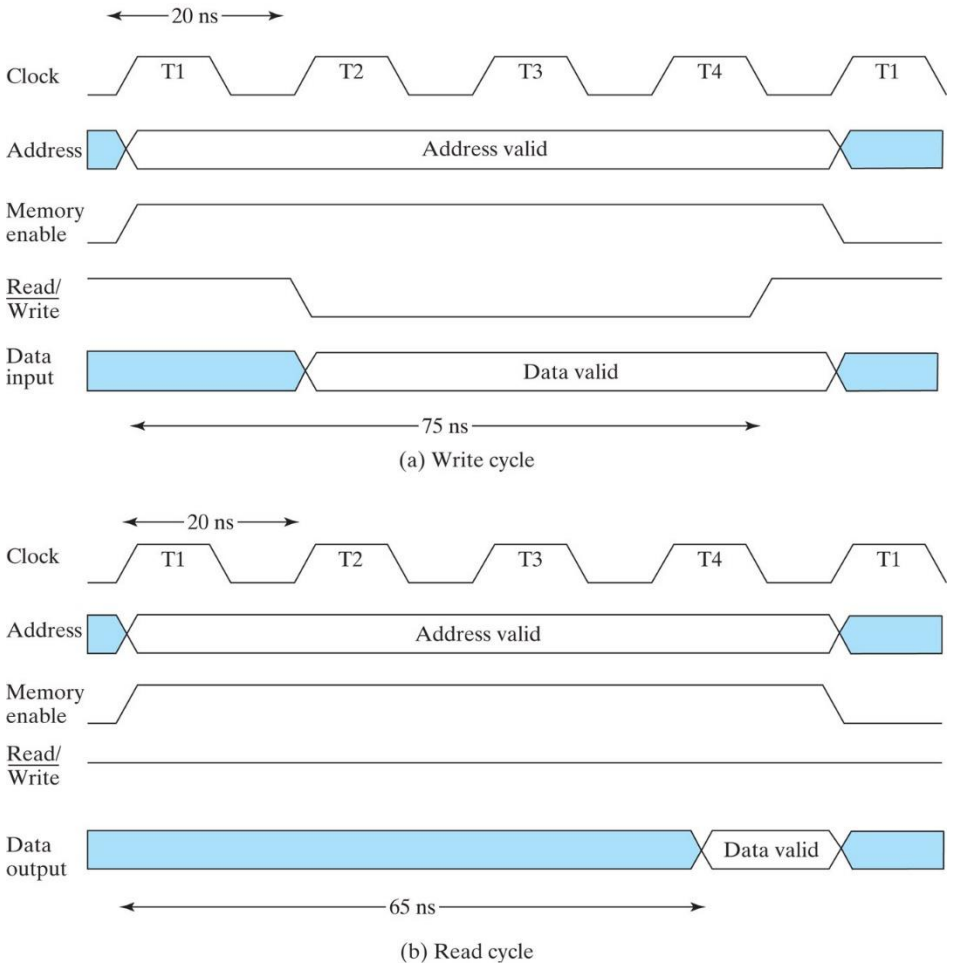

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Figure 7-4: Static RAM Cell

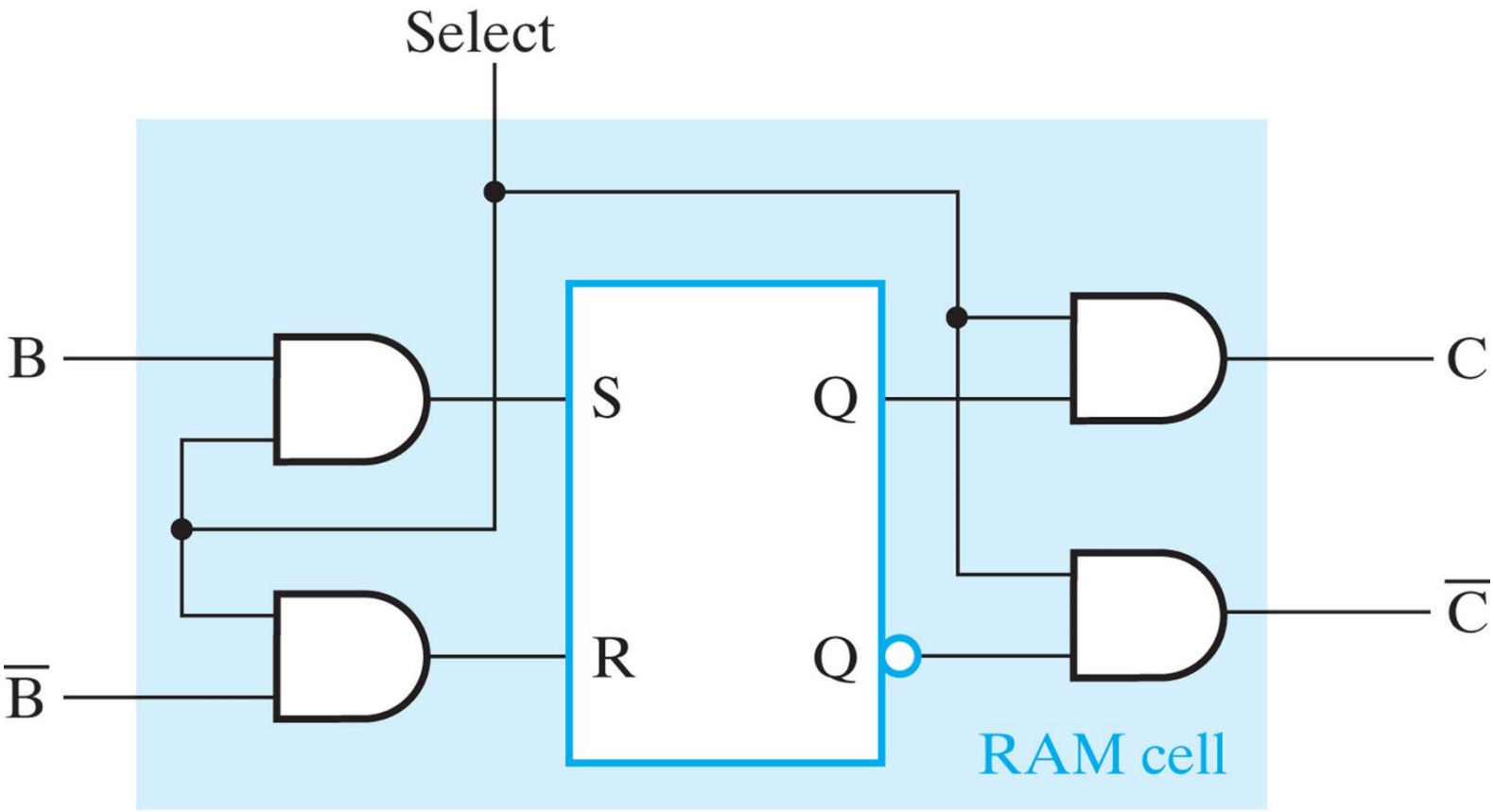


Figure 7-5: RAM Bit Slice Model

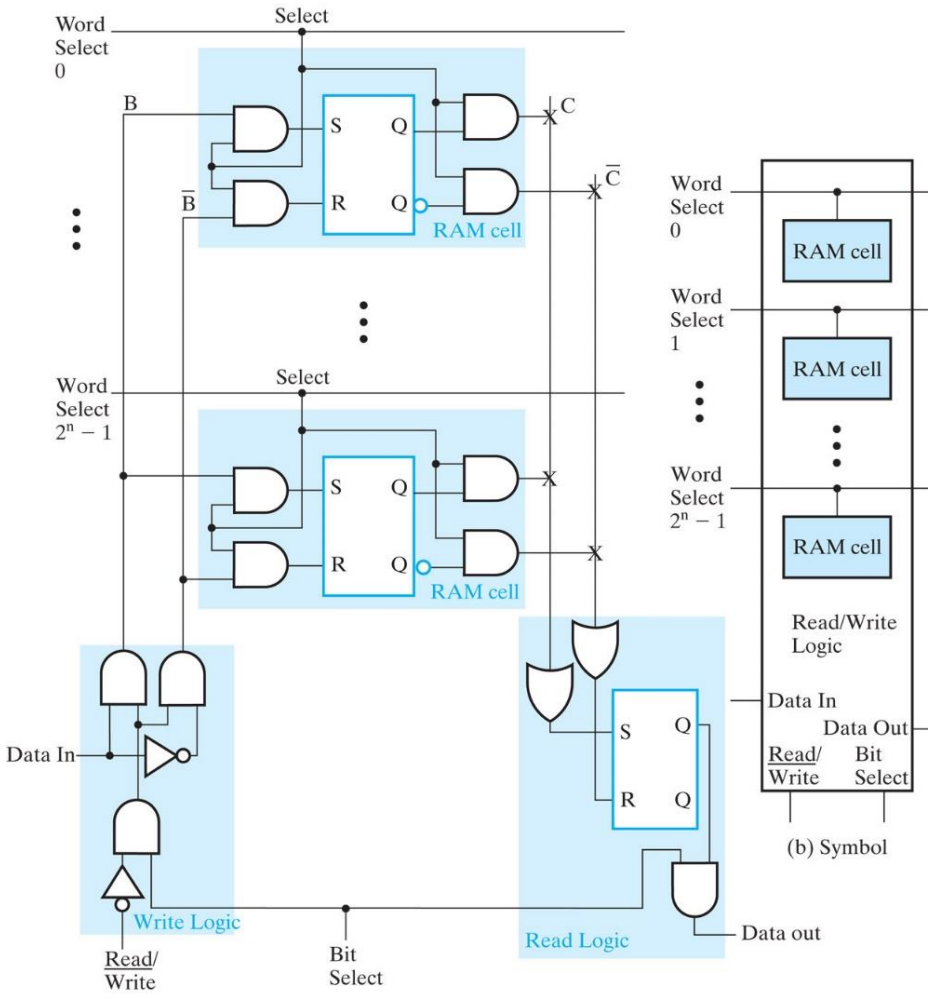


Figure 7-6: 16-Word by 1-Bit RAM Chip

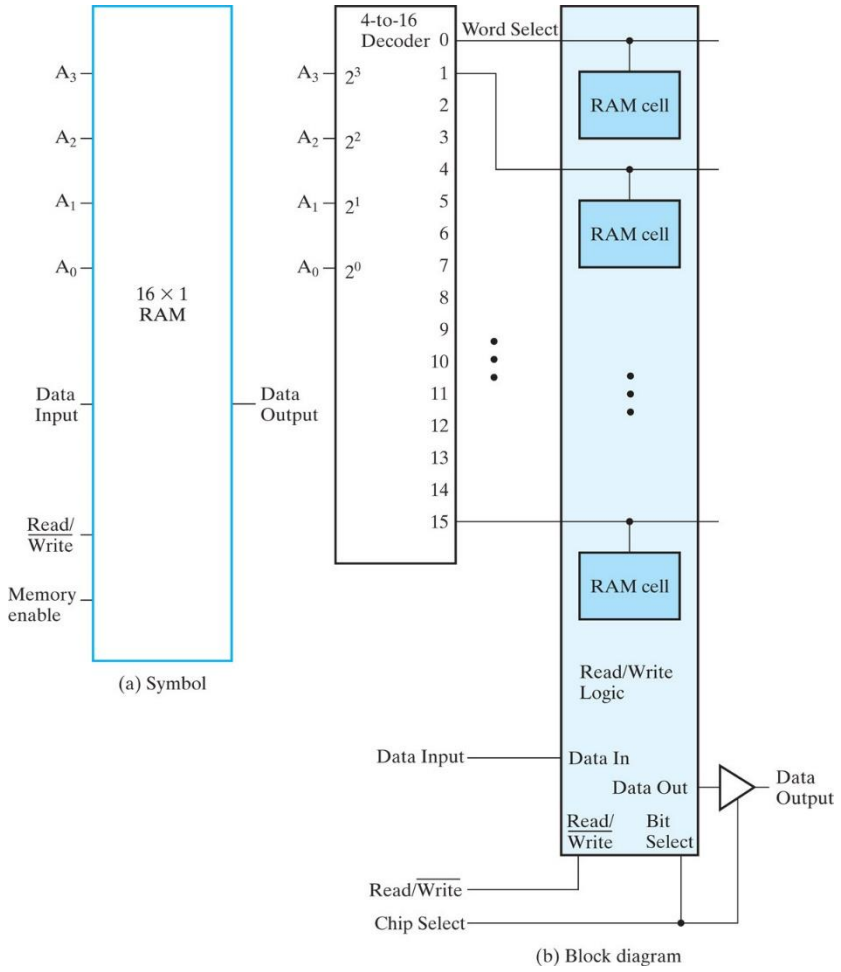


Figure 7-7: Diagram of a 16 × 1 RAM Using a 4 × 4 RAM Cell Array

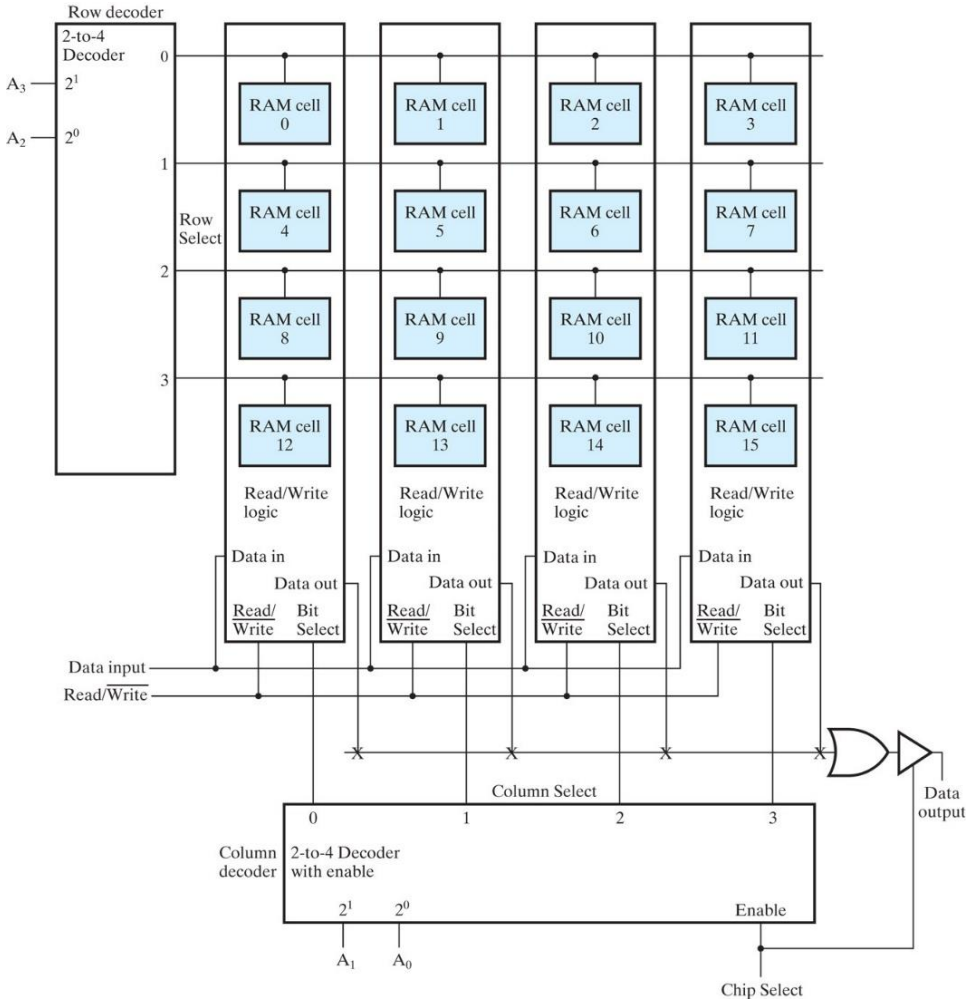
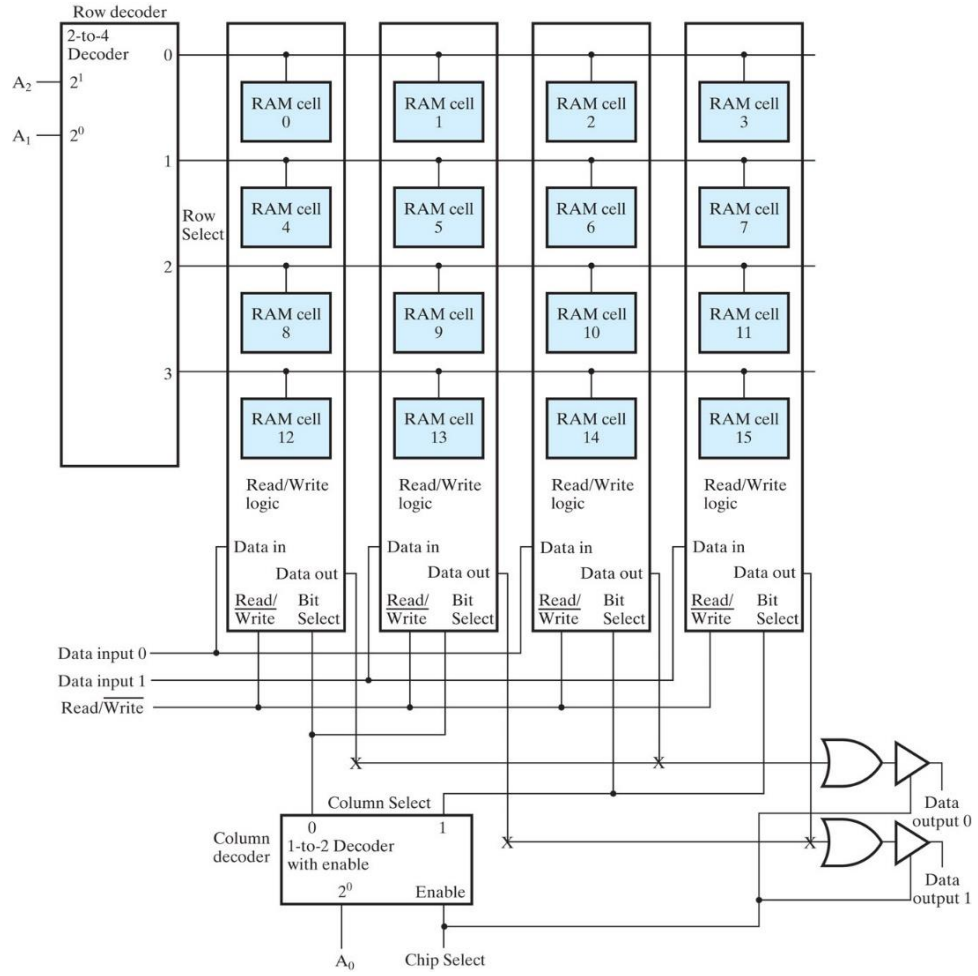


Figure 7-8: Block Diagram of an 8 × 2 RAM Using a 4 × 4 RAM Cell Array



Contents

Figure 7-9: Symbol for a 64K × 8 RAM Chip

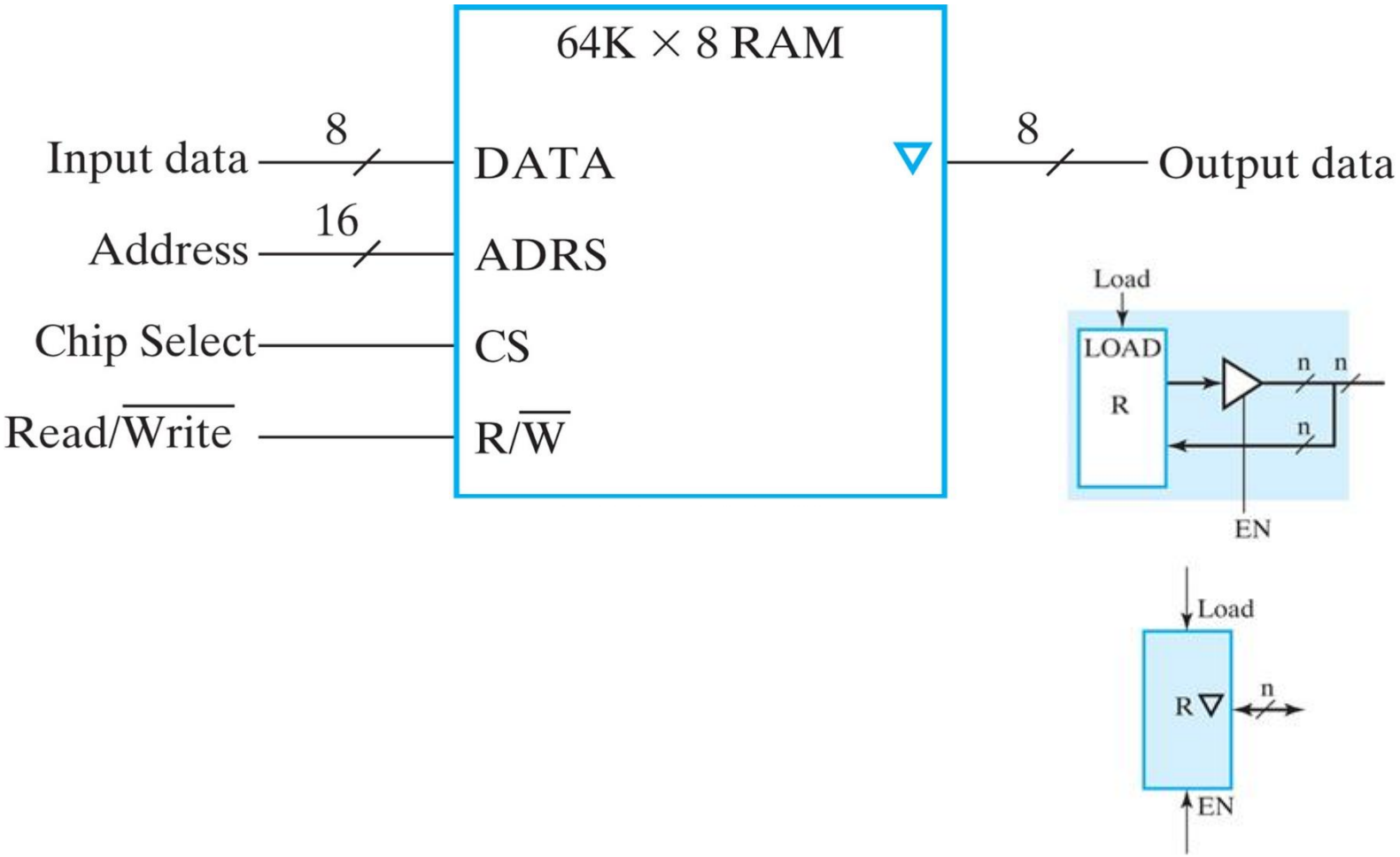


Figure 7-10: Block Diagram of a 256K × 8 RAM

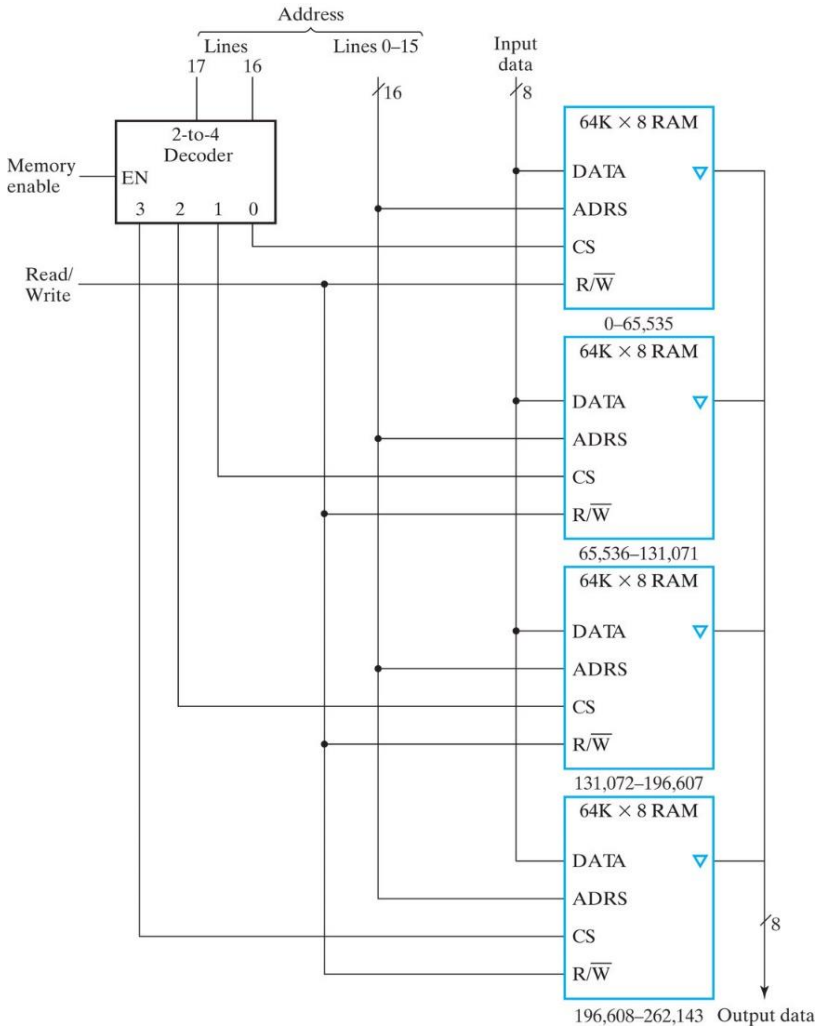


Figure 7-11: Block Diagram of a 64K × 16 RAM

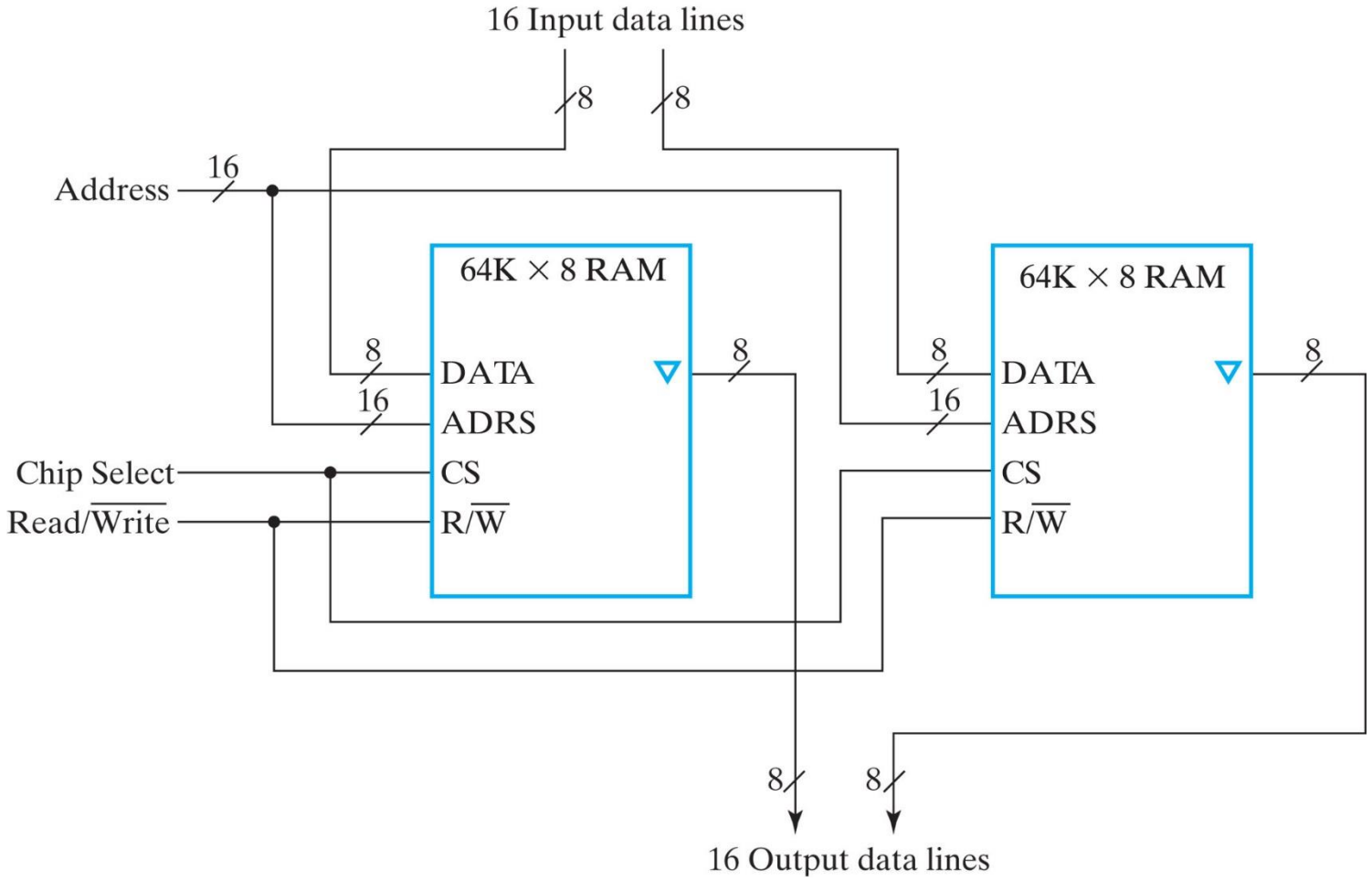


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Figure 7-12: Dynamic RAM cell, hydraulic analogy of cell operation, and cell model

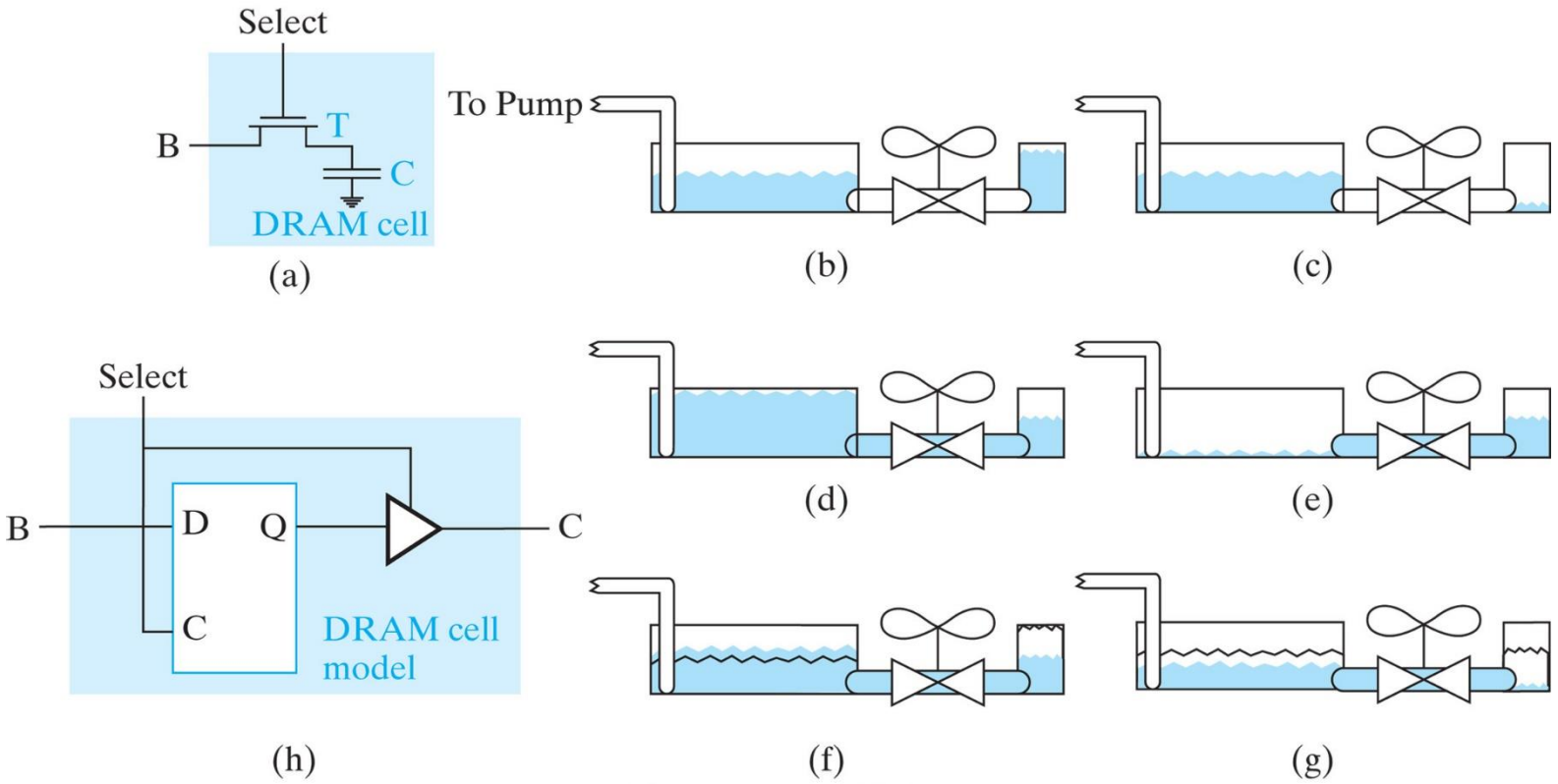


Figure 7-13: DRAM Bit-Slice Model

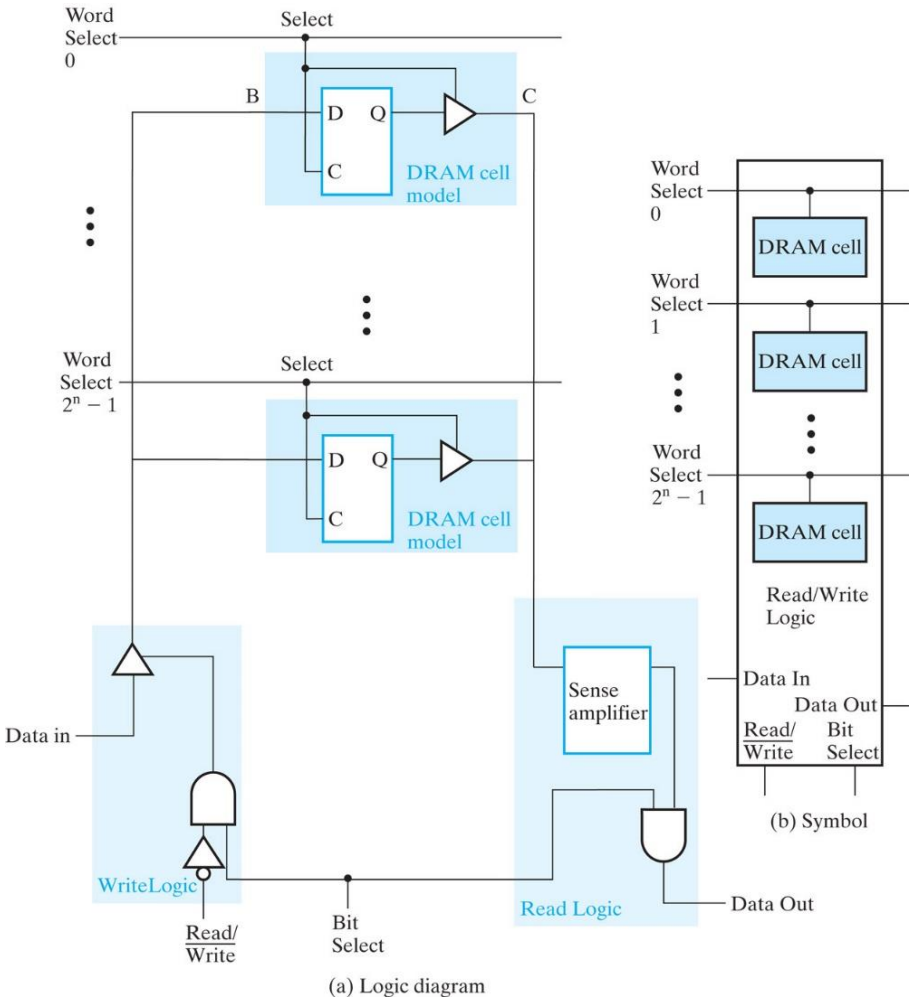


Figure 7-14: Block Diagram of a DRAM Including Refresh Logic

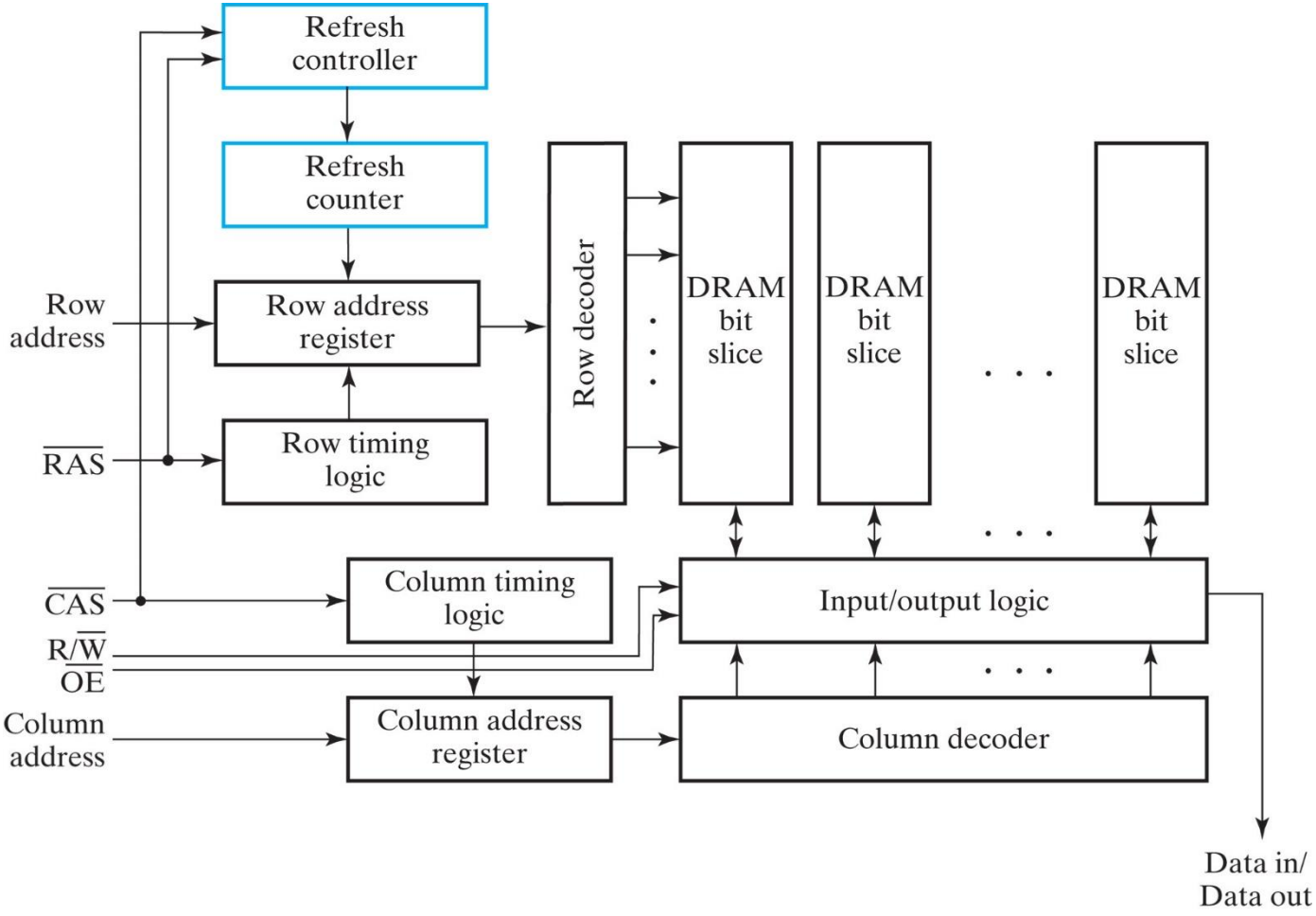
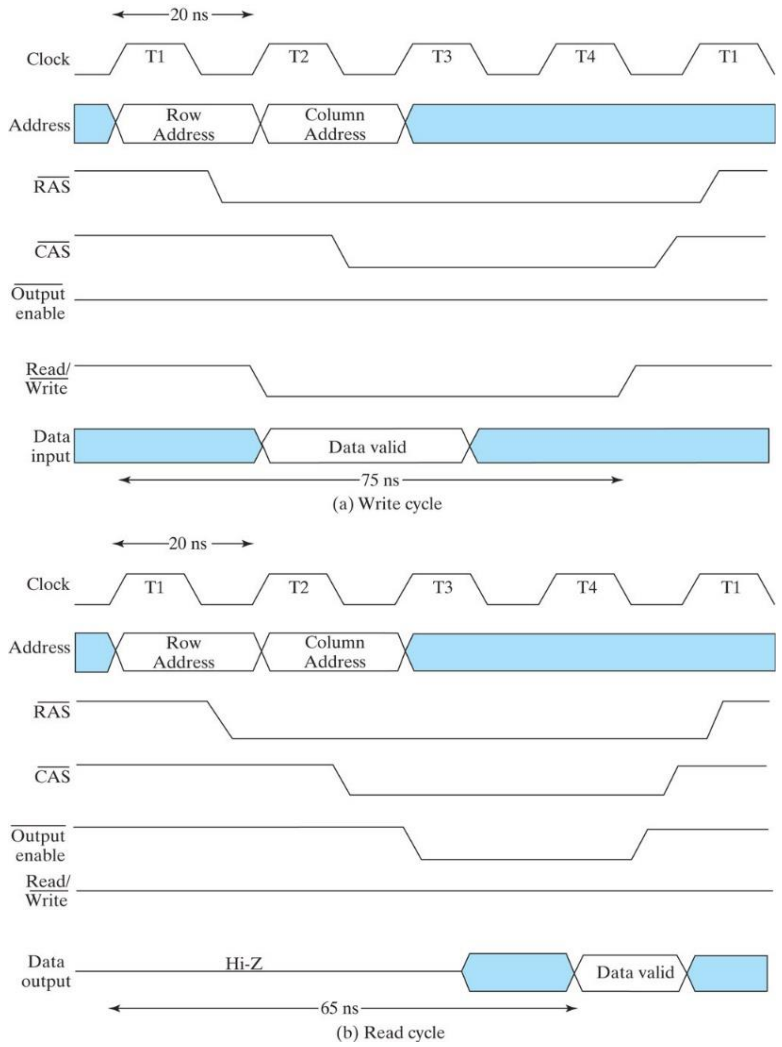
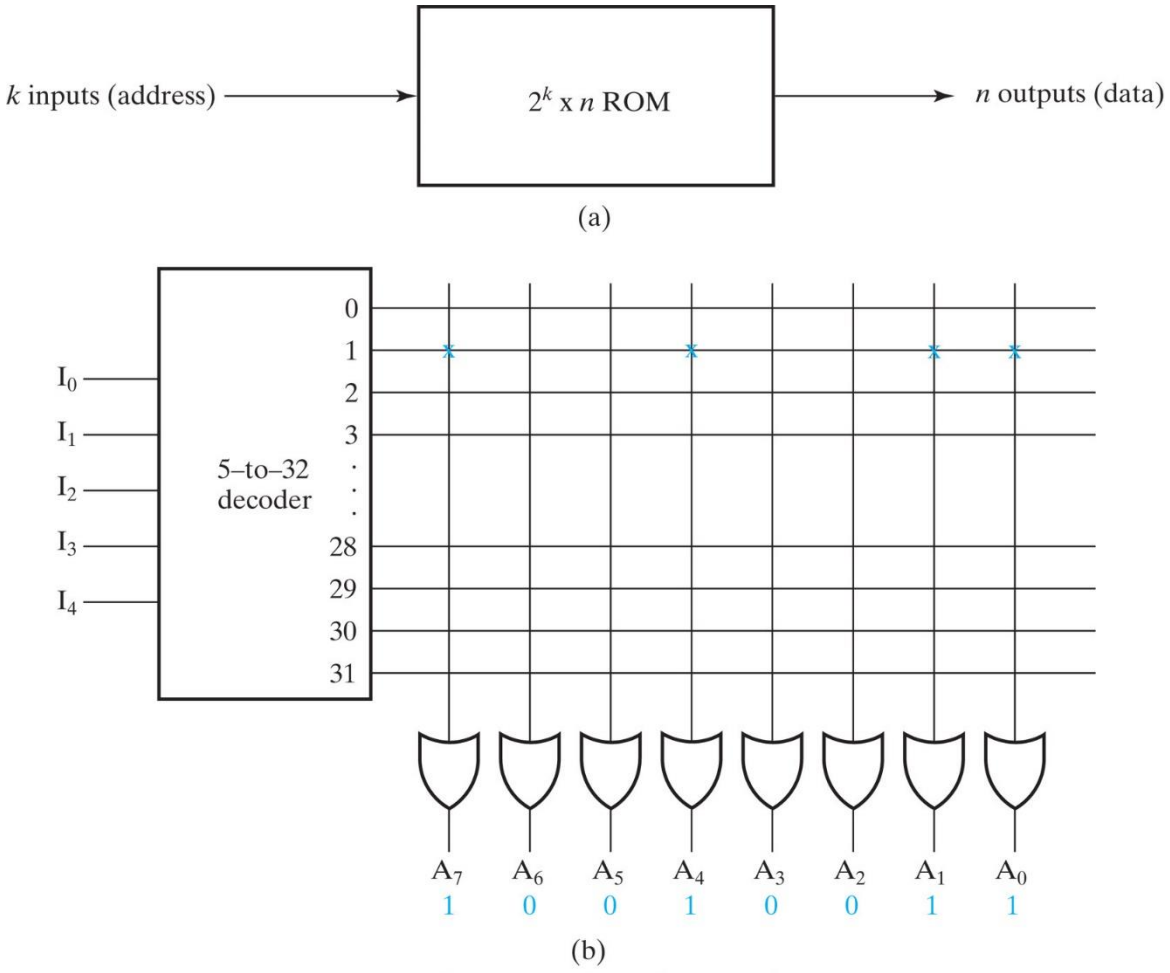


Figure 7-15: Timing for DRAM Write and Read Operations



Contents

Figure 5-7 Block Diagram and Internal Logic of a ROM



Summary: Random Access Memory Types

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

William Stallings Computer Organization and Architecture, 8th Edition, Chapter 5