DESIGN OF AN EXCELLENT GAIN FLATNESS 3-5 GHZ CMOS LOW NOISE AMPLIFIER FOR ULTRA-WIDEBAND APPLICATIONS

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A report submitted in partial fulfillment of the requirements for the degree of Bachelor of Engineering (Hons) (Electronic Engineering)

SCHOOL OF MICROELECTRONIC ENGINEERING
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First and foremost, I would like to express my utmost gratitude and praises to Allah that for His uncountable blessings, I am able to complete this work successfully. I also would like to ask Him that this project would be stepping stone in my career and also able to acts as a reference for other people.

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ABSTRAK

REKABENTUK CMOS PENGUAT RENDAH HINGAR DENGAN KONSISTENSI GANDAAN YANG CEMERLANG UNTUK APLIKASI ULTRA-JALUR LEBAR

Amir Hilmi Bin Ahmad Azizi

Penguat bunyi yang rendah (LNA) akan ditempatkan di bahagian hadapan sistem penerima wayarles. Fungsi LNA adalah untuk menyediakan frekuensi radio isyarat penguatan dengan bunyi yang seminimum mungkin. Walau bagaimanapun, konsistensi gandaan untuk LNA adalah sukar untuk dicapai. Oleh itu, keuntungan adalah tinggi LNA adalah sangat penting untuk memastikan keuntungan yang berterusan semasa memindahkan isyarat. Projek ini didedikasikan untuk mereka-bentuk 3-5 GHz CMOS LNA dengan konsistensi gandaan yang tinggi untuk aplikasi UWB. LNA tersebut direka menggunakan litar suap balik dengan komponen perintang dan kapasitor yang bertindak sebagai topologi digunakan semula semasa untuk memaksimumkan gain dan struktur induktif sumber degenerasi untuk mengekalkan gain manakala topologi common-source yang konvensional ditambah sebagai peringkat kedua untuk mengekalkan jalur lebar. The LNA direka mempunyai kehilangan pulangan input (S11) kurang daripada -8 dB, kehilangan pulangan output (S22) kurang daripada -7 dB, keterbalikan pengasingan (S12) kurang daripada 37 dB. Gain yang diperolehi adalah 26 dB dan angka itu dikekalkan sepanjang frekuensi 3-5 GHz. Angka kebisingan ialah 3.7 dB manakala penggunaan kuasa dikompromi kepada 21.6 mW. Analisis kestabilan untuk LNA yang direka menunjukkan ia stabil tanpa syarat manakala analisis kelinearan menunjukkan angkat -19 dBm pada titik mampatan P1dB. Sebagai kesimpulannya, LNA yang telah direka mempunyai gandaan sebanyak 18% lebih tinggi daripada kajian yang sedia ada.

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ABSTRACT

DESIGN OF AN EXCELLENT GAIN FLATNESS 3-5 GHZ CMOS LOW NOISE AMPLIFIER FOR ULTRA-WIDEBAND APPLICATIONS

Amir Hilmi Bin Ahmad Azizi

Low noise amplifier (LNA) is placed in the front end of a wireless receiver system. The function of LNA is to provide radio frequency signal amplification with minimal noise possible. However, the flatness gain for LNA is difficult to achieve. Therefore, high flatness gain LNA is very important to ensure constant gain during transferring the signals. This project was dedicated to design 3-5 GHz CMOS LNA with high gain flatness for UWB applications. The LNA designed employs a RC feedback circuit which acts as a current reused topology to maximize the gain and inductive source degeneration structure to maintain gain flatness while a conventional common source is added as second stage to maintain wideband bandwidth. The designed LNA has input return loss (S11) less than -8 dB, output return loss (S22) less than -7 dB, reverse isolation (S12) less than 37 dB. The gain obtained is 26 dB and the flatness is maintained throughout 3-5 GHz frequency with tolerance of ±0.5 dB. The noise figure analysed is 3.7 dB while power consumption is compromised to 21.6 mW. The Stern stability analysis show that designed LNA is unconditionally stable while the linearity analysis shows input 1dB compression point of -15 dBM. The input third order intercept point (IIP3) is 15 dBm and phase linearity property (group delay) obtained across whole band is of ±75. The layout chip design has the size of 0.72 mm by 0.74 mm. As a conclusion, two stage LNA with cascode common source with current reused and CS as second stage is good choice to realized wideband LNA design. A comparison between present results and previous reported LNA shows that current LNA design has 18% higher gain thus make it suitable for certain UWB applications.

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a	Radius
b	Beta

LIST OF ABBREVIATIONS

LNA	Spontaneous Brillouin Scattering
UWB	
NF	
GHZ	
VSWR	

Chapter 1
Introduction

1.1 Aims and motivation

Thesis work is a partial requirement of Bachelor of Engineering in Electronic at School of Microelectronic Engineering, Universiti Malaysia Perlis. In this thesis work, low noise amplifier (LNA) will be designed which will operates in 3-5 GHz frequency to be used for ultra wideband (UWB) applications. LNA specifications will be optimized and comparable with existing products. As UWB applications is emerging into big market in the future, this LNA can be used inside a device's receiver.

1.2 Overview of UWB

Recently, there is growth in demand for ultra- wideband (UWB) which is a wireless technology useful in delivering high digital data rate over wide spectrum of frequency bands [1]. The advantages offered by UWB are abilities to operate in distance of 230 feet at very low power and it's robustness in obstructed environments. The frequency set in America by Federal Communications Commission (FCC) for UWB techniques is from 3.1GHz to 10.6GHz [2]. UWB's spectrum can work in unison with other licensed spectrum users thus make it as an ideal choice in a wide range of applications mainly in medical and military fields.

In this project, a CMOS LNA with high gain flatness for UWB applications is designed and simulated by using CMOS 0.13-um process. It is based on a cascade feedback topology which has several advantages such as a higher gain and a wider bandwidth.

1.3 Problem statement

The Low Noise Amplifier (LNA) is a core block of an Ultra Wide Band (UWB) receiver since it amplifies a very weak signal received at the antenna to acceptable levels while introducing less self-generated noise and distortions. However, the LNA design poses a unique challenge as it requires simultaneous optimization of various performance parameters like power gain, input matching, noise figure, power consumption and linearity over the entire UWB band. Furthermore, the flatness gain for LNA is quite difficult to achieve in ultra wideband range. Therefore, high flatness gain LNA is very important to ensure a constant gain during transferring the signals.

1.4 Objectives

The main aim for this project is to design a low noise amplifier, which required to have a low noise figure with good input matching and excellent gain flatness in the wide frequency range of operation from 3- 5 GHz. The CMOS LNA will be designed and simulated by using CMOS 0.13-um process. The objectives of the task undertaken are:

- To propose 3-5 GHz CMOS LNA for UWB applications.
- To design and simulate the proposed LNA using EDA tools.
- To analyse the LNA performance and compare it with previous LNA works.
- To design the layout for LNA's chip size estimation

1.5 Scope

The project is based on circuit design which is the proposed LNA will be designed and simulated using electronic design automation (EDA) tool. The simulation results will be analysed and optimize d by comparing with previously published works of UWB LNA. The layout of LNA is designed for chip size estimation. The DRC and LVS of the circuit will not be performing in the project due to the time limitation.

1.6 Organization of the thesis

This thesis demonstrate the procedure to create LNA that operated in UWB frequency that have high gain flatness and other optimized RF parameters. There are five chapters covered in the thesis. The thesis is organized as follows.

Chapter 1 covers the introduction of UWB which focuses on the UWB frequency of operation and it's competitive advantages compared to other wireless technology. This chapter also presents, problem statement, objectives of the studies, project scope and finally thesis organization.

Chapter 2 presents the literature reviews that explain UWB technology and LNA operations in details. The UWB operation is described by the its nature of operation and frequency spectrum involved, as well as its potential application in industrial and medical field. Further, the LNA's working principle as a part of component of a receiver's system is explained clearly. It also review on different LNA circuit topologies and their advantages and disadvantages are tabulated. Besides that, this chapter also reviews on numerous LNA performance criteria such that input and output impedance matching, noise figure, s-parameters, voltage standing wave ratio (VSWR) and stability.

Chapter 3 provides design processes and analysis required in LNA design. The project flowchart of LNA design is described in graphic. The proposed circuit schematic is shown and the function of each of the components in the circuit is elaborated. Further, the components' type and their sizing are determined by taking into account the requirements of gain, noise and linearity.

Chapter 4 provides results and discussion and presents the simulated analysis of the design by providing analysis and discussion for the finding. The first section covers the electrical characterization of s-parameters. Then, next results covered are noise analysis, stability analysis, linearity analysis group delay analysis. Besides, IC layout is shown which every components and interconnections are drawn precisely. The layout chip size is briefted. Finally, current LNA results are summarized and compared with previous works.

Chapter 5 summarizes the conclusions made in the present study and recommendations for future research in this particular area. The conclusions are written based on the findings reported in Chapter 4. Recommendations for future studies are presented due to their significance with the current research.

Chapter 2
Literature review

2.1 Introduction

To have a better understanding and supporting of the thesis work, a theoretical background literature is included in this part. Relevant theories are described briefly.

2.2 Ultra wideband operation

Ultra wideband can be explained by describing it's frequency of operation and applications that can operate within the UWB specifications.

2.2.1 Ultra wideband frequency of operation

UWB short-range wireless communication offered different characteristics compared to a traditional carrier wave system. UWB waveforms are short time duration and have some rather unique properties. In spreading signals over very wide bandwidths, the UWB concept is particularly appealing since it facilitates optimal sharing of a given bandwidth between distinctive systems and applications. Recent years, advanced developments have been experimented on using UWB signals as communication technologies.

From Figure 2.1, it can be observed that UWB occupies a very wide bandwidth and operate in the range 3 GHz up to 10 GHz and the transmission needs to occupy bandwidth of at least 500MHz. This aspect enables it to carry data rates of gigabits per second. For this reason, UWB supports a bit rate greater than 100 Mbps within a 10-meter radius for wireless personal area communications.

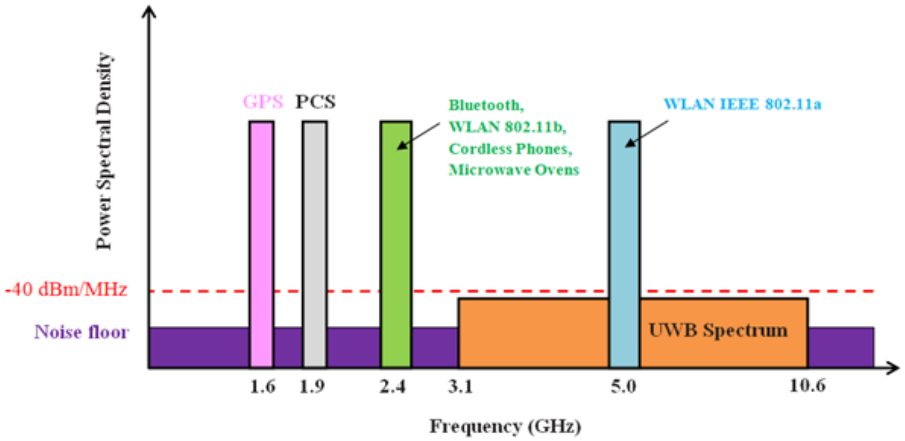

Figure 2.1: Spectrum allocated for UWB transmission

The wide bandwidth that UWB operating means that they will cross the boundaries of existing licensed carrier based transmission such as WLAN. However, UWB's power spectral density is very low at -40 dBm/ MHz. For this reason, UWB will not causing any noticeable interference to other carrier based licensed users.

2.2.2 Ultra wideband application

Since UWB signal has low power spectral density (PSD), it enables UWB devices to operate in same spectrum with other wireless technology without interfering other operations. This communication feature is useful in low data rate communication. UWB allows the operation of multiples devices wihout interferences at the same time in the same space. For example, computer devices such as monitor, mouse, keyboard and printer can operate at the same time without interferences using UWB technology.

In healthcare industry, UWB technology can benefited in such a way that patients can be monitored intensively. A network of UWB sensors such as electrocardiogram (ECG), oxygen saturation sensor (SpO2) and electromyography (EMG) can be used to develop a proactive and a smart healthcare system. This can benefit the patient in chronic condition and provides long term health monitoring. In UWB system, the transmitter is often kept simpler and most of the complexity is shifted towards receiver, which permits extremely low energy consumption and thus extends battery life.

2.3 Overview of CMOS low noise amplifier

Low noise amplifier (LNA) is conventionally used in all wireless applications. Based on Figure 1.1, LNA is placed in receiver most front ends in- between Band Selection Filter and Image Rejection filter. The function of LNA is to provide signal amplifying without giving much noise, as the name suggested. However, the flatness gain for LNA is quite difficult to achieve in ultra wideband range. Therefore, high flatness gain LNA is very important to ensure constant gain during transferring the signals.

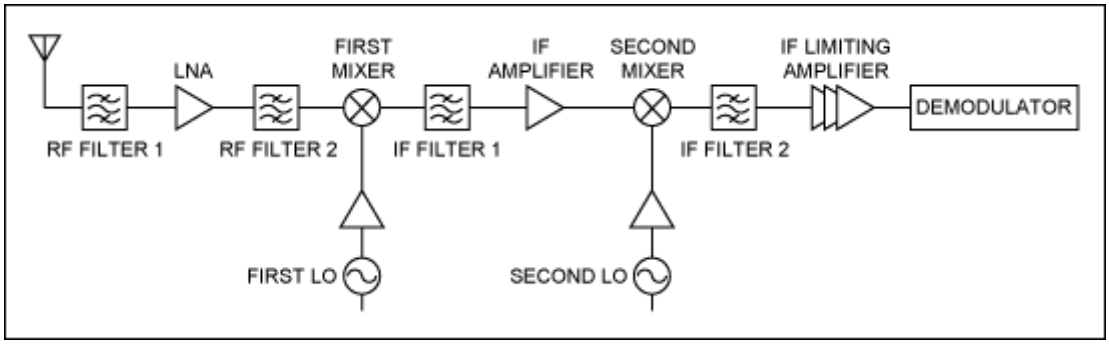

Figure 2.2: Location of LNA in a receiver system

2.4 Comparisons of LNA topologies

In order to design an LNA that has high gain with excellent flatness over wideband frequency, the circuit's topology that will be used must be thoroughly understood. The topology should be selected such that it consumes less power, provides higher gain and contains lesser number of components to avoid degradation in noise figure. The most common used LNA topologies are common-source, common-gate and cascode.

The common-source transistor is used to in obtaining good noise figure but has disadvantage due to high sensitivity to temperature and component tolerance. In addition, common source topology with shunt series feedback, power consumption is low but stabilizing among noise figure, gain and input output matching is a challenging task. Common source configuration with resistor termination adds extra noise to LNA due to the thermal noise of resistor . Lastly, common source topology with inductive degeneration with low power consumption and better stability is best choice for UWB applications [9]. The circuit topology for common-source LNA is shown in Figure 2.2.

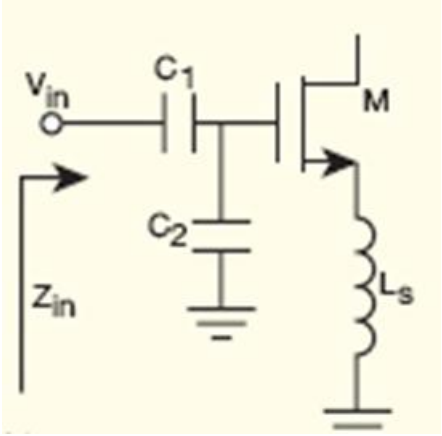

Figure 2.3: Common-source LNA

In common gate configuration, the LNA consumes very -low power but provide minor gain of less than 10dB. It also has a low noise figure at lower frequencies, but the noise figure rise exponentially with increasing signal frequency. The high drain-source capacitance in common-gate implementations requires inductive feedback, which serves to improve noise figure, gain, and stability at higher frequencies. The circuit topology for common-gate LNA is shown in Figure 2.3.

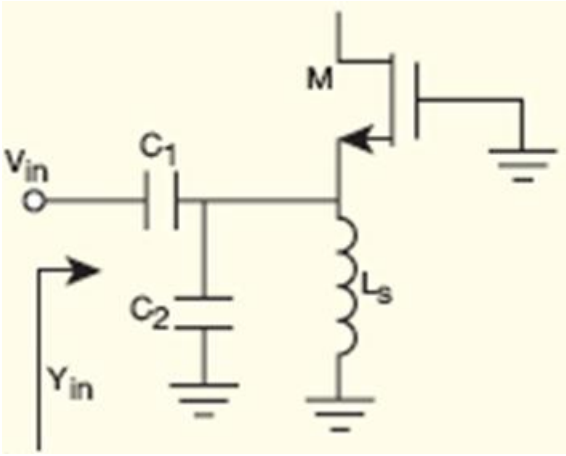

Figure 2.4: Common-gate LNA

Lastly, the cascode amplifier combines both common-source stage and common-gate transistor. As a result, cascode amplifier provides flat gain over wide frequency. The advantages of cascode LNA are improved linearity, stability and bandwidth with only minimal degradation of noise figure performance.

In order to achieve wideband amplification, the feedback configuration is preferred in IC fabrication due to the uniformity and stability at frequencies below 12GHz. The cascade configuration offered various advantages for wideband applications such as higher gain, wider bandwidth, and better stability. Most importantly, by carefully choosing feedback resistance, the requirements of wideband systems for both noise and power simultaneously satisfied. The cascode configuration is also able to reduce high frequency roll- off of the input devices due to Miller effect. The input and output matchings are able to performed independently. The stability and

circuit's bandwidth is improved by using negative parallel feedback. A single- stage CMOS cascode feedback LNA consists of a cascaded n- channel MOS and a resistive parallel feedback as illustrated in Figure 2.4.

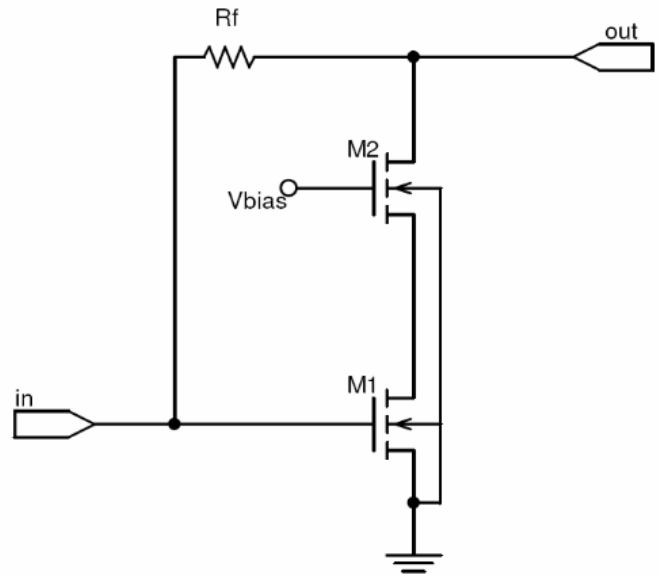

Figure 2.5: Common-gate LNA

Comparison of the topologies is summarized and shown in Table 2.1.

Table 2.1 Comparison of different LNA circuit topologies

Characteristic	Common-Source	Common-Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Highest
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Highest
Bandwidth	Narrow	Fairly broad	Broad
Stability	Moderate	High	High
Reverse Isolation	Low	High	High
Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance.	Good	Less	Less

2.5 Input and output impedance matching

Impedance matching is one of the important steps to design LNA as it is required for the reason that to provide maximum power transfer between the source and its load. By impedance matching, load impedance is made equal to the source impedance by minimizing the reflections and acquire an satisfactory noise level and optimum gain. Input matching network is tuned for the purpose optimal value of input reflection coefficient, gain and noise figure (NF). Likewise, to get optimal output reflection coefficient, output matching network is configured. Figure 2.4 shows a general transistor circuit with input and output matching network.

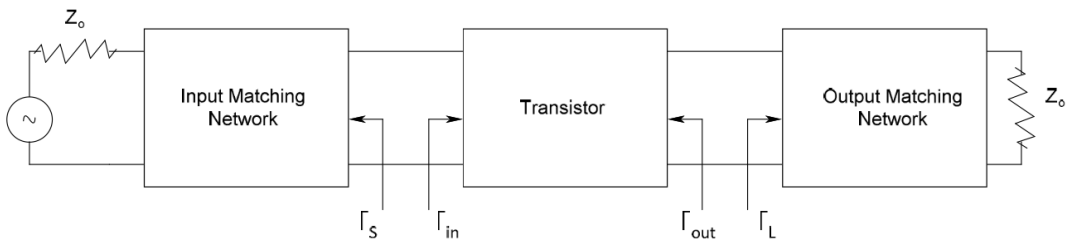

Figure 2.6: Input and output matching netwok of a transistor

In general, the input match is a compromise between noise figure, gain, and input return loss. The amplifier is not possible to obtain both maximum gain and low noise figure. The condition for impedance matching is that real part of the impedances should be equal to the real part of the load and reactance's should be equal and opposite in character. For example, to achieve matching for source impedance R + jX, load matching should be adjusted R – jX.

2.6 Noise figure

A parameter called noise figure (NF) is a commonly used method of specifying the additive noise inherent in a circuit or system. The parameter is used only in the situation which the sources impedance is resistive. However, it is often the case in a front end, and so this method of specifying noise is adopted here.

The noise figure is defined as how much the internal noise of an electronic element degrades its SNR (signal noise ratio). It is often specified for a 1Hz bandwidth at a given frequency. In this case, the noise figure is also called spot noise figure to emphasize the very small bandwidth as opposed to the average noise figure, where the band of interest is taken into account. The noise figure is defined as:

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}N_{out}}{S_{out}N_{in}} \tag{2.1}$$

Where,

N_{in} : input power and always taken as the noise in the source resistance.

N_{out} : output noise power including the circuit contribution and noise transmit from the source resistance.

Combine S_{out}= GS in into equation above, where G is power gain of corresponding stage,

$$NF = \frac{N_{out}}{GN_{in}} \tag{2.2}$$

2.7 S-Parameters

S-parameters are used extensively to characterize electrical networks using reference impedances. The concept of S-parameters characterizations can be explained using two-port networks. Two-port S-parameters are defined by considering a set of voltage traveling waves. When a voltage wave from a source is incident on a network, a portion of the voltage wave is transmitted through the network, and a portion is reflected back toward the source. Incident and reflected voltage waves may also be present at the output of the network. Figure 2.6 shows the 2 port network configuration

From S-parameters analysis, the stability condition and maximum gain of LNA can be obtained.

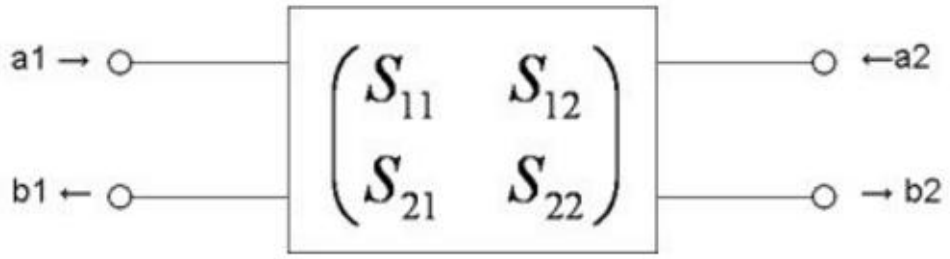

Figure 2.7: S-parametes port topology

The relation of an and bn can be understood as equation below:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.3}$$

Where $\boldsymbol{a_n}$ represents the power wave travelling towards the two-port network and $\boldsymbol{b_n}$ is the power wave reflected back. The power variables and network S-parameters are related by the expressions:

$$S_{11} = b_1/a_1,\ a_2 = 0$$
$$S_{12} = b_1/a_2,\ a_1 = 0$$
$$S_{21} = b_2/a_1,\ a_2 = 0$$
$$S_{22} = b_2/a_2,\ a_1 = 0 \qquad (2.4)$$

The S-parameters that are analysed from the LNA are :

1) S_{11}(dB) , input reflection gain
2) S_{22} (dB), output reflection gain
3) S_{21}(dB), forward gain
4) S_{12}(dB), reverse gain

To begin the S-parameter analysis, there are variables that needed to be provided by designer. One of the step is the characteristic step must be given value, which is usually 50 Ω. Port numbers must be allocated and other condition that can influence the IC such as temperature, bias current and control voltage values need to be entered.

2.8 Refelection coefficient

The reflection coefficient is used to analyses the amount of electromagnetic wave is reflected by an impedance discontinuity in the transmission medium. It is used when wave propagates in a medium containing discontinuities. The reflection coefficient, Γ can be summarised in Equation

$$\Gamma=\frac{Z_L-Z_S}{Z_L+Z_S} \tag{2.5}$$

Where ZL is the impedance towards the load and ZS is the impedance towards the source.

2.9 Voltage standing wave ratio

The parameter Voltage Standing Wave Ratio (VSWR) is a function of the reflection coefficient, which describes the power reflected from antenna. In other word, VSWR is used to measure how well is the antenna's impedance matched to the transmission it is connected to. The VSWR is defined by the following formula:

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2.6}$$

Where reflection coefficient is given by Γ.

2.10 Stability analysis

Stability in an LNA refers to an amplifier's immunity to causing spurious oscillations. Using Stern stability factor, circuit stability is characterizes as below equation:

$$K_f = \frac{1+ |\beta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (2.7)$$

Where

$$\beta = S_{11}S_{22} - S_{21}S_{12} \quad (2.8)$$

If $K_f > 1$, the circuit is said to be unconditionally stable

Chapter 3
Methodology

3.1 Introduction

Designing an LNA with outstanding specifications required thoroughly understanding of IC design flow and advanced planning in order to reduce time taken to complete this project. In this chapter, general usage of Cadence Virtuoso as selected EDA tool will be explained. Flowchart diagram to design the schematic and layout of LNA is illustrated for easy understanding. Finally, the complete circuit schematic is drawn and each of component's parameter is listed.

3.2 Utilizing of Cadence Virtuoso

Cadence is an Electronic Design Automation (EDA) environment which allows different applications and tools to integrate into a single framework. Cadence support all the stages of IC design and verification from a single environment. In addition, These tools support different fabrication technologies. Virtuoso platform which can be used in Cadence environment, is a schematic editor tool for designing full- custom integrated circuit. Virtuoso Analog Design Environment is an industry standard platform that supports a variety of analog simulators, and has the flexibility to use different simulators on the same design. The analog IC components used in the schematic editor is compatible with Silterra foundry.

Firstly a schematic view of the circuit is created using the Virtuoso Schematic Editor. Virtuoso Schematic Editor is capable of supporting digital, analog and RF integrated circuit designs within the same environment. Alternatively, a text netlist input can be employed. Then, the circuit is simulated using the Cadence Affirma analog simulation environment. Different simulators can be employed such as Spectre RF and HSPICE which provide distinctive IC simulation environment.

3.3 Schematic design flow

The project is started by identifying the low noise amplifier specifications. The vital characteristics of the amplifier are the noise figure (NF) and the gain at source impedance. The trade-offs of the optimizations is the scarification of other important characteristics such as gain, power consumption, gain flatness and input and output loss. These specifications are defined early in the project as expected results of the amplifier.

The next step of the project is designing the circuit topology. In this step, network interconnections of the circuit components will be produced. Distributed and feedback configurations are the most commonly used as it has better uniformity and stability at frequencies below 12GHz. In addition, the cascode structure is considered to be the best topology for wideband applications because of advantages such as higher gain, wider bandwidth, and better stability. Above all, it can satisfy the requirements of wideband systems for both noise and power simultaneously through a careful choice of feedback resistance [6].

The electronic design automation tool (EDA) will be used in the process of designing the amplifier's circuit schematics. The EDA tool chose for this project is Cadence. The tool provided the users with the IC electronic components such as transistors and resistors to be placed on circuit. The technology of IC is set to 0.13-um. The obtained simulated result will be analysed and compared with desired specification before proceeding to last process. Layout design will be done only for estimating the LNA chips size. The complete process flow of this project is shown in Figure 3.2.

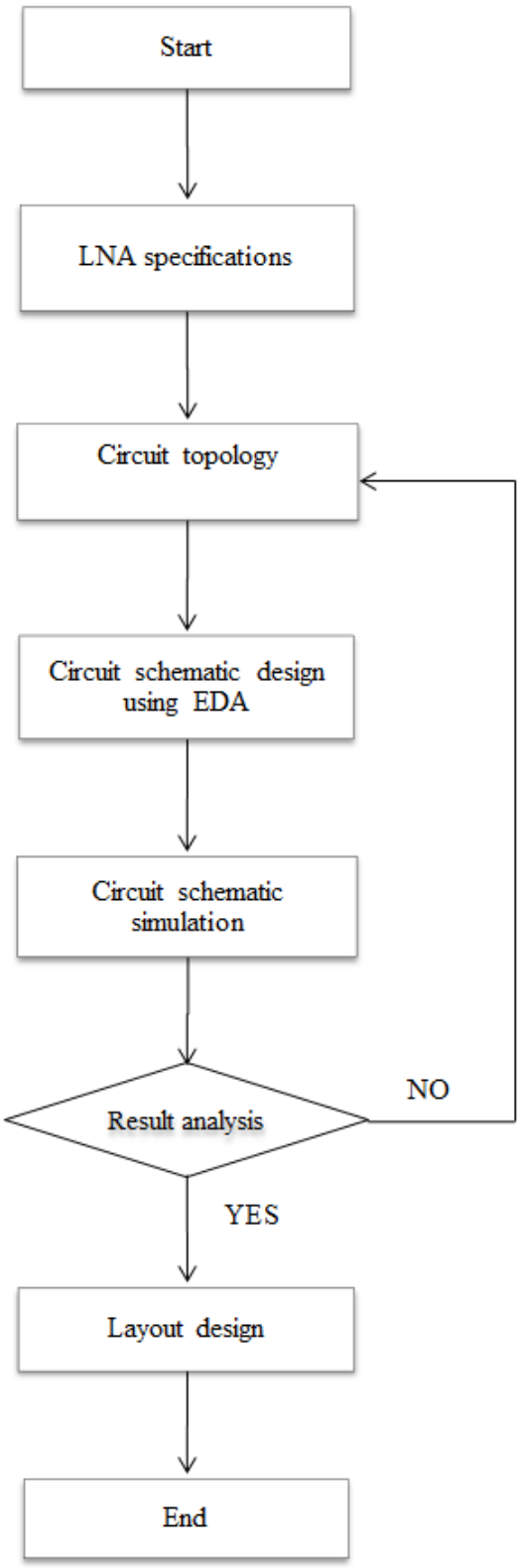

Figure 3.1: Flowchart of LNA design process

3.4 Block Diagram of LNA

In wireless design, low- noise amplifier (LNA) is a critical interface between the antenna and the electronic circuits. Positioned at the front end of the receiver channel, LNA amplifies very weak signals so that the output signal has reduced of unwanted background noise. After the extraction and amplification, the signal is now capable of being processed by the blocks that located further down the receiver chain. Some aspects that must be take into account while designing amplifier and measure performance amplification process are power dissipation, supply voltage, linearity and noise. In addition, input and output impedance also play some role to determine how the circuit interact leading and lagging stages. Figure 2.2 shows block diagram of a functional LNA.

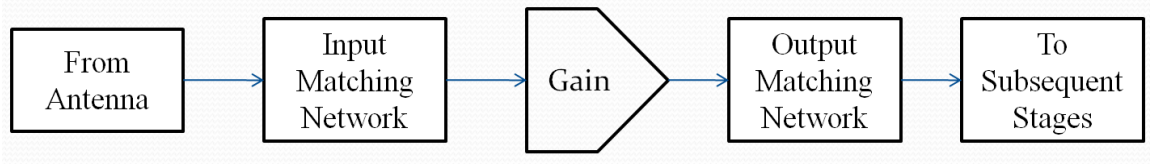

Figure 3.2: Block diagram of functional LNA

3.5 Circuit Schematic

The best LNA circuit topology for operating under UWB frequency is chosen after detailed study on different topology advantage. The selected circuit has two stages of amplification which utilized cascade and common source topology. Using Microsoft Visio, the schematic is drawn as Figure 3.3.

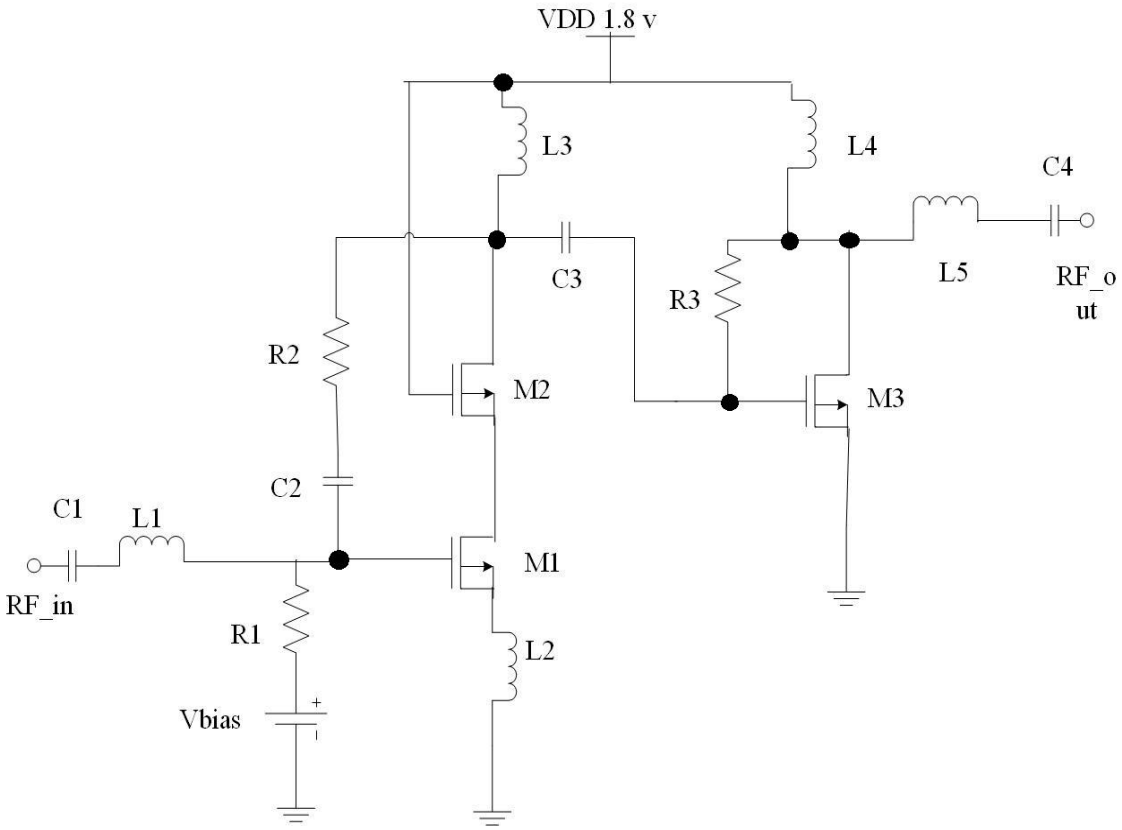

Figure 3.3: Proposed LNA circuit schematic

Based on the schematic drawn, the proposed design has two stages of amplifications to achieve good signal boost in ultra wideband frequency. For the first stage, the structure used is cascoded Common-Source (CS) with current reused topology. In this stage, Transistor M1 operated as CS amplifier and connected in cascade with Transistor M2, which operated as Common-Gate (CG) amplifier. The CS amplifier act as the driver of the LNA by providing high voltage gain and the addition of Inductor L2 as a source inductive degeneration at the source of Transistor M1 provided good linearity.

In order provides wider bandwidth to satisfy UWB requirement, CG amplifier is connected at the drain of CS amplifier. While CG decrease the voltage gain (S21), the high- frequency performance of LNA is improved due to equivalent Miller capacitance is reduced at the output.

At the front end of RF input, Capacitor C1 acts as a dc blocking component and connected in series with Inductor L1 to provide good input matching performance. Current reused topology used Resistor R2 and Capacitor C2 as RC feedback components.

3.6 Components parameters

The complete sizing of transistors and all other component are listed in Table 3.1.

Component type	Component name	Component value
N- mosfet transistor	W1	W/L = 90 uM/130 nm
	W2	W/L = 70 uM/130 nm
	W3	W/L = 40 uM/130 nm
Inductor	L1	1n H
	L2	80p H
	L3	9n H
	L4	4.5n H
	L5	2n H
Capacitor	C1	100f F
	C2	300f F
Resistor	R1	1k Ω
	R2	800 Ω
	R3	800 Ω

Table 3.1 Components used in the schematic and their sizings

3.7 Conclusion

The good understanding of Cadence Virtuoso as an EDA tool to design the LNA is important in order to achieve good design specification. Designer can use the flowchart prepared in order to solve complicated problem arisen. It is important to understand the location of LNA is in a receiver so that the obtained specification should meet proper requirements such as high signal gain. In addition, the circuit's component parameter need to be adjusted correctly to be able to meet the desired results.

Chapter 4
Results and discussion

4.1 Introduction

The proposed LNA circuit schematic has been drawn using Cadence Virtuoso tool. Each of components such as resistor, transistor and inductor is given suitable value to meet the target IC specifications. The parameters optimized included transistor's sizing, transistor biasing voltages, power supply, capacitance and inductor values. The result simulated is intended to be as close as possible to desired target specification by rigorously optimizing component's parameters.

The analyses used in testing the LNA are s-parameter (SP), periodic steady state analysis (PSS) and DC analysis. SP analysis focuses on calculating linear small signal s-parameter around certain DC operating points. On the other hand, PSS is a large-signal analysis that runs around operating points which has frequency translation. DC analysis are performed to measure the current and voltage that passed through each components placed on the circuit.

4.2 S-Parameters analysis

S-parameters include information on the reflected incident power waves as well as the crosstalk between the lines. In other words, S-parameters describe the input-output relationship between 2 ports in the LNA circuit design. The parameters tested on the amplifier are input matching (S11), output matching (S22), gain (S21), and output reverse loss (S12). S11 is a measure of the input complex reflection coefficient when the output port is terminated with the match system load while S22 is

the output complex reflection coefficient when the input port is terminated with a match system load. S12 and S21 are forward and reverse transmission gain respectively. The S-parameter is simulated between frequency of 1-10 GHz and the result is shown in Figure 4.1

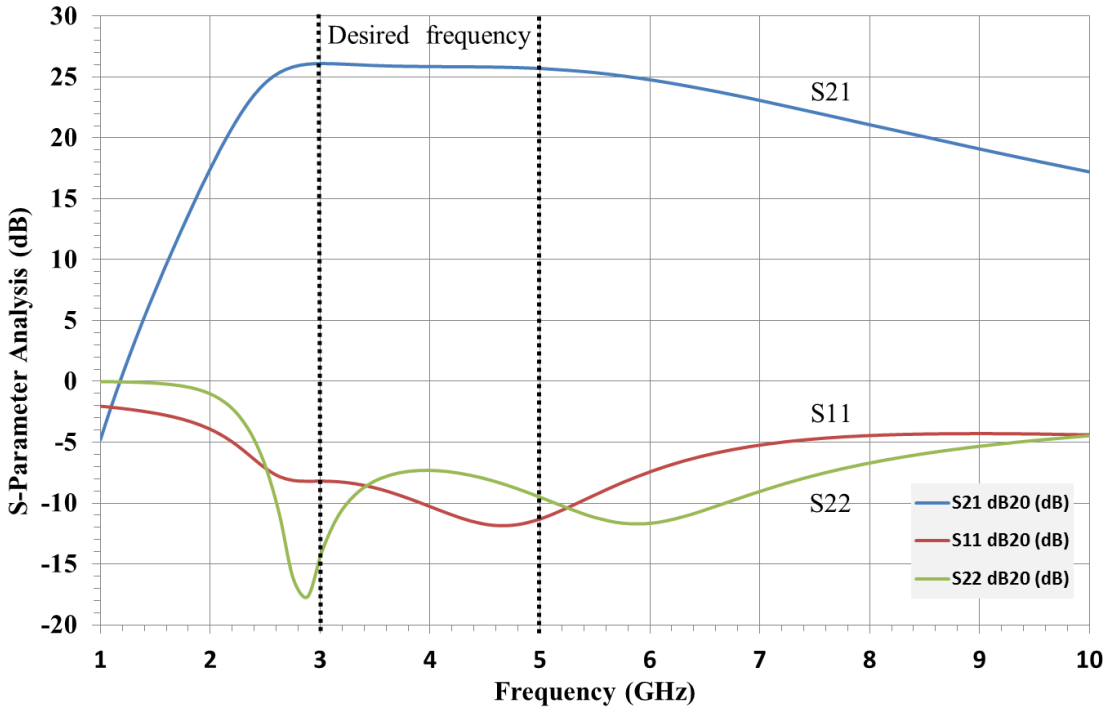

Figure 4.1: S-parameter response of LNA

Based on Figure 4.1, the LNA has a high gain of +26 dB with excellent flatness throughout 3-5 GHz. The gain flatness is maintained in desired bandwidth with variation of ±0.5 dB. The input matching is maintained below -8 dB and output matching below -7 dB throughout desired bandwidth. The input and output matchings are considered acceptable although they are less than the target value of below -10 dB. The good input matching value obtained is contributed by the usage of resistive shunt feedback and inductive source degeneration in the circuit. The circuit also employs resistive termination which further improves the input matching.

The output return loss is desired at to -40 dB. The s-parameters result is comparable to other products. The usage of cascode topology improve the reverse isolsation. The complete s-parameters are shown in Figure 4.2.

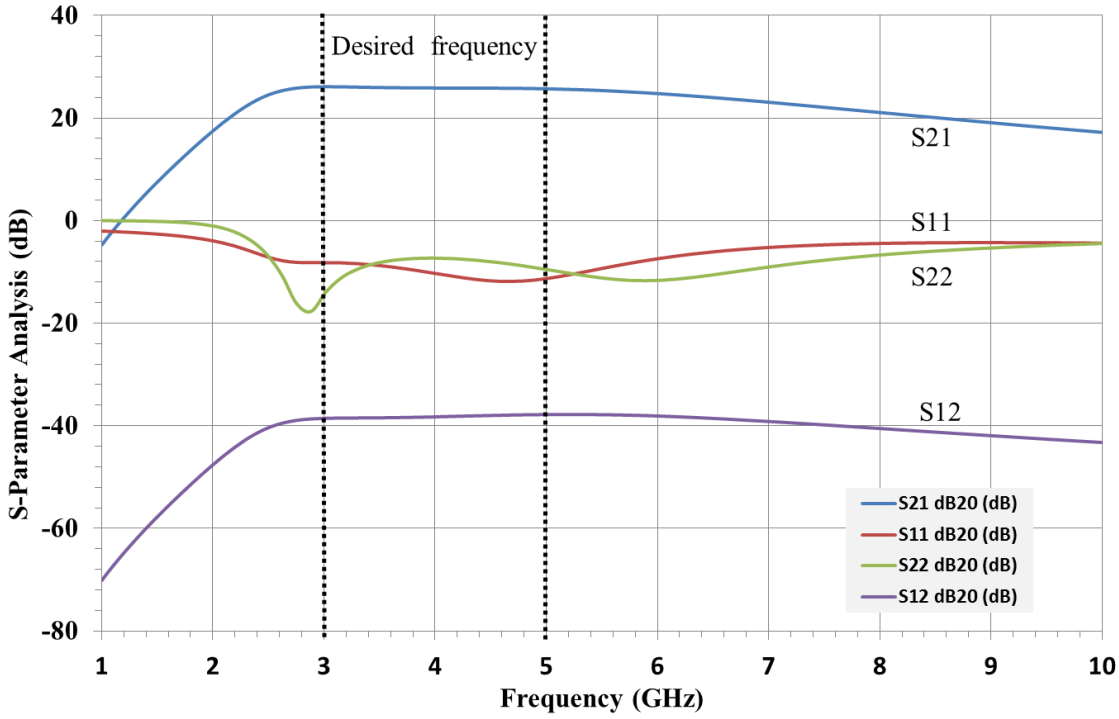

Figure 4.2 : S-parameter response of LNA

4.3 Noise analysis

Noise figure is used to determine the degradation in the Signal to Noise Ratio (SNR) as the LNA processes the signal. In a low noise amplifier, the output signal power must be greater than the output noise power, thus due to low output noise power, output SNR will increase. Noise figure for the LNA is measured using Spectre circuit simulator and the result is shown in Figure 4.3.

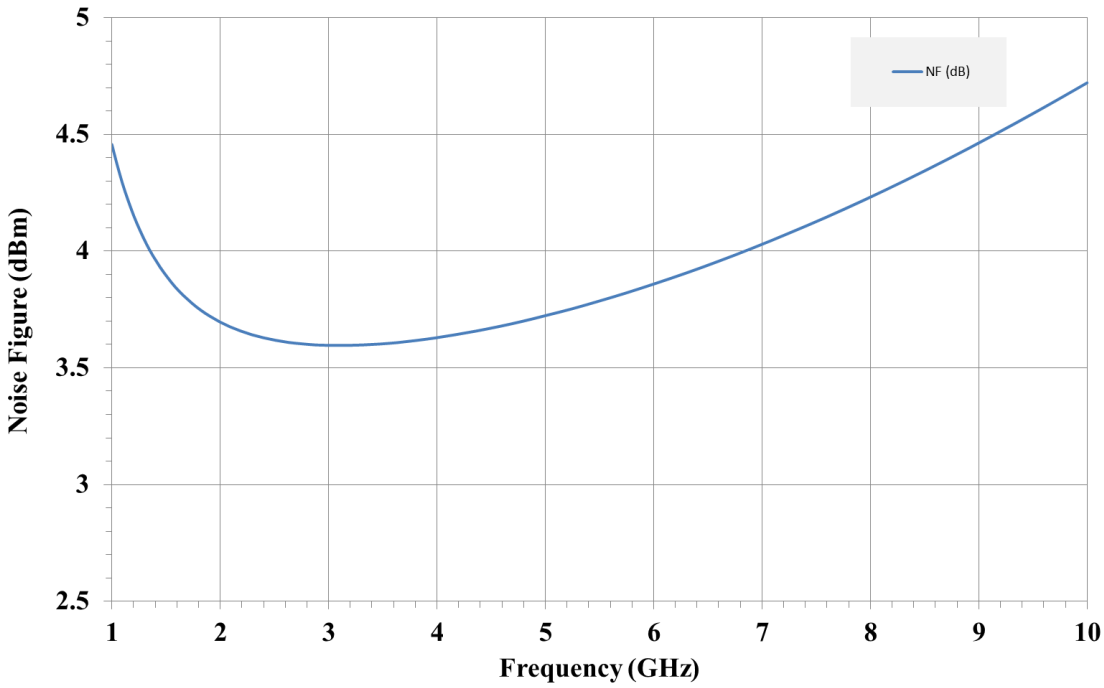

Figure 4.3: Overall S-parameter response of LNA

For this LNA, the overall noise figure (NF) of 3.7 dB can be seen from Figure 4.3. Value of noise figure increased exponentially as the gain increase in this two stage circuit design. The noise figure can be lowered by reducing the inductor that placed in after the input of radio frequency, but S11 quality will also decreased. There is a trade-off between noise figure (NF) and input reflection coefficient.

4.4 Stability analysis

Stability test is performed to verify whether the LNA designed is stabled or not. The LNA designed might become unstable when feedback occurs from output to the input under certain combinations of source and load impedances. The source of LNA instability might be come from manufacturing, voltage variation and unpredicted extreme frequencies. Stability analysis is performed using S-parameters measuremend using Cadence Spectre tool and the result is shown in Figure 4.4.

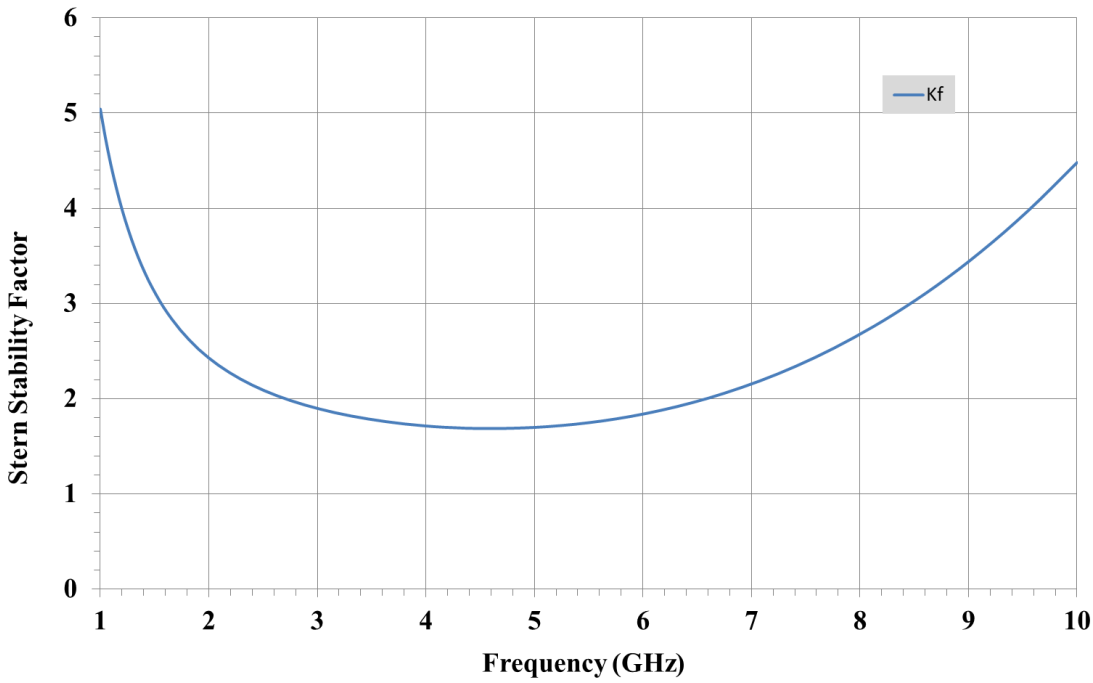

Figure 4.4 Stability analysis

If $K_f > 1$, the circuit is said to be unconditionally stable. From the Figure 4.4, the designed LNA is proved to be un-conditionally stable as stability analysis shows that $K_f > 1$ throughout 3-5 Ghz bandwidth and bias conditions. The unconditional stability achieved means that the LNA will become stable with the presence of any load to the input or output of the amplifier. The stability achieved can be attributed to the adding of shunt conductance at input port.

4.5 Linearity analysis

Linearity is one of crucial parameter in all RF systems beside S-parameter analysis as it indicate the output level of intermodulation and higher order harmonics. The LNA must have high linearity to prevent the intermodulation tones created by the interference signal from corrupting the carrier signal. Using periodic steady-state (PSS) analysis, linearity of LNA is determined.

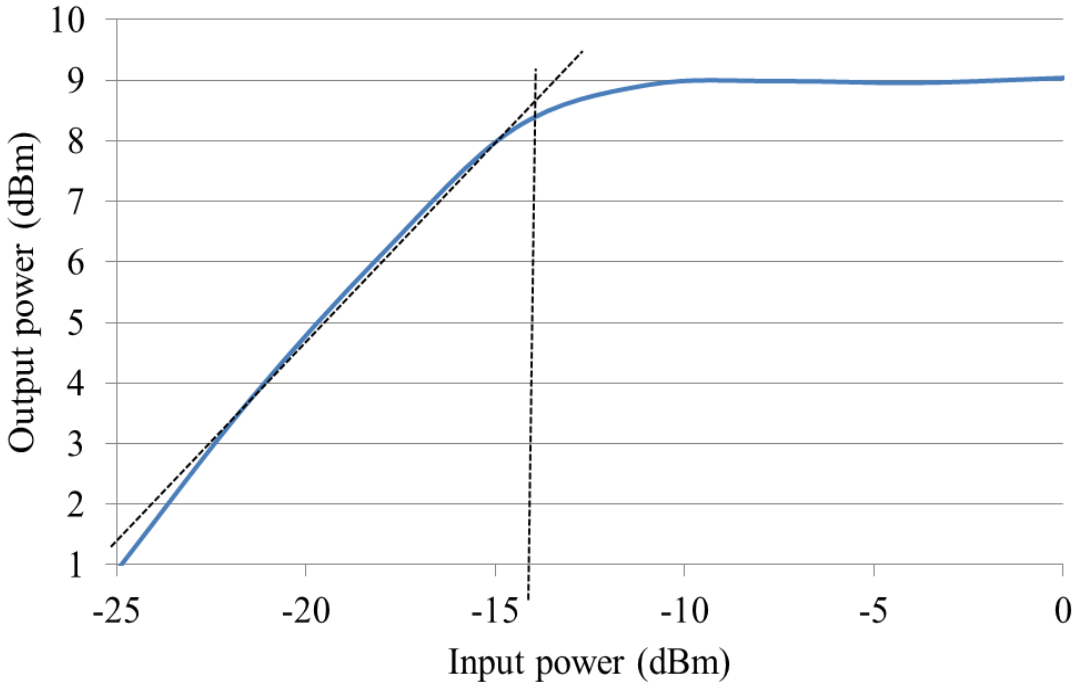

Figure 4.5 P1dB compression point

. From Figure 4.4, the linearity analysis with P1dB gain compression point 0f --14 dBM at 4 Ghz. The acceptable linearity possessed by the LNA prevent the interference signal produce form intermodulation tone from corrupting the carrier signal. The linearity analysis is continued with Third Order Intercept Point simulation which shown in Figure 4.6.

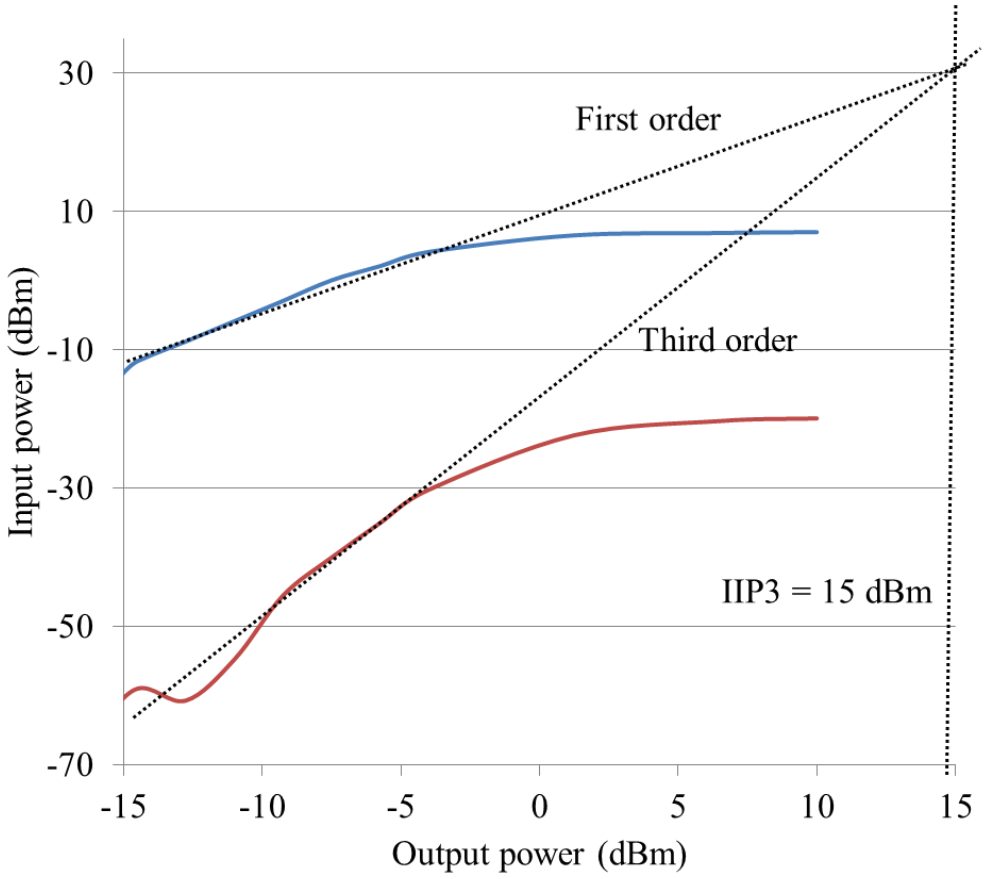

Figure 4.6 Third order intercept point simulation

Intercept point (IP3) is the extrapolated point where the curvs of the fundamental signal and third order intercept. By referring Figure 4.6, the input power level IIP3 is -15 dBM. The linearity result concluded that the LNA can tolerate to multiple RF signals outside the bandwidth of interest.

The IIP3 analyse were conducted at frequency of 4 GHz and 4.1 GHz. The beat frequency is set to 10 kHz. The simulation took considerable amount of time to complete as the simulator need to analyse from 4GHz to 4.1 GHz by increment of 10 kHz.

4.6 Group delay analysis

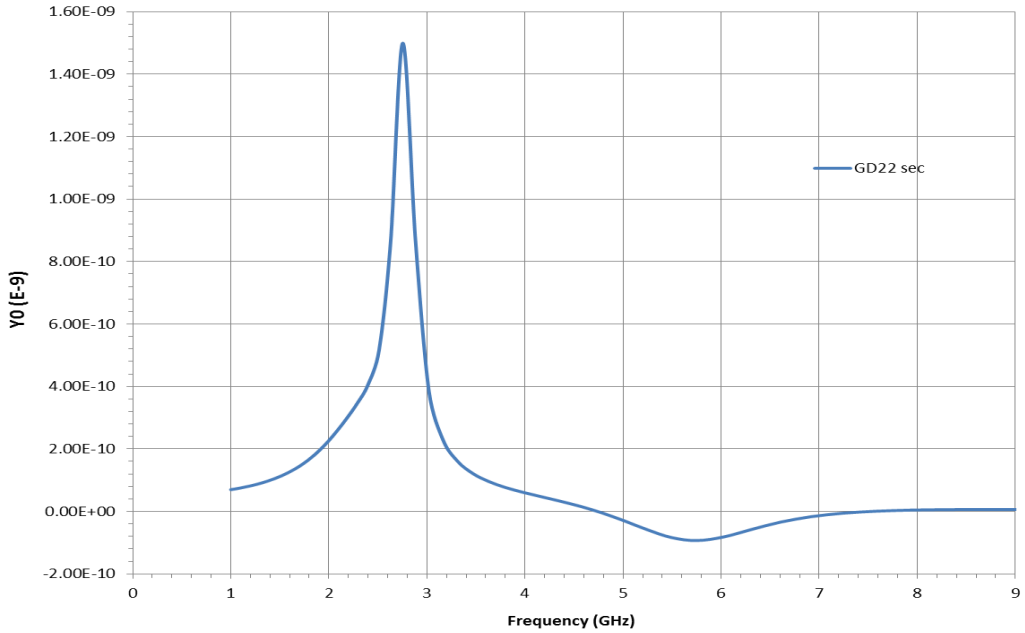

Figure 4.7 Group delay analysis

Group Delay is a measurement of transit time of a signal through the LNA versus frequency. In addition, the group delay curve also indicates how much a device will distort a signal. Based on Figure 4.7, group delay of the LNA is ± 75ps.

4.7 IC layout

After the designed LNA is simulated with various tests and the result specifications obtained are satisfactory, the final procedure for the IC design is layout drawing. The layout is created using Cadence Virtuoso Layout Editor based on CMOS 0.13-um process technology. The complete layout drawing is shown on Figure 4.8.

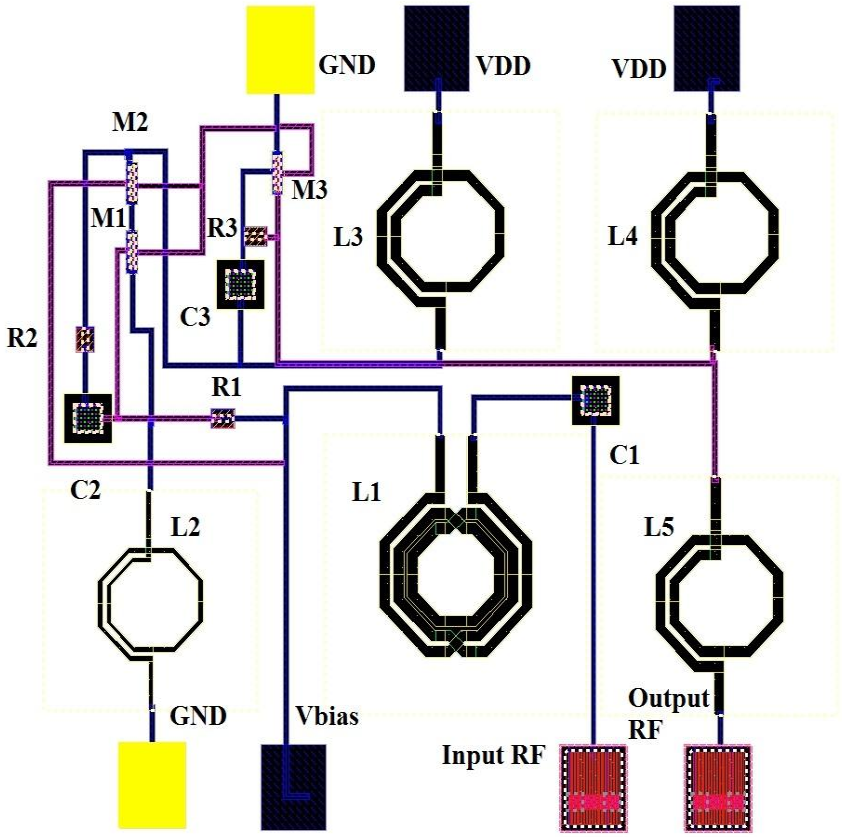

Figure 4.8 LNA IC layout

Based on the layout drawn, the die area including the bond pads is 0.72 mm by 0.74 mm. Thus, the calculated total area the LNA takes is 0.53 mm^2. Layout for the LNA is reduce its size by putting the components in efficient space. Layout size for the LNA have to be as small as possible for several reasons that explained as below.

The LNA must have smallest space as possible so it can be placed alongside with other components of a wireless receiver system which has limited chip area. Another reason is to achieve high speed and minimum power dissipation due to unnecessary extension of components. In addition, the fact that more chips per wafer can be acquired resulting in lower production cost thus make the design relevant in the market.

In the layout, there are only types of metal used for interconnection between components, which are Metal 1 and Metal 2. The use of only two materials for interconnection results in better cost due to less complicated fabrication process step. In addition, component wear out failure can be subsequently reduce because less usage of vias for connecting different metal types.

The capacitor type used in the layout is metal–insulator–metal (MIM) capacitor. MIM capacitor is preferred as it possessed better linearity, higher tolerance to process variations, higher breakdown voltage, and lower temperature coefficient compared to its counterpart, which is metal-oxide-metal (MOM) capacitors. However, MIM falls short in terms of fabrication cost and capacitance density compared to MOM. Also spiral inductor type is used as they have many advantages such as low tolerance value, cheap fabrication cost large range of temperature operation and able to withstand mechanical vibration.

4.8 Product comparisons

The data from every simulation done is recorded and tabulated for comparison purpose. Previous LNA design for UWB application from other works also search and tabulated to be compared with current product. The other research paper taken is from V.P. Bhale that uses single stage topologies and named as Research Paper 1 at the table. Research Paper 2 is also from V.P. Bhale that used single stage cascode amplifier. The full summarisation of comparisons between current and previous research papers is shown in Table 4.1.

Table 4.1 Summarisation of products comparisons

References	Research Paper 1	Research Paper 2	Research Paper 3	This research
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS
Frequency of Operation	3- 5 GHz	3-5 GHz	3- 5 GHz	3-5 GHz
Supply Voltage	1.8 V	1.8 V	1.8 V	1.2 V
Gain	12.7 dB	22 dB	8.6- 9.5 dB	26 dB
S11	< -6 dB	<-10	<-10	<-8
S22	< -8 dB	<-10	-----	<-7
S12	-26.8 dB	-40 db	-----	-37 dB
NF	2.31 dB	3.5 dB	2.7 dB	3.7 dB
NFmin	2.158 dB	3 dB	-----	3 dB
P1db	-6.46719 dB	-----	-----	-14 dBm
IIP3	------	----	---	15 dBm
Power Consumption	11.7 mW	12.5 mW	15 mW	21.6 mW
Stability	Stable designs	Stable Design	-----	Stable Design
Group Delay	---	---	-----	± 75ps
Chip size	----	----	-----	0.53 mm^2

High gain is one of the important specification of LNA because the signal processed need to pass to the subsequent stages in a receiver system. Based on table 4.1., designed LNA have amplifier gain of 26 dB. The gain value is highest compared to other product. The highest gain among previous LNA works is Product 2 which is 22 dB. Due to the fact that the LNA improves the gain of previous product by 18%, it is suitable to be used in specific wireless applications that required high gain. The LNA also tested to be an unconditional stable design.

In general, S11 should have value as low as possible to allow more signal pass through without being reflected and avoid interferences from reflected signal. The value of input matching, S11 and output matching, S22 of this product are < -8 and < -7, respectively. The matching network value of this LNA is higher than two other products but lower than Product 1 which has < -6 dB for S11 and < -8 dB for S22. However, the difference with superior matching network is 3 dB which is minimal.

The designed LNA has noise figure of 3.7 dB, which is just 0.2 dB higher than Product 2 that also used cascode amplifier topology (3.5 dB).. The power consumption of LNA is 21.6 mW, which it achieved the calculated target specification. The disadvantage some of the parameter is the tradeoff that unable hard to adjust in radio frequency Ic design process. The drawback by some parameters such as power consumption and noise figure are trade off that needed to be tolerated with in radio frequency IC design process.

Chapter 5
Conclusion and future work

5.1 Conclusion

As the world progressed with new technology, wireless devices created for various purposes crowded existing wireless frequency spectrum to transmit information. UWB technology is an emerging frequency that allows high bandwidth transmission from 3.1 GHz to 10.6 GHz.

Common-gate circuit topology is not suitable for operation of LNA in wideband frequency. The topology chose is two stage cascode amplifier with a common source amplifier at last stage. The circuit also employed current-reused technique with RC feedback to obtain higher gain.

The analyses of designed LNA achieved excellent results. The LNA has gain of 26 dB, which is an improvement compared to previous work by 18%. The flatness of the gain throughout the desired gain is very good. Input and output matching of the LNA are comparable to other products while the linearity of the IC is under acceptable range. Also, noise figure obtained is in range with desired specification which is 3.7 db along with group delay which is 75ps. The chip layout designed has reasonable size of 75 mm.

In every radio-frequency IC, there always performance trade-offs that needed to be balanced. Although power consumption of the LNA met target desired specification which 21.6 mW, it is the highest compared to other products.

5.2 Future work

As the technology keep progressing rapidly, the designed LNA must be improved such that the disadvantages is reduced. The power consumption issue of the LNA can be improved by efficiently reducing the transistor's width and it's threshold voltage. The power consumption also can be reduced by revising the circuit topology and reducing number of circuit components. The input and output matching of the LNA can be improved by increasing the inductance value near the input frequency.

A well-designed IC are only beneficial as it through the end of fabrication processes. Using the layout designed, the LNA can be turned into touchable product by manufacture it in local semiconductor fabrication plant. It is hoped that this LNA design could be improved further and give numerous benefits to industries.

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