UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402
Computer Assignment 4-5
State Machine and Basic RTL
Quartus Pre-and Post-Layout Simulation

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Simulation:

SerIn ─── 1

┌─────────────────────┐
│ 6 bit   │   SO
en-6shift ──│ righ Shitr Registr │──────
└─────────────────────┘

┌──────────────┐
│ DCD   │
└──────────────┘
en-Dcd

┌─────────────┐
│   X·8   │   eq-gt
en-byte ──│   │
└─────────────┘

7   A   ┌───────┐   eq
             │ A ⩾ B │
             │   │   gt
         B   └───────┘

┌─────────────────────┐
│ 7 bit up Countr   7 │
en-byte ──│   │
└─────────────────────┘

P3

P2

P1
P0

SerIn ──┐ ┌─────────┐
        │ │   DFF   │
en-byte └──│   │
           └─────────┘

┌───────────────┐   ┌──────────────┐
│   │   SO ──→ │   │ ──→ en-6shift
│ Data Path   │ eq-gt ──→│ Controller │ ──→ en-byte
│   │ SerIn ──→│   │ ──→ en-Dcd
│   │   │   │ ──→ OutValid
└───────────────┘   └──────────────┘ ──→ error