University of Tehran

Electrical and Computer Engineering Department

ECE (8101) 342 - Object Oriented Modeling of Electronic Circuits – Spring 1402-03

Computer Assignment 1 – C++ Logic Modeling

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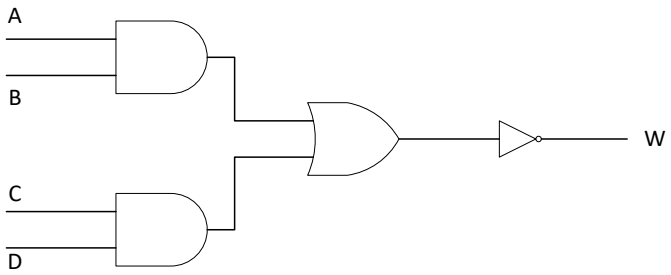
Name:	**Date:**

In this exercise, your task is to design a functional model extractor. This involves converting a netlist comprising of basic AND, OR, and NOT gates into a Boolean expression. We refer to this expression as a function representing a gate cluster. The primary objective is to improve simulation speed and simplify logic simulation.

Your input is a Verilog netlist description using AND, OR and NOT gates. The objective is to translate this description to a functional Verilog description of the netlist with the same number of inputs and outputs as the original netlist, and as many expressions (**assign** statements) as the number of outputs.

A Verilog testbench is to be created to test the two circuits alongside each other with the name test data.

A sample "input.v" file is available in the attachments that describes the circuit shown below and the functional equivalent of this circuit, "expected_output.v".



Guidelines:

- Write a clear and comprehensive work report for this exercise, detailing all stages of your work along with the overall methodology.
- Ensure that your code is clean, readable, and appropriately commented when necessary.
- This exercise requires in-person submission, and your code will be tested using an independent undisclosed testbench.
- You only have to support the style used in the "input.v" file. Your input is line-oriented with gate instances on separate lines.