PCSrc Control Unit branch LEG_ ResultSrc_{1:0} MemWrite funct7₅ ALUControl_{2:0} funct3 ALUSrc ImmSrc_{1:0} RegWrite CLK CLK CLK WE WE3 SrcA Zero ● PCNext RD1 Instr ReadData RD MZIR **ALUResult** RD Instruction A2 RD2 SrcB Data Memory Memory WD3 Register WriteData WD 7 PcImm Added **PCTarget ImmExt Extend** Pc4Adder+ PCPlus4 Result Immentend

		PCSrc	ResultSrc	MemWrite	ALUControl	ALUSrc	ImmSrc	RegWrite
R-Type	add	00	00	0	000	0	XXX	1
	sub	00	00	0	001	0	XXX	1
	and	00	00	0	010	0	XXX	1
	or	00	00	0	011	0	XXX	1
	slt	00	00	0	101	0	XXX	1
І-Туре	lw	00	01	0	000	1	000	1
	addi	00	00	0	000	1	000	1
	xori	00	00	0	100	1	000	1
	ori	00	00	0	011	1	000	1
	slti	00	00	0	101	1	000	1
	jalr	10	10	0	000	1	000	1
S-Type	SW	00	XX	1	000	1	001	0
J-Type	jal	01	10	0	XXX	X	010	1
В-Туре	beq	zero ? 01 : 00	XX	0	001	0	011	0
	bne	zero ? 00 : 01	XX	0	001	0	011	0
	blt	aluresult[0] ? 01 : 00	XX	0	101	0	011	0
	bge	aluresult[0] ? 00 : 01	XX	0	101	0	011	0
U-Type	lui	00	11	0	XXX	X	100	1