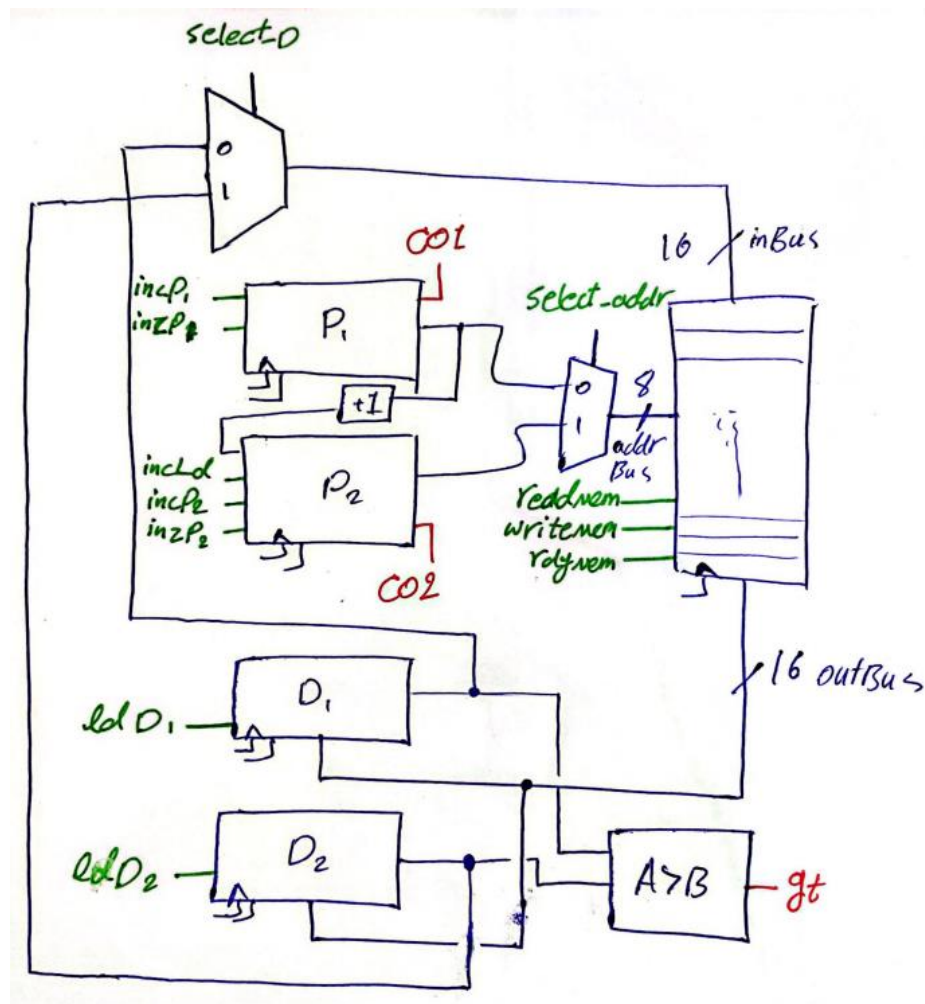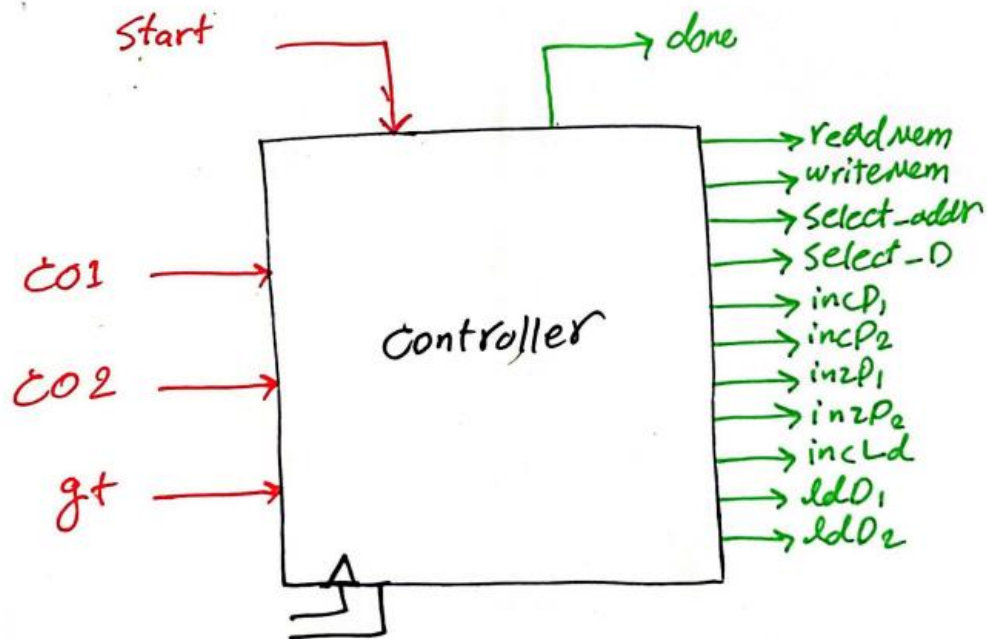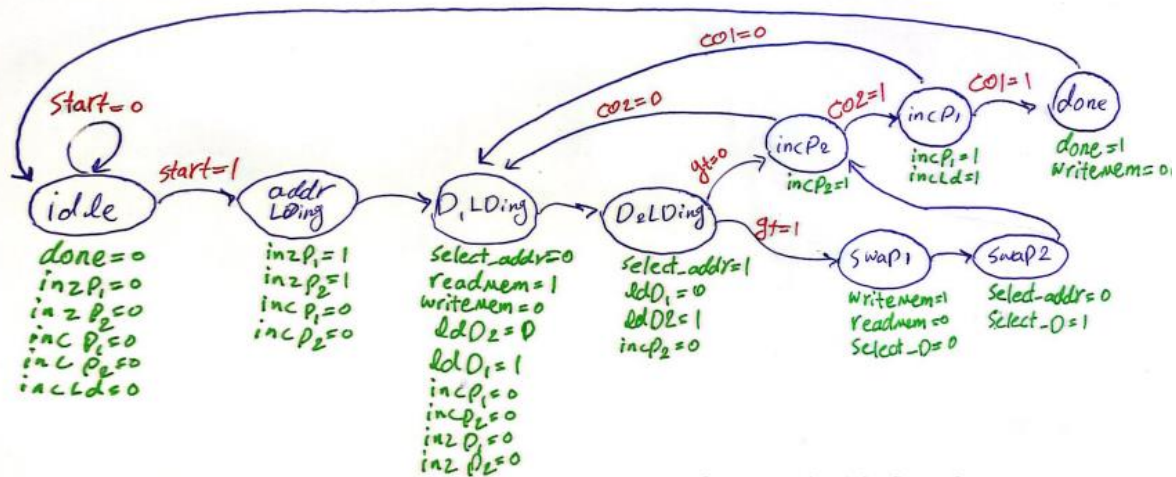**UNIVERSITY OF TEHRAN**
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894 Spring
1402
Computer Assignment 6
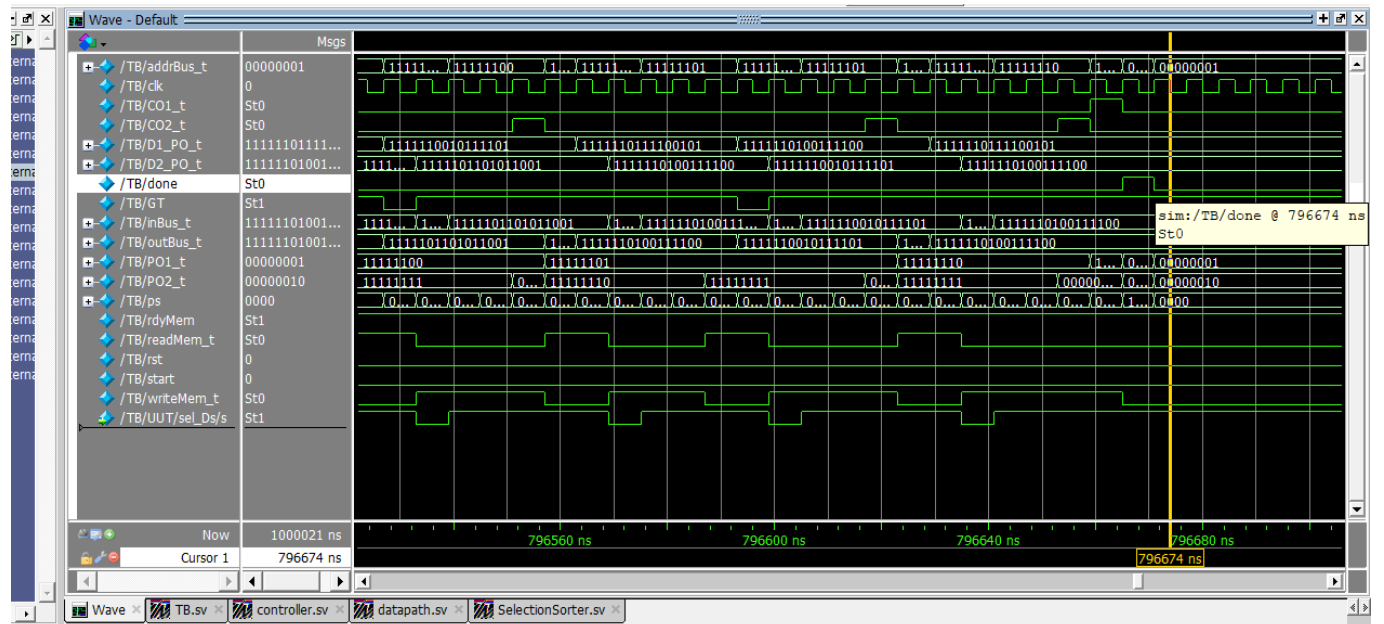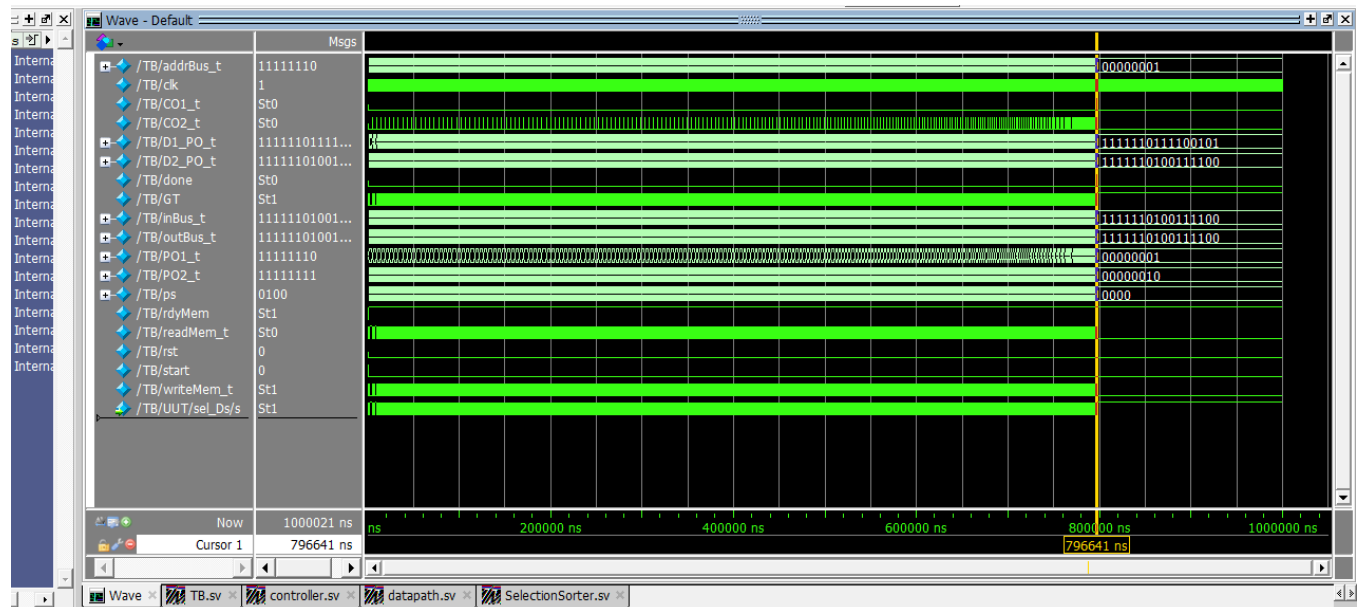**RT Leve Component Design and FPGA Implementation – Week 24**

Name: Amirhesam Jafari rad / 810100247
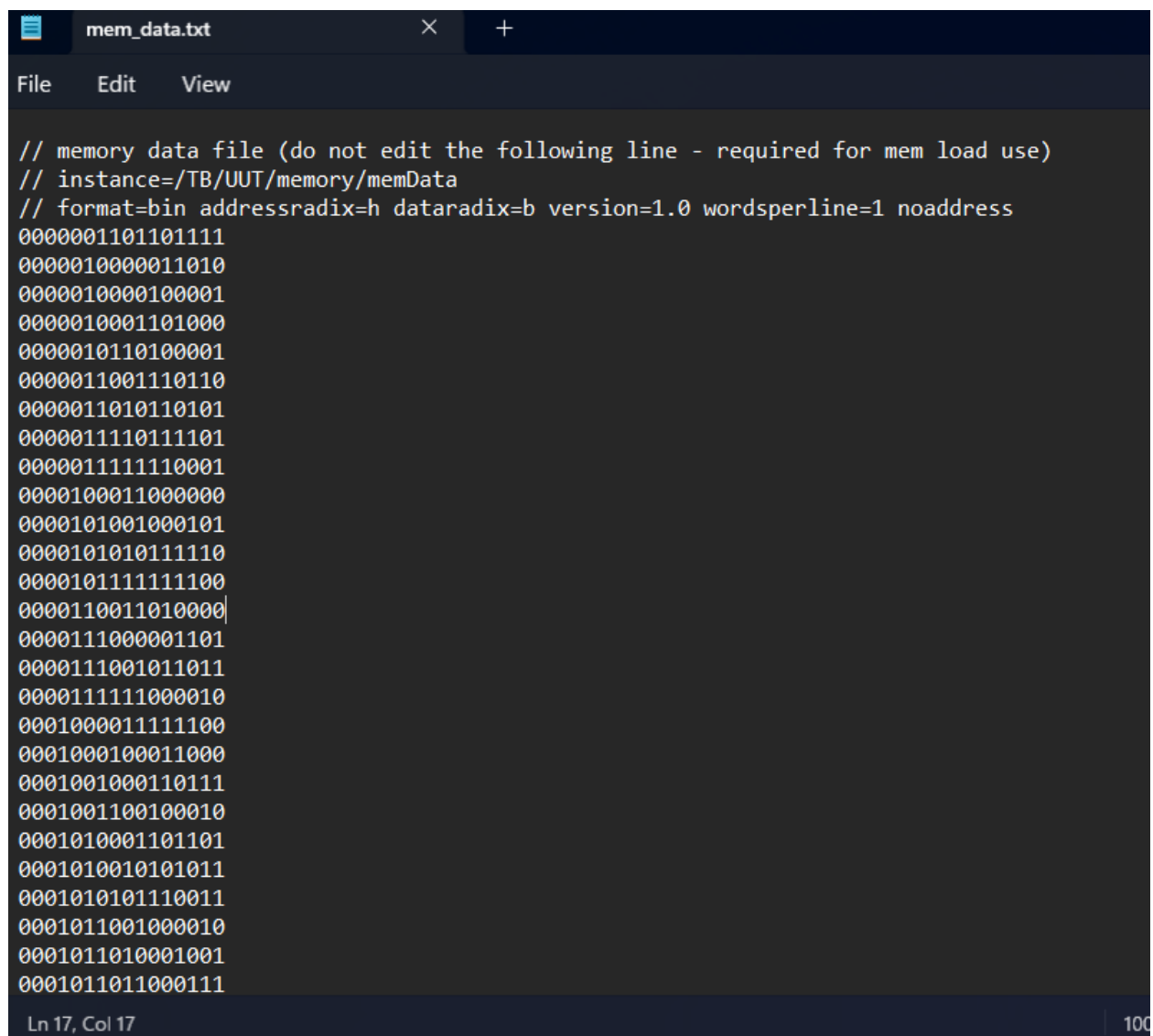
Date: 1402/3/23

a)

State Diagram

Transitions:
- idle → idle: Start = 0
- idle → addr LDing: start = 1
- addr LDing → D_1 LDing
- D_1 LDing → D_2 LDing
- D_2 LDing → incP2: gt = 0
- D_2 LDing → Swap1: gt = 1
- Swap1 → Swap2
- Swap2 → incP2
- incP2 → incP1: CO2 = 1
- incP2 → D_1 LDing: CO2 = 0
- incP1 → done: CO1 = 1
- incP1 → D_1 LDing: CO1 = 0
- done → idle

States and outputs:

idle
- done = 0
- $inzP_1 = 0$
- $inzP_2 = 0$
- $incP_1 = 0$
- $incP_2 = 0$
- incLd = 0

addr LDing
- $inzP_1 = 1$
- $inzP_2 = 1$
- $incP_1 = 0$
- $incP_2 = 0$

D_1 LDing
- Select_addr = 0
- readmem = 1
- writemem = 0
- $ldD_2 = 0$
- $ldD_1 = 1$
- $incP_1 = 0$
- $incP_2 = 0$
- $inzP_1 = 0$
- $inzP_2 = 0$

D_2 LDing
- Select_addr = 1
- $ldD_1 = 0$
- $ldD_2 = 1$
- $incP_2 = 0$

incP2
- $incP_2 = 1$

incP1
- $incP_1 = 1$
- incLd = 1

done
- done = 1
- writemem = 0

Swap1
- writemem = 1
- readmem = 0
- Select_D = 0

Swap2
- Seled-addr = 0
- Select_D = 1

Controller

Inputs: Start, CO1, CO2, gt

Outputs: done, readmem, writemem, Select_addr, Select_D, $incP_1$, $incP_2$, $inzP_1$, $inzP_2$, incLd, ldD_1, ldD_2

B)

Sorted Memory:

```
// memory data file (do not edit the following line - required for mem load use)
// instance=/TB/UUT/memory/memData
// format=bin addressradix=h dataradix=b version=1.0 wordsperline=1 noaddress
0000001101101111
0000010000011010
0000010000100001
0000010001101000
0000010110100001
0000011001110110
0000011010110101
0000011110111101
0000011111110001
0000100011000000
0000101001000101
0000101010111110
0000101111111100
0000110011010000
0000111000001101
0000111001011011
0000111111000010
0001000011111100
0001000100011000
0001001000110111
0001001100100010
0001010001101101
0001010010101011
0001010101110011
0001011001000010
0001011010001001
0001011011000111
```

Ln 17, Col 17   100