UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1400-01
Computer Assignment 2
Hierarchical iterative circuits
Week 6

Name:

Date:

This problem uses transistors and gates of Assignment 1 to build a cascadable 1-bit comparator. It then uses the 1-bit comparator to build a cascadable 4-bit comparator, and then hierarchically builds a 16-bit comparator.

1. A five-input, three-output circuit has *a, b, l, e, g* inputs and *L, E,* and *G* outputs. If *ab* is 01, the *L* output becomes 1. If *ab* is 10, the *G* output becomes 1. If *ab* is 00 or 11, outputs *L, E, G* get values on inputs *l, e,* and *g*.

a. Use gates developed in Assignment 1 to build the *L, E,* and *G* outputs. This circuit is referred to as *bit_comparator*.

b. Hand-analyze the circuits developed here to find the worst-case delay values for the three outputs.

c. Develop a testbench to test the three outputs for functional verification and for a delay calculation that is more accurate than the hand-analysis of Part b.

d. Using delay values from Part c, write a SystemVerilog module for the *bit_comparator* circuit using **assign** statements.

e. Run simulations to compare circuits of Part a and Part d. The *bit_comparator* that is carried over to the next problem is that developed in Part d of this problem.

2. In this problem you will develop a 4-bit cascadable comparator.

a. Cascade four units of the *bit_comparator* of Part d of Problem 1 to build a cascadable *quad_comparator*. The inputs and outputs are as they are with the *bit_comparator* except that the *a* and *b* inputs are 4-bit vectors, i.e., *a[3:0]* and *b[3:0]*. This description consists of four instantiations of the *bit_comparator* module.

b. Hand-analyze the circuit developed above to find the worst-case delay values for the three outputs. The worst-case delay values are to be based on the *bit_comparatr* delay values developed in Problem 1 Part d. Use your calculated delay values in the *quad_comparator* module.

c. Develop a testbench to test the three outputs for functional verification and for a delay calculation of *quad_comparator* module that is more accurate than the hand-analysis of Part b.
d. Using delay values from Part c, write a SystemVerilog module for the *quad_comparator* circuit using **assign** statements.
e. Run simulations to compare circuits of Part b and Part d. The *quad_comparator* that is carried over to the next problem is that developed in Part d of this problem.

3. In this problem you will develop a 16-bit cascadable unsigned and a signed comparator.

a. Cascade four units of the *quad_comparator* of Part d of Problem 2 to build a cascadable *hex_comparator*. The inputs and outputs are as they are with the *quad_comparator* except that the *a* and *b* inputs are 16-bit vectors, i.e., *a[15:0]* and *b[15:0]*. This description consists of four instantiations of the *quad_comparator* module.
b. Hand-analyze the circuit developed above to find the worst-case delay values for the three outputs. The worst-case delay values are to be based on the *quad_comparatr* delay values developed in Problem 2 Part d. Use your calculated delay values in the *hex_comparator* module.
c. Develop a testbench to test the three outputs for functional verification and for a delay calculation of the *hex_comparator* module that is more accurate than the hand-analysis of Part b.
d. Using delay values from Part c, write a SystemVerilog module for the *hex_comparator* circuit using **assign** statements.
e. Run simulations to compare circuits of Part b and Part d. The *hex_comparator* of Part d becomes your final 16-bit comparator.
f. Use the *hex_comparator* of Part e to build a signed 16-bit comparator. We refer to this comparator as *hex_comparator_signed*. Run simulations to verify the timing and operation of the 16-bit signed comparator.

Deliverables:

Generate a report that includes all the items below:

A. For Parts 1, 2, and 3, do Parts a and b on paper. Make sure your SystemVerilog descriptions of the rest of the problems correspond to the circuit diagram that you have documented.
B. Calculate hand simulations and include your arithmetic in the report. On paper, show your timing extractions from the waveforms. Show waveform images as proof of simulation. Your simulation run and the project built for this purpose must be demonstrated to the TA.
C. For Parts e of the three problems and Part f of Problem 3, show waveforms that prove the correct operation of your circuits.
D. All project files and waveforms must be demonstrated to the TA. Using waveforms, circuit diagrams, and other circuit representations justify your answers for functional correctness, timing, and gate counts.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.