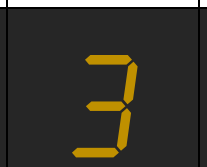
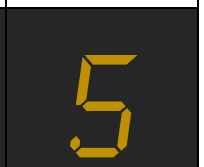
SUTECH FPGA 1400 {Input no.1}

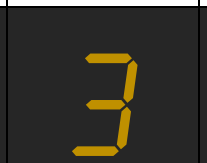
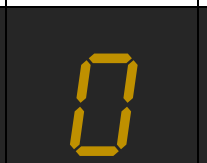
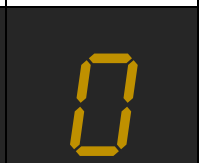
Set initial clock to the following input:

HIN_1	HIN_0	MIN_1	MIN_0
			
0x06	0x70	0x79	0x5f

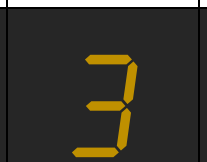
Set an alarm at:

HIN_1	HIN_0	MIN_1	MIN_0
			
0x06	0x70	0x79	0x5b

Your digital clock's alarm should start at:

HOUT_1	HOUT_0	MOUT_1	MOUT_0	SOUT_1	SOUT_0
					
0x06	0x70	0x79	0x5b	0x7e	0x7e

and it should stop at:

HOUT_1	HOUT_0	MOUT_1	MOUT_0	SOUT_1	SOUT_0
					
0x06	0x70	0x79	0x5b	0x06	0x7e