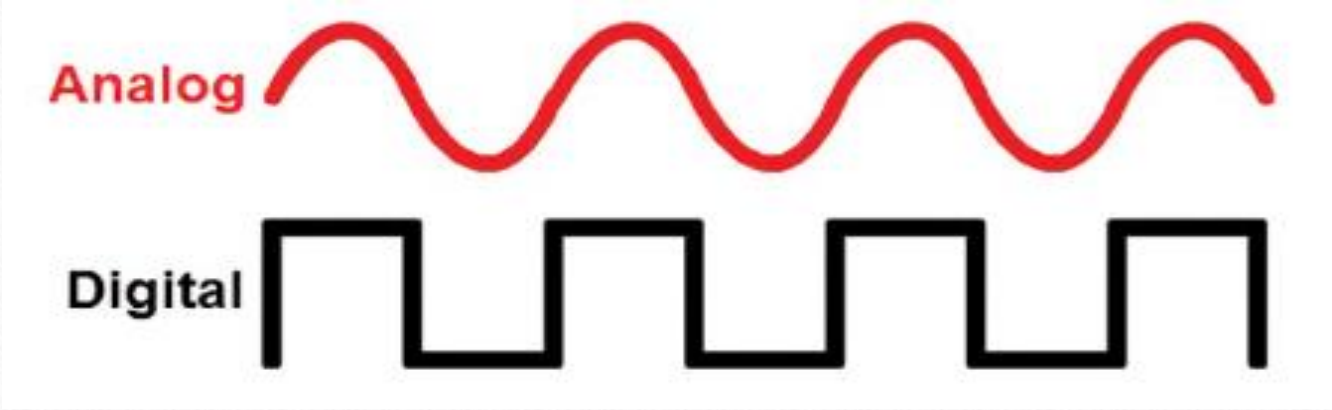
Digital Modulation

Digital VS Analog

- provides more information **capacity**
- high data **security**
- quicker system availability with great **quality** communication



digital modulation techniques

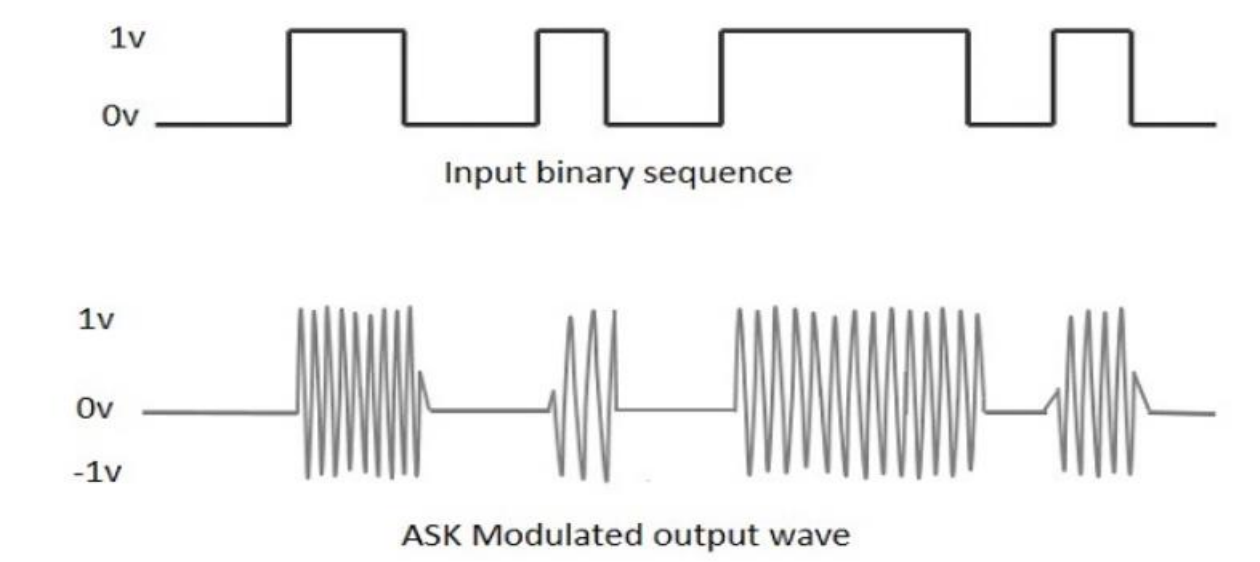
1. ASK – Amplitude Shift Keying
2. FSK – Frequency Shift Keying
3. PSK – Phase Shift Keying (BPSK, QPSK, DPSK)
4. M-ary Encoding (M-ary ASK, M-ary FSK, M-ary PSK)

- Data Rate And Baud Rate

5. QAM – Quadrature Amplitude Modulation
6. APSK – Amplitude Phase Shift Keying

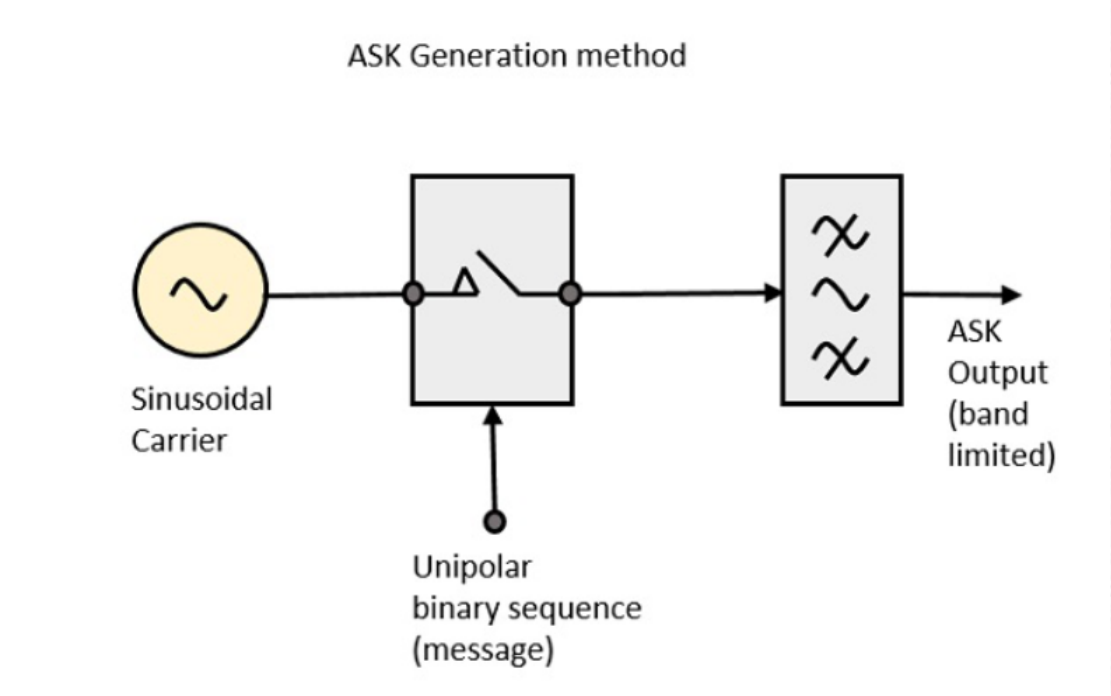
Amplitude Shift Keying ASK

- Any modulated signal has a high frequency carrier. The binary signal when ASK modulated, gives a **zero** value for **Low** input while it gives the **carrier output** for **High** input.



ASK Modulator

- The carrier generator, sends a continuous high-frequency carrier. The binary sequence from the message signal makes the unipolar input to be either High or Low. The high signal closes the switch, allowing a carrier wave. Hence, the output will be the carrier signal at high input. When there is low input, the switch opens, allowing no voltage to appear. Hence, the output will be low.

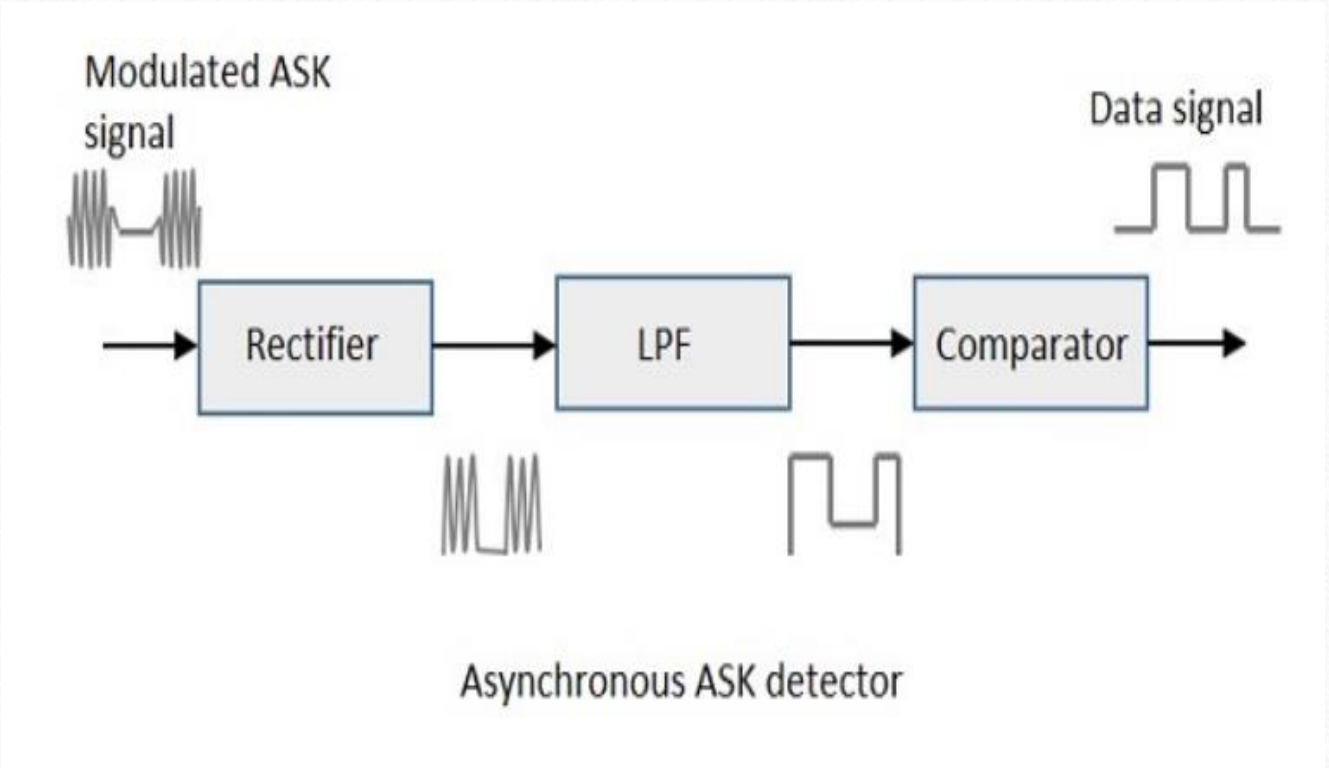


ASK Demodulator

- Asynchronous ASK Demodulation/detection
- Synchronous ASK Demodulation/detection

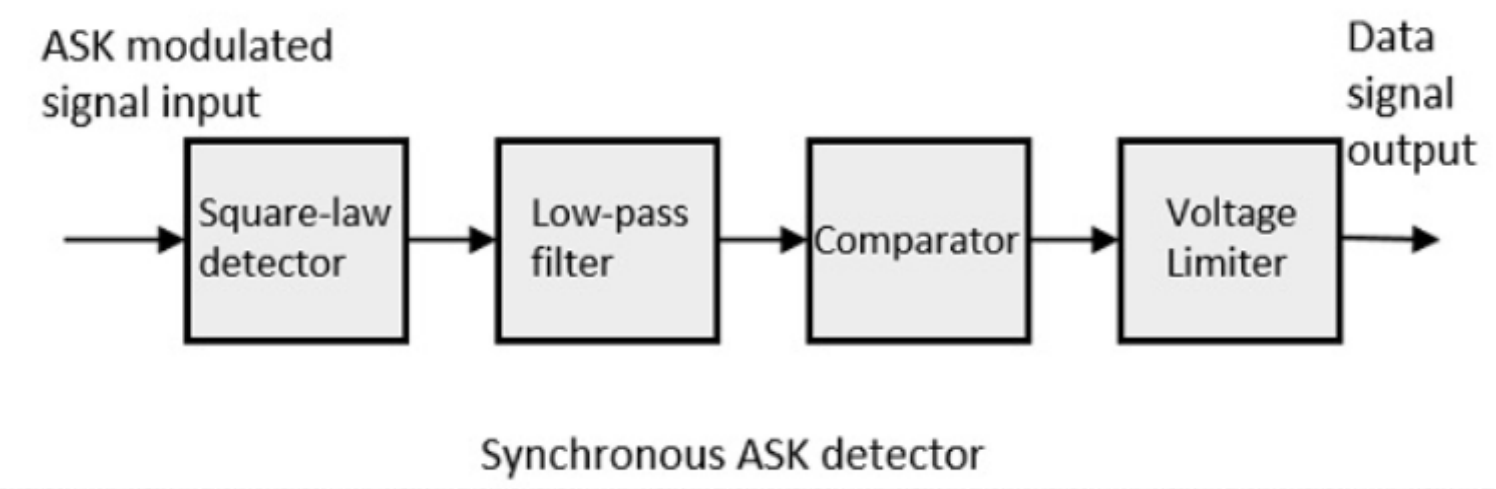
Asynchronous ASK Demodulator

- The Asynchronous ASK detector consists of a half-wave rectifier, a low pass filter, and a comparator.
- The modulated ASK signal is given to the half-wave rectifier, which delivers a positive half output. The low pass filter suppresses the higher frequencies and gives an envelope detected output from which the comparator delivers a digital output.



Synchronous ASK Demodulator

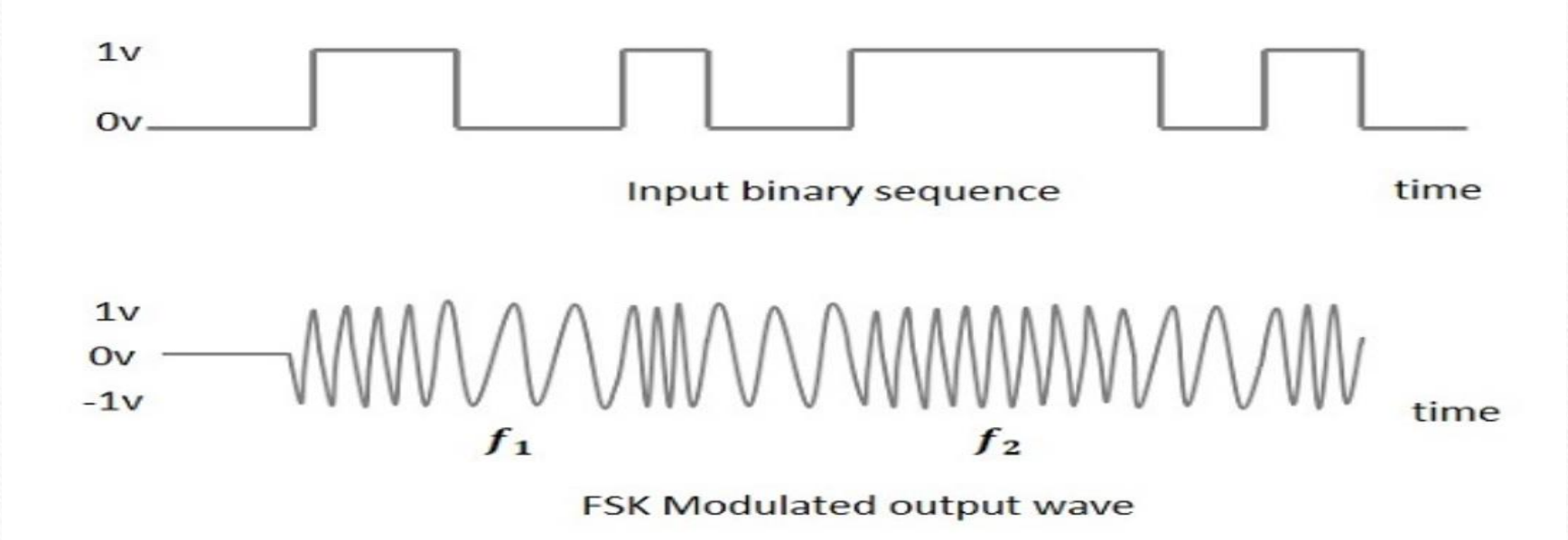
- The ASK modulated input signal is given to the Square law detector. A square law detector is one whose output voltage is proportional to the square of the amplitude modulated input voltage. The low pass filter minimizes the higher frequencies. The comparator and the voltage limiter help to get a clean digital output.



Synchronous ASK detector

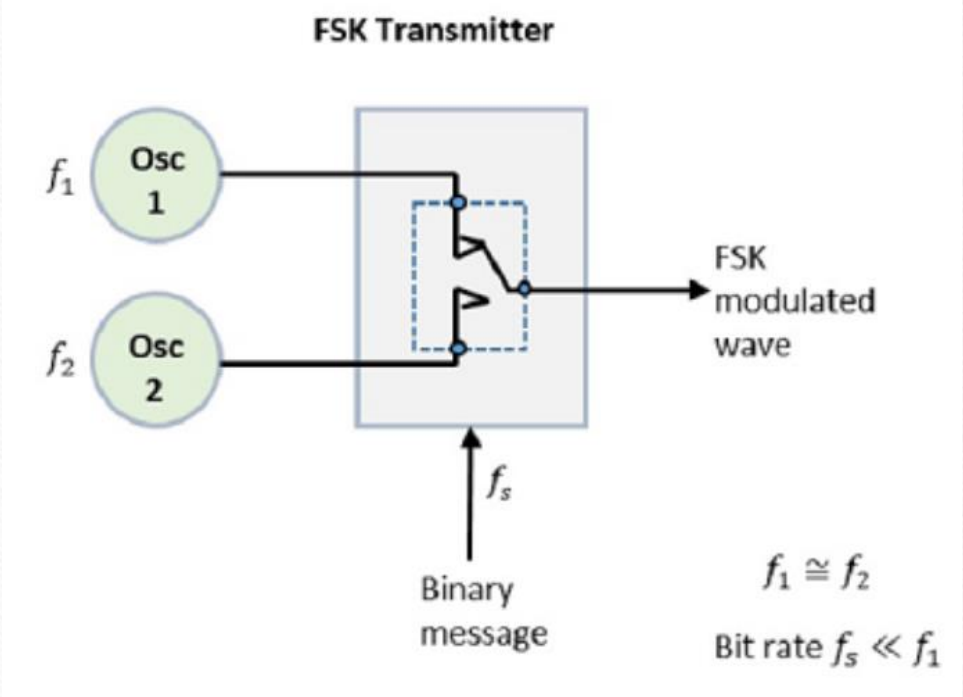
Frequency Shift Keying FSK

- frequency of the carrier signal varies according to the digital signal changes. FSK is a scheme of frequency modulation.



FSK Modulator

- The two oscillators, producing a higher and a lower frequency signals, are connected to a switch along with an internal clock. To avoid the abrupt phase discontinuities of the output waveform during the transmission of the message, a clock is applied to both the oscillators, internally. The binary input sequence is applied to the transmitter so as to choose the frequencies according to the binary input.



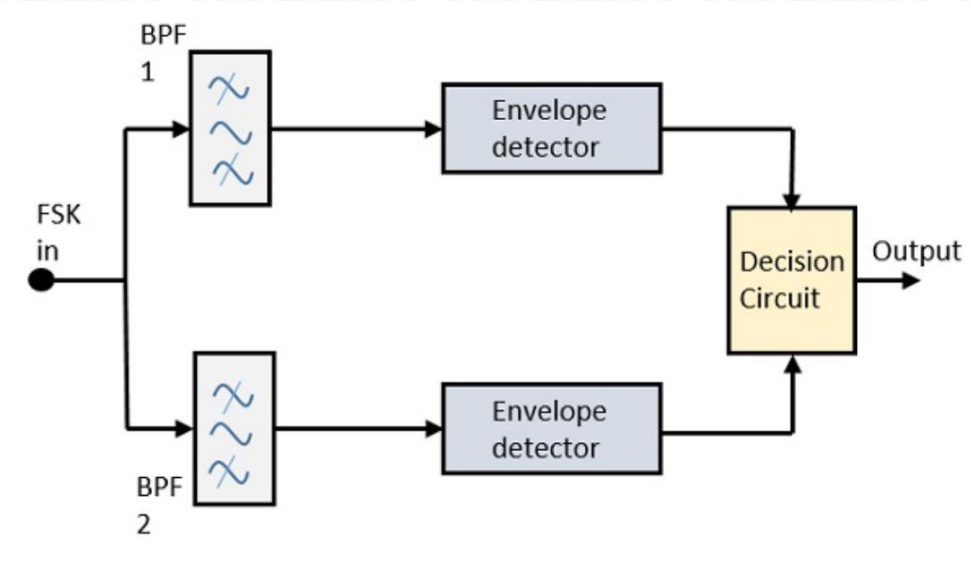
FSK Demodulator

- Asynchronous FSK Detector
- Synchronous FSK Detector

  The synchronous detector is a coherent one, while asynchronous detector is a non-coherent one.

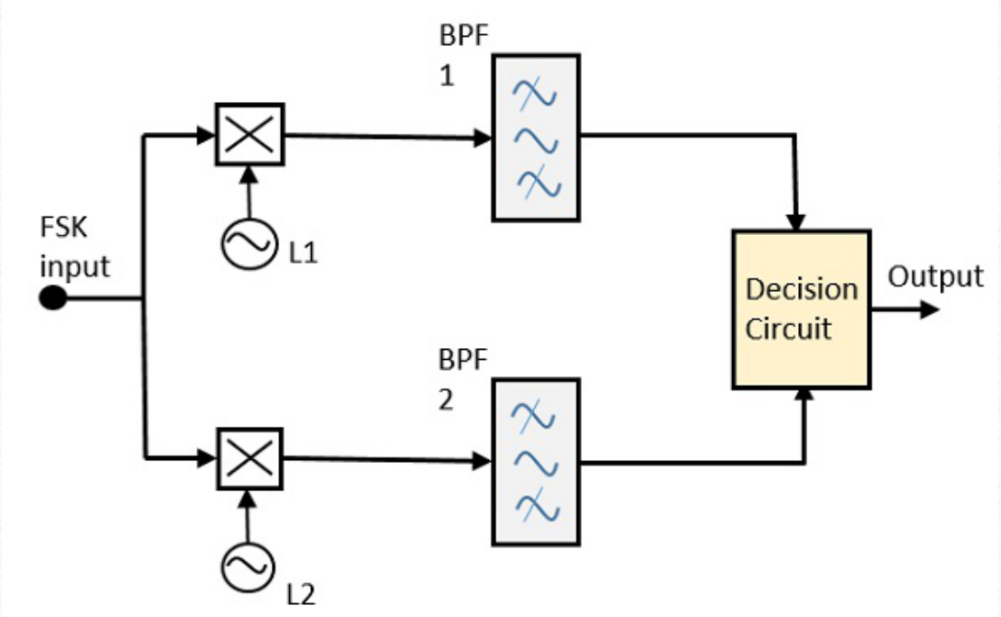
Asynchronous FSK Detector

- The FSK signal is passed through the two Band Pass Filters BPFs , tuned to **Space** and **Mark** frequencies. The output from these two BPFs look like ASK signal, which is given to the envelope detector. The signal in each envelope detector is modulated asynchronously.
- The decision circuit chooses which output is more likely and selects it from any one of the envelope detectors. It also re-shapes the waveform to a rectangular one.



Synchronous FSK Detector

- The FSK signal input is given to the two mixers with local oscillator circuits. These two are connected to two band pass filters. These combinations act as demodulators and the decision circuit chooses which output is more likely and selects it from any one of the detectors. The two signals have a minimum frequency separation.



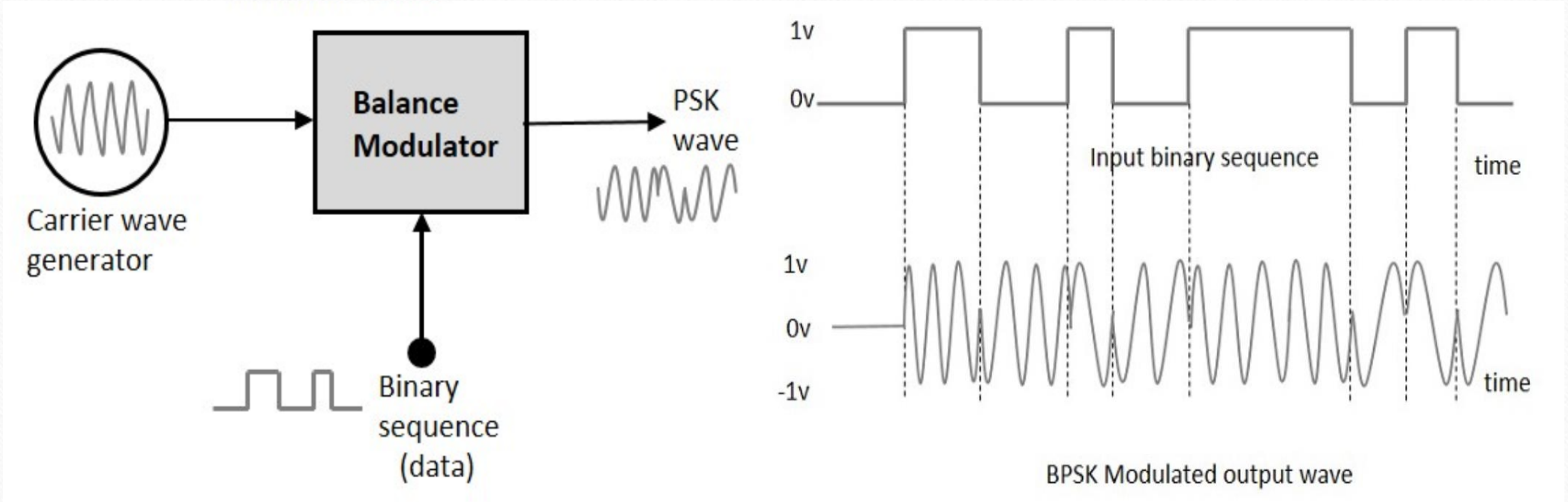
Phase Shift Keying PSK

- PSK technique is widely used for wireless LANs, bio-metric, contactless operations, along with RFID and Bluetooth communications.
- PSK is of two types, depending upon the phases the signal gets shifted:

  Binary Phase Shift Keying == BPSK == 2-phase PSK (0 ,180)

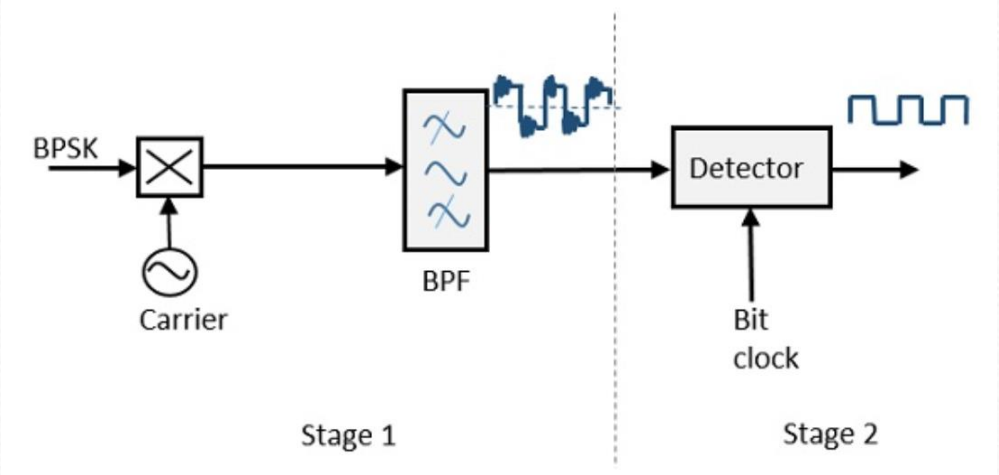
  Quadrature Phase Shift Keying == QPSK == (0, 90, 180, 270)
- PSK can be done by eight or sixteen values also, depending upon the requirement.

BPSK Modulator



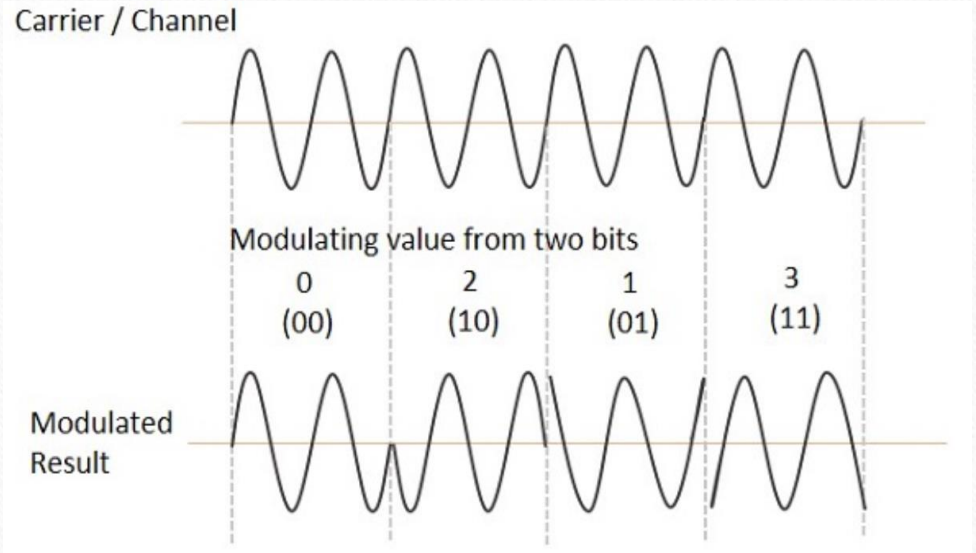
BPSK Demodulator

- By recovering the band-limited message signal, with the help of the mixer circuit and the band pass filter, the first stage of demodulation gets completed. The base band signal which is band limited is obtained and this signal is used to regenerate the binary message bit stream.
- In the next stage of demodulation, the bit clock rate is needed at the detector circuit to produce the original binary message signal. If the bit rate is a sub-multiple of the carrier frequency, then the bit clock regeneration is simplified. To make the circuit easily understandable, a decision-making circuit may also be inserted at the 2nd stage of detection.



Quadrature Phase Shift Keying QPSK

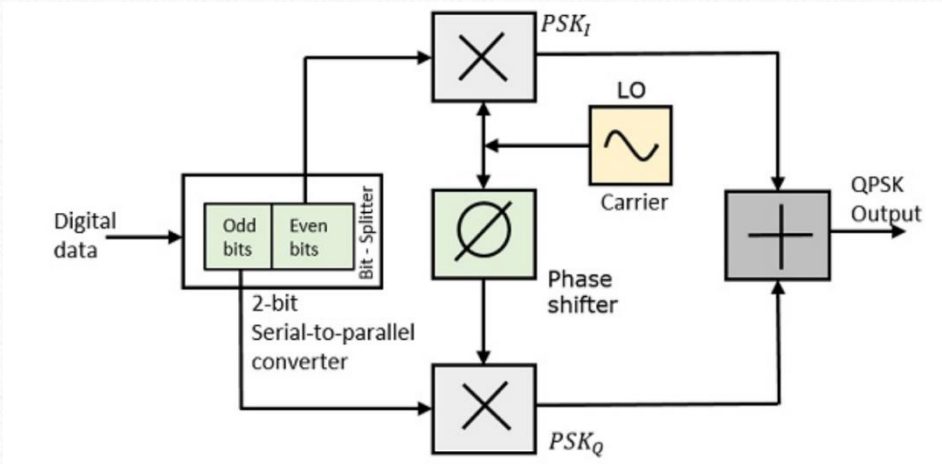
- is a variation of BPSK, and it is also a Double Side Band Suppressed Carrier DSBSC modulation scheme, which sends two bits of digital information at a time, called as **bigits**.
- Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs. This decreases the data bit rate to half, which allows space for the other users.



QPSK Modulator

- The QPSK Modulator uses a bit-splitter, two multipliers with local oscillator, a 2-bit serial to parallel converter, and a summer circuit.

- At the modulator's input, the message signal's even bits (i.e., 2nd bit, 4th bit, 6th bit, etc.) and odd bits (i.e., 1st bit, 3rd bit, 5th bit, etc.) are separated by the bits splitter and are multiplied with the same carrier to generate odd BPSK (called as $\mathbf{PSK_I}$) and even BPSK (called as $\mathbf{PSK_Q}$). The $\mathbf{PSK_Q}$ signal is anyhow phase shifted by 90° before being modulated.



- The spectral efficiency is 2 bits/Hz, meaning twice the data rate can be achieved in the same bandwidth as BPSK.

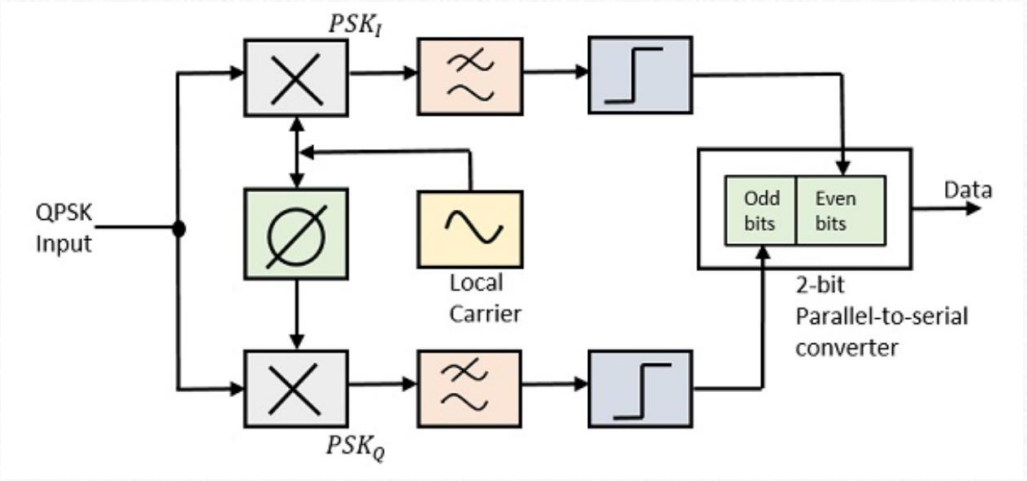
TABLE 1: CARRIER PHASE SHIFT FOR EACH PAIR OF BITS REPRESENTED

Bit pairs	Phase (degrees)
0 0	45
0 1	135
1 1	225
1 0	315

QPSK Demodulator

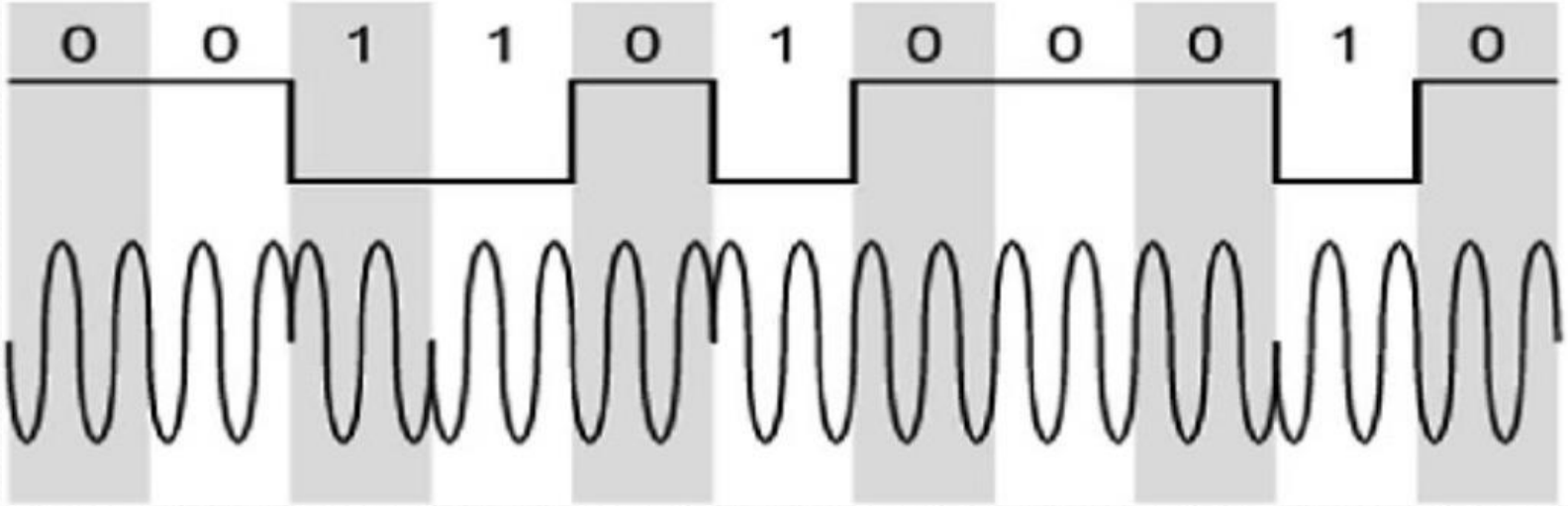
- The QPSK Demodulator uses two product demodulator circuits with local oscillator, two band pass filters, two integrator circuits, and a 2-bit parallel to serial converter. Following is the diagram for the same.

- The two product detectors at the input of demodulator simultaneously demodulate the two BPSK signals. The pair of bits are recovered here from the original data. These signals after processing, are passed to the parallel to serial converter.



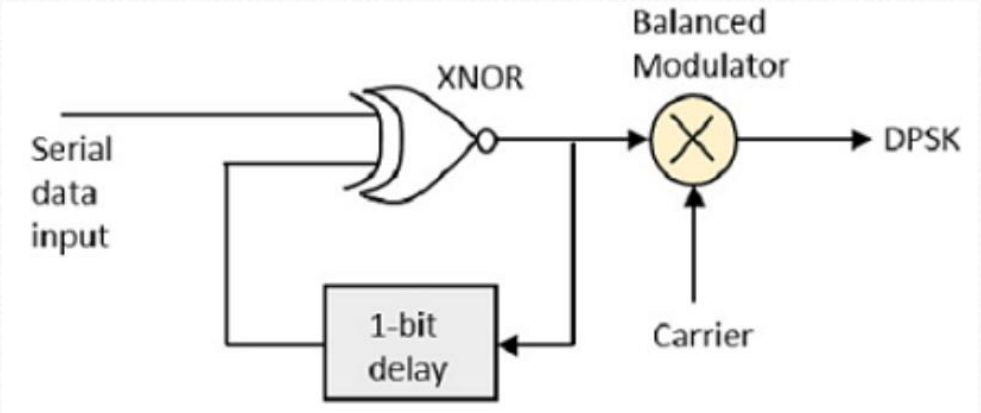
Differential Phase Shift Keying DPSK

- the phase of the modulated signal is shifted relative to the previous signal element. No reference signal is considered here. The signal phase follows the high or low state of the previous element. This DPSK technique doesn't need a reference oscillator.



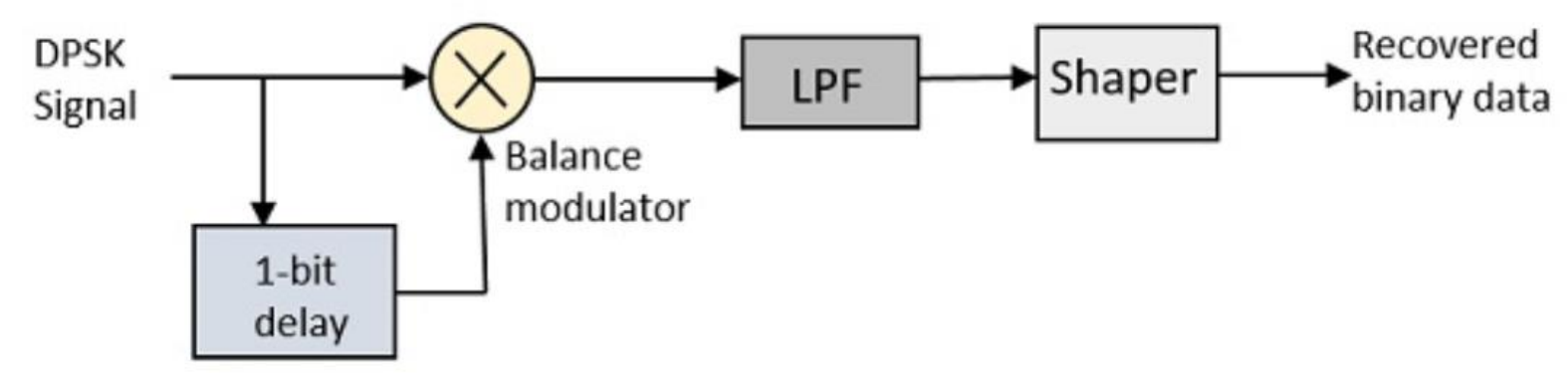
DPSK Modulator

- DPSK is a technique of BPSK, in which there is no reference phase signal. Here, the transmitted signal itself can be used as a reference signal. Following is the diagram of DPSK Modulator.
- DPSK encodes two distinct signals, i.e., the carrier and the modulating signal with 180° phase shift each. The serial data input is given to the XNOR gate and the output is again fed back to the other input through 1-bit delay. The output of the XNOR gate along with the carrier signal is given to the balance modulator, to produce the DPSK modulated signal.



DPSK Demodulator

- In DPSK demodulator, the phase of the reversed bit is compared with the phase of the previous bit. Following is the block diagram of DPSK demodulator.
- it is evident that the balance modulator is given the DPSK signal along with 1-bit delay input. That signal is made to confine to lower frequencies with the help of LPF. Then it is passed to a shaper circuit, which is a comparator or a Schmitt trigger circuit, to recover the original binary data as the output.



M-ary Encoding

- The word binary represents two bits. **M** represents a digit that corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables.
- This is the type of digital modulation technique used for data transmission in which instead of one bit, two or more bits are transmitted at a time. As a single signal is used for multiple bit transmission, the channel bandwidth is reduced.

M-ary Equation

- If a digital signal is given under four conditions, such as voltage levels, frequencies, phases, and amplitude, then **M = 4**.
- The number of bits necessary to produce a given number of conditions is expressed mathematically as $N = log_2^M$

  Where

  N is the number of bits necessary

  M is the number of conditions, levels, or combinations possible with **N** bits.

Types of M-ary Techniques

- In general, Multi-level M−ary modulation techniques are used in digital communications as the digital inputs with more than two modulation levels are allowed on the transmitter's input. Hence, these techniques are bandwidth efficient.

1. M-ary ASK
2. M-ary FSK
3. M-ary PSK

M-ary ASK

- This is called M-ary Amplitude Shift Keying M−ASK or M-ary Pulse Amplitude Modulation PAM .
- The **amplitude** of the carrier signal, takes on **M** different levels.

Representation of M-ary ASK

$$S_m(t) = A_m cos(2\pi f_c t) \quad A_m \epsilon (2m - 1 - M)\Delta, m = 1, 2 \ldots . M \quad and \quad 0 \leq t \leq T_s$$

Data Rate And Baud Rate

- The maximum theoretical data rate or channel capacity (C) in bits/s is a function of the channel bandwidth (B) in Hz and the signaltonoise ratio (SNR):

➢ $C = Blog_2^{(1+SNR)}$

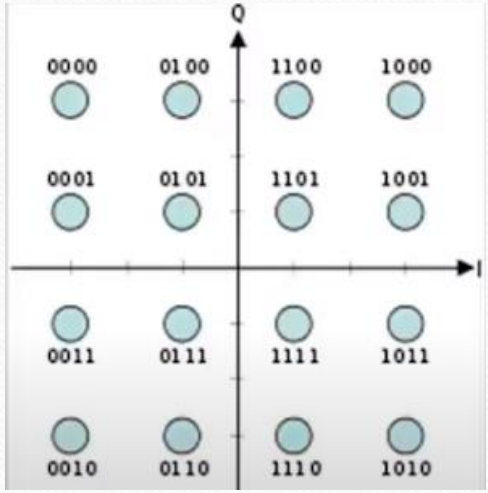
- This is called the ShannonHartley law. The maximum data rate is directly proportional to the bandwidth and logarithmically proportional the SNR. Noise greatly diminishes the data rate for a given bit error rate (BER)

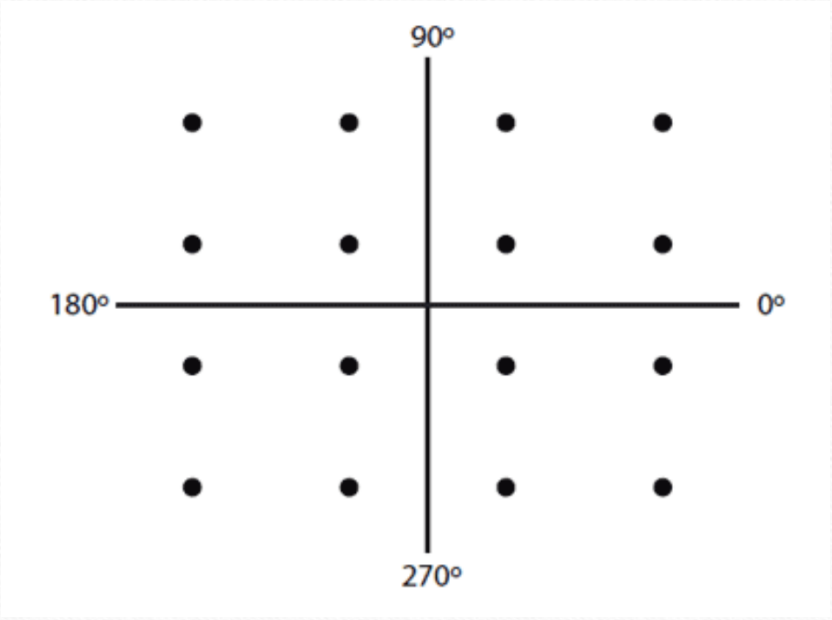
Quadrature Amplitude Modulation (QAM)

- The creation of symbols that are some combination of amplitude and phase can carry the concept of transmitting more bits per symbol further. This method is called quadrature amplitude modulation (QAM).
- For example, 8QAM uses four carrier phases plus two amplitude levels to transmit 3 bits per symbol. Other popular variations are 16QAM, 64QAM, and 256QAM, which transmit 4, 6, and 8 bits per symbol.

- While QAM is enormously efficient of spectrum, it is more difficult to demodulate in the presence of noise, which is mostly random amplitude variations. Linear power amplification is also required. QAM is very widely used in cable TV, WiFi wireless localarea networks (LANs), satellites, and cellular telephone systems to produce maximum data rate in limited bandwidths.

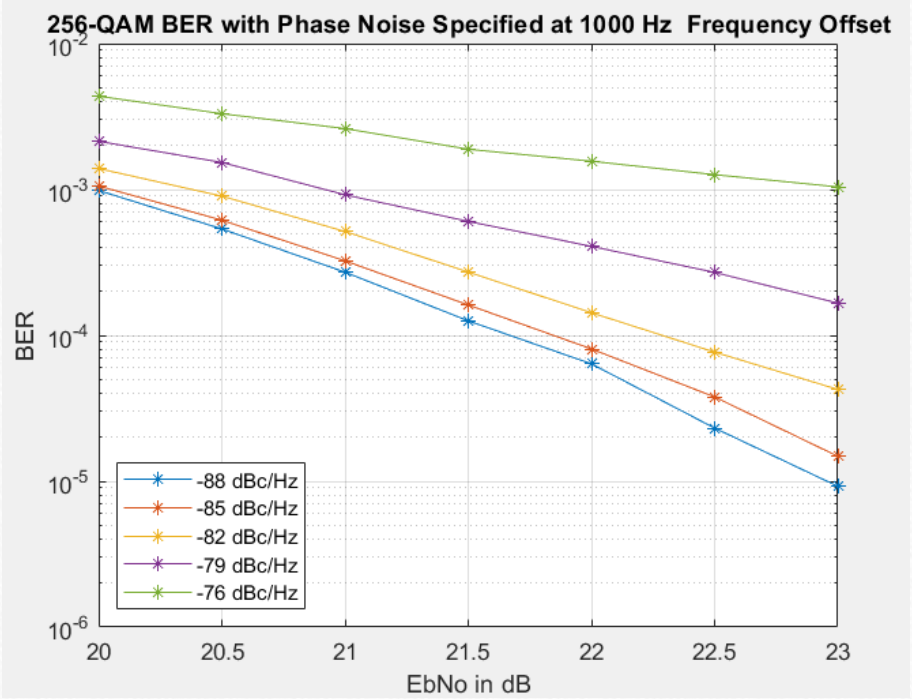
- 16QAM uses a mix of amplitudes and phases to achieve 4 bits/Hz. In this example, there are three amplitudes and 12 phase shifts.





BER Plot (Bit error rate)

- BER Plot showing the performance of 256-QAM with various levels of phase noise.
- E_b/N_o is classically defined as the ratio of Energy per Bit (Eb) to the Spectral Noise Density (No).



Amplitude Phase Shift Keying (APSK)

- Amplitude phase shift keying (APSK), a variation of both MPSK and QAM, was created in response to the need for an improved QAM. Higher levels of QAM such as 16QAM and above have many different amplitude levels as well as phase shifts. These amplitude levels are more susceptible to noise.
- APSK uses fewer amplitude levels. It essentially arranges the symbols into two or more concentric rings with a constant phase offset θ. For example, 16APSK uses a doublering PSK format. This is called 412 16APSK with four symbols in the center ring and 12 in the outer ring.

- Two close amplitude levels allow the amplifier to operate closer to the nonlinear region, improving efficiency as well as power output. APSK is used primarily in satellites since it is a good fit with the popular traveling wave tube (TWT) PAs.

- 16APSK uses two amplitude levels, A1 and A2, plus 16 different phase positions with an offset of θ. This technique is widely used in satellites.