Amir Taherin

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"We are on the cusp of another Golden Age." - Hennessy and Patterson

Education

Ph.D.

2020–Present **Computer Engineering**, *Northeastern University*, MA, USA.
Department of Electrical and Computer Engineering
– NUCAR Lab

Advisor Prof. David Kaeli

Co-advisor Prof. Yanzhi Wang

Course Works

- Advanced Computer Architecture
- High Performance Computing
- Introduction to Machine Learning and Pattern Recognition
- Simulation and Performance Evaluation

Events

- IBM Global Summer School 2021: **Quantum Machine Learning**
- Google Systems Innovation Summit 2021

M.Sc.

2018–2020 **Computer Science**, *University of Rochester*, NY, USA.
Department of Computer Science
– Computer Systems Group

Course Works

- Operating Systems
- Mobile Systems Architecture
- Introduction to Artificial Intelligence
- Parallel and Distributed Computing
- Computer's Models and Limitations
- Data Mining

M.Sc.

2014–2016 **Computer Systems Architecture**, *Sharif University of Technology*, Tehran, Iran.
Department of Computer Engineering
– Computer Architecture Group
– Embedded Systems Research Laboratory (ESRLab)

Master's Thesis

Title **"Energy Management in Fault-Tolerant Mixed-Criticality Systems"**

Advisor Prof. Alireza Ejlali

Course Works

- Advanced Computer Architecture
- Advanced VLSI Design
- Embedded Systems Design
- Low Power Digital Systems Design
- System on Chip Design
- Fault-Tolerant Systems Design

- Advanced Design of Dependable Systems

B.Sc.

2006–2011 **Computer Engineering – Hardware Major**, *K. N. Toosi University of Technology*, Tehran, Iran.
Department of Computer Engineering
– Computer Hardware Group

Final Project

Title **"Survey on VoIP Vulnerabilities, Threats and Countermeasures in order to Optimize Countermeasures Against a Well Known Threat"**

Selected Course Works

- Computer Architecture
- Digital Design
- Linear Control Systems
- Data Transmission
- Microprocessor
- Operating Systems
- Internet Engineering
- Multimedia
- VLSI Design
- Digital Electronics
- Signals and Systems
- Data Structure and Algorithm
- Computer Networks
- Voice over Internet Protocol
- Artificial Intelligence
- Project Management

Research Interests

- Quantum Computing
- Computer Architecture
- Mobile Systems Architecture
- System on Chip (SoC) Architecture
- Cyber-Physical and Mixed-Criticality Systems
- Cloud Computing
- Real-Time Systems
- Low Power and Energy Efficient Digital Systems
- Fault Tolerance and Design-for-Reliability
- Dependability Evaluation and Reliability Assessment
- Hardware Design and Synthesis
- VLSI and Electronic Circuits

Publications

Journal Papers:

TSUSC-2018 **"Reliability-Aware Energy Management in Mixed-Criticality Systems"**, *Amir Taherin, Mohammad Salehi, Alireza Ejlali, IEEE Transactions on Sustainable Computing*, vol. 3, no. 3, pp. 195-208, 2018.

Conference Papers:

DSN-2021 **"Examining Failures and Repairs on Supercomputers with Multi-GPU Compute Nodes."**, *Amir Taherin, Tirthak Patel, Giorgis Georgakoudis, Ignacio Laguna, and Devesh Tiwari*, In The 51st Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN '20)., Taipei, Taiwan.

FPGA-2020 **"Energy-Efficient 360-Degree Video Rendering on FPGA via Algorithm-Architecture Co-Design."**, *Qiuyue Sun, Amir Taherin, Yawo Siatitse, and Yuhao Zhu*, In The 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '20). Association for Computing Machinery, New York, NY, USA.

RTEST-2015 **"Stretch: Exploiting Service Level Degradation for Energy Management in Mixed-Criticality Systems"**, *Amir Taherin, Mohammad Salehi, Alireza Ejlali*, The CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST), Tehran, Iran.

Technical Skills

Quantum Computing: IBM Qiskit

Operating Systems: Windows, Linux, Android

Programming Languages	C/C++ (*OpenMP, MPI, pthread*), Python, TCL/OTcl, StateFlow, MATLAB, Assembly languages of X86, and ARM
HDLs	Verilog
CAD Tools	Synopsys (*Design Compiler, HSPICE, PrimePower, Platform Architect*), Cadence (*Virtuoso, SoC Encounter*), Mentor Graphics (*ModelSim*), Xilinx (*ISE Design Suite, Vivado HLS, SDSoC*), MATLAB, Simulink
Dev. Boards	Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit
ML tools	Weka
CMSs	Joomla, Drupal, Plone, OwnCloud
Typesetting	LaTeX, TeX, Microsoft Office

Teaching Experience

Spring 2020 **Parallel and Distributed Computing**, *Teacher Assistant*, University of Rochester, Rochester, NY.
Under Supervision of Prof. Sandhya Dwarkadas

Fall 2019 **Programming Languages Design and Implementation**, *Teacher Assistant*, University of Rochester, Rochester, NY.
Under Supervision of Prof. Michael L. Scott

Spring 2019 **Computer Organization**, *Teacher Assistant*, University of Rochester, Rochester, NY.
Under Supervision of Prof. Yuhao Zhu

Spring 2016 **Embedded Systems Design**, *Teacher Assistant*, Sharif University of Technology, Tehran, Iran.
Under Supervision of Prof. Alireza Ejlali

Spring 2016 **Logic Design**, *Teacher Assistant*, Sharif University of Technology, Tehran, Iran.
Under Supervision of Prof. Shaahin Hessabi

Spring 2015 **Advanced Logic Design**, *Teacher Assistant*, Sharif University of Technology, Tehran, Iran.
Under Supervision of Prof. Alireza Ejlali

Honors and Awards

2015 – 2016 **National Elites Foundation Scholarship** from Presidency of Islamic Republic of Iran. Tehran, Iran.

2016 **Ranked 3rd** in cumulative GPA among all students of computer architecture (41 students), Sharif University of Technology, Tehran, Iran.

2014 **Rank Obtained 21** in the Nation-wide University Entrance Exam of Graduate Studies in Computer Science and Engineering among 8,998 Participants. Tehran, Iran.

2006 **Rank Obtained 1525** in the Nation-wide University Entrance Exam in Undergraduate Studies, Physics and Mathematics Track, among 1,345,000 Participants. Tehran, Iran.

Academic Services

TETC-2018 **Reviewer**, *IEEE Transactions on Emerging Topics in Computing.*

RTEST-2017 **Reviewer**, *The CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST).*

RTEST-2015 **Reviewer**, *The CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST).*

Standard Test Scores

TOEFL **115/120**: Reading: 28/30, Listening: 29/30, Speaking: 29/30, Writing: 29/30

Selected Projects

2019 **Implementing and Testing Basic and Advanced Spin Locks for Shared Memory Systems**, *Locks: C++ mutex, naive TAS lock, TAS lock with well-tuned exponential backoff, naive ticket lock, ticket lock with well-tuned proportional backoff, MCS lock, K42 MCS lock, CLH lock, 'K42' CLH lock , Developed in C++*, University of Rochester, NY, USA.
Parallel and Distributed Computing Course Project

2019 **Implementing Drinking Philosophers Problem for Shared Memory Systems**, *Based on TOPLAS 89, Developed in C++*, University of Rochester, NY, USA.
Parallel and Distributed Computing Course Project

2019 **Frequent Item-set Mining on International Symposium on Computer Architecture (ISCA)**, *Data Mining on: Title, Abstract, References, Citations, etc. , Developed in Python*, University of Rochester, NY, USA.
Data Mining Course Project

2018 **Estimating the Baseline of Power and Energy Consumption in Mobile Computing Accelerators**, *Using LIKWID Performance Monitoring and Benchmarking Suite*, University of Rochester, NY, USA.
Problem Seminar Course Project

2018 **Implementing Basic Learning Algorithms**, *Decision Tree, Multi-layer feed-forward NN, Developed in Python*, University of Rochester, NY, USA.
Artificial Intelligence Course Project

2018 **Implementing a Game Engine to Play Super and Qubic TTT**, *Based on Depth-limited H-MINMAX and Alpha-Beta Pruning Algorithms, Developed in Python*, University of Rochester, NY, USA.
Artificial Intelligence Course Project

2018 **Survey on Scheduling of Fast Computational Accelerators**, *Based on GPU architecture*, University of Rochester, NY, USA.
Operating Systems Course Project

2018 **Implementing Kernel-Level Counter-based Clock Page Replacement Algorithm for Memory Management**, *Applied both to Active and Inactive Lists, Developed in C*, University of Rochester, NY, USA.
Operating Systems Course Project

2018 **Implementing Kernel-Level Synchronization Primitives**, *Using RB-Tree from Linux kernel data structures and Spinlocks, Developed in C*, University of Rochester, NY, USA.
Operating Systems Course Project

2016 **Design and Implementation of Low-Power On-Chip Interconnect in 90nm CMOS Technology**, *Based on Bus-Inverting and Reduced Voltage Swing Techniques, Developed in HSPICE*, Sharif University of Technology, Tehran, Iran.
Low Power Digital Systems Design Course Project

2016 **Layout Design of Basic Gates in 90nm CMOS Technology**, *Families: Static CMOS, Pseudo-nMOS, DCVSL, Dual-Rail Domino, Developed in Virtuoso Layout Editor*, Sharif University of Technology, Tehran, Iran.
Advanced VLSI Course Project

2015 **Reliability Model of TMR Configured Multicore Processors Based on DVFS and AVF**, *Developed in MATLAB*, Sharif University of Technology, Tehran, Iran.
Advanced Design of Dependable Systems

2015 **Designing and Implementing Incubator Temperature Control**, *Designed and implemented in two different MoC's, (1) Differential Equations (PI and PID Controllers) with MATLAB/Simulink, and (2) Automata-Based Programming (CFSM) with MATLAB/Simulink StateFlow*, Sharif University of Technology, Tehran, Iran.
Embedded Systems Design Course Project

2015 **Implementing ER-EDF and EDF-VD Mixed-Criticality Scheduling Algorithms**, *ER-EDF (DATE 2013) and EDF-VD (ECRTS 2012), Developed in MATLAB*, Sharif University of Technology, Tehran, Iran.
Embedded Systems Design Course Project

2015 **Designing and Implementing a Complex Multiplication ASIC (Hard) IP-Core in 0.18μm CMOS Technology**, *A complete ASIC design flow written in Verilog, synthesized in Synopsys Design Vision, placed, routed and RC-extracted in SoC Encounter, and verified by post layout simulation in HSIM*, Sharif University of Technology, Tehran, Iran.
System on Chip Design Course Project

2015 **Designing and Implementing a Complex Multiplication IP-Core on FPGA**, *Developed in Xilinx ISE Design Suite for Spartan-6, Spartan-4 and Virtex-4, Virtex-5, Virtex-6, Virtex-7 families*, Sharif University of Technology, Tehran, Iran.
System on Chip Design Course Project

2014 **Survey on Limitations and Challenges of Using Multicore Processors in Safety-Critical Systems**, *In Context of Mixed-Criticality Systems*, Sharif University of Technology, Tehran, Iran.
Fault Tolerant Systems Design Course Project

2014 **Reliability Evaluation and Assessment**, *Systems: TMR, 5MR, TMR with Error Recovery, RAID5, RAID6, Standby-Sparing, by Relex tools*, Sharif University of Technology, Tehran, Iran.
Fault Tolerant Systems Design Course Project

2014 **Designing and Implementing a Cache Prefetcher**, *Algorithms: Next-Line Prefetcher, Stride Prefetcher, Temporal Streaming of Shared Memory (TMS) Prefetcher (ISCA 2005), Developed in C++*, Sharif University of Technology, Tehran, Iran.
Advanced Computer Architecture Course Project

2014 **Designing and Implementing a Cache Simulator**, *Replacement Policies: LRU, LFU, MRU, Pseudo LRU, Belady's optimal, and Shepherd Cache (MICRO 2007), Developed in C++*, Sharif University of Technology, Tehran, Iran.
Advanced Computer Architecture Course Project

2009 **Implementing a Multi-Threaded Web Server**, *Developed in C++*, K. N. Toosi University of Technology, Tehran, Iran.
Operating Systems Course Project

2008 **Implementing a Pipelined MIPS Processor**, *Developed in Quartus*, K. N. Toosi University of Technology, Tehran, Iran.
Computer Architecture Course Project

2007 **Designing and Implementing Chess Engine**, *A simple chess engine developed in C++*, K. N. Toosi University of Technology, Tehran, Iran.
Advanced Programming Course Project

Professional Positions

2020 – now **Graduate Research Assistant**, *GoodWill Laboratory*, Department of Electrical and Computer Engineering, Northeastern University, Boston, MA.

2018 – 2020 **Graduate Research and Teaching Assistant**, Department of Computer Science, University of Rochester, Rochester, NY.

2014 – 2017 **Graduate Research Assistant**, *Embedded Systems Research Laboratory (ESRLab)*, Department of Computer Engineering, Sharif University of Technology, Tehran, Iran.
Under Supervision of Prof. Alireza Ejlali

Languages

Persian Mother tongue

English Full professional proficiency *TOEFL iBT: 115/120*

References

Available on request.