DESIGNING LAYOUT FOR AN INVERTER

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AIM:

To design a layout for a CMOS inverter and enable DRC and LVS checks to ensure layout is error free.

TOOLS:

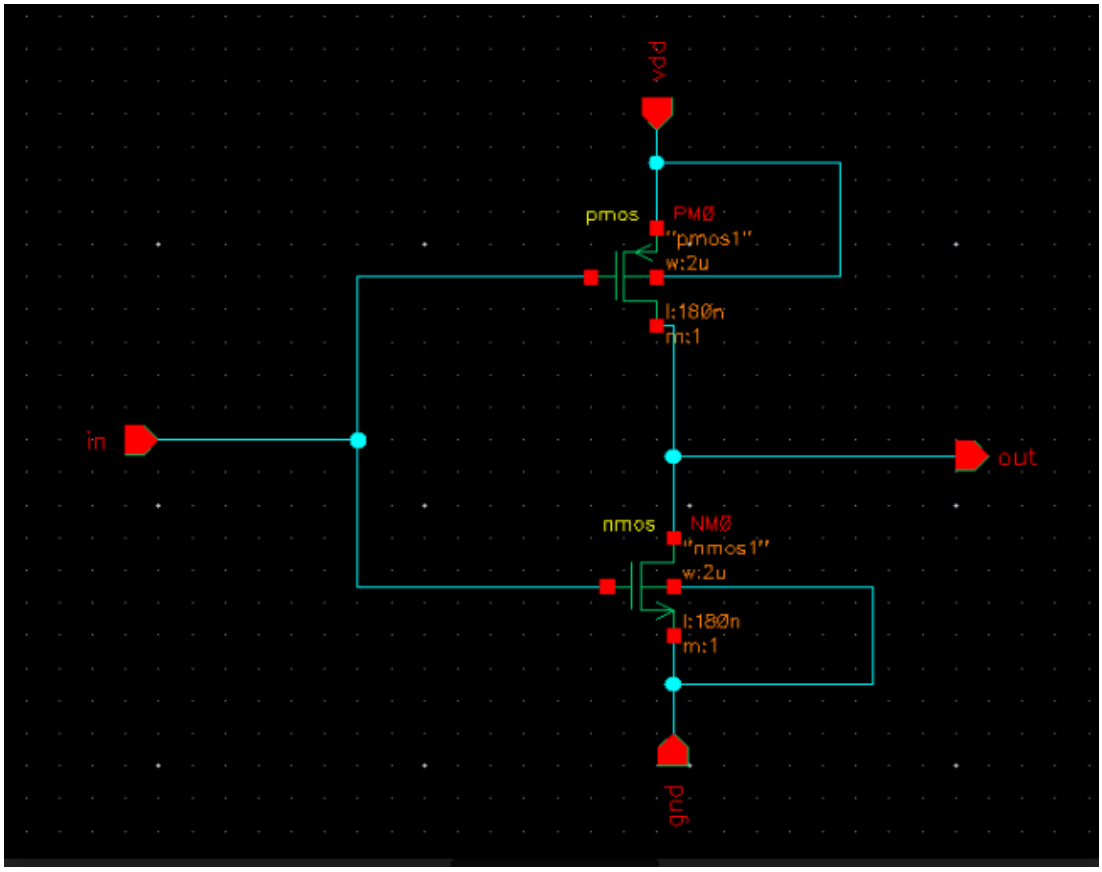
Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology library.

PROCEDURE:

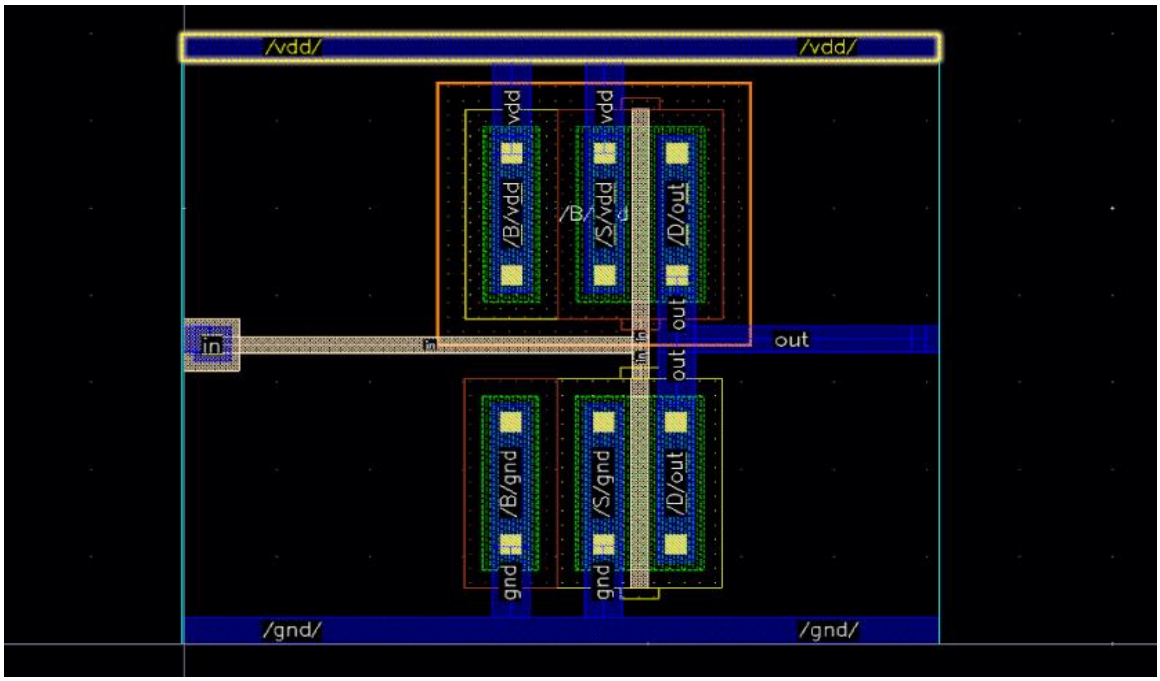
1. Create a layout of an inverter CMOS circuit schematic.
2. Give appropriate interconnections (signal and power routing).
3. Check for DRC errors and debug them.
4. Correct the LVS errors to make the layout error free.

SCREENSHOTS:

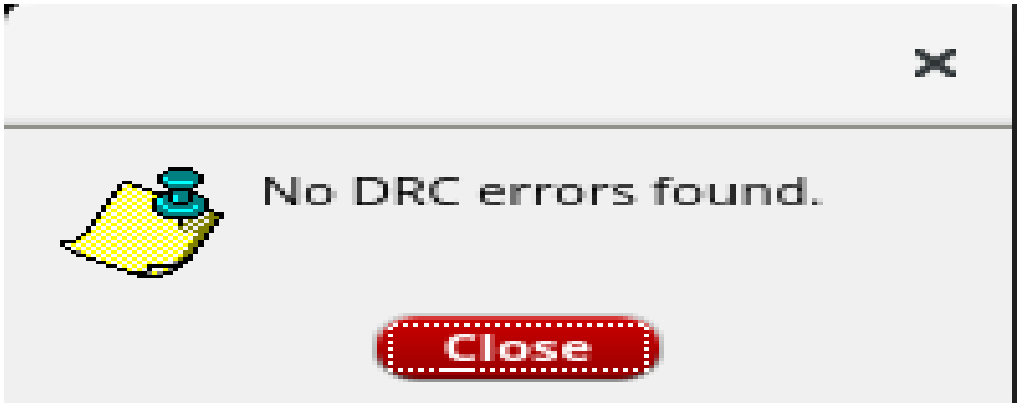
1. **INVERTER SCHEMATIC:**



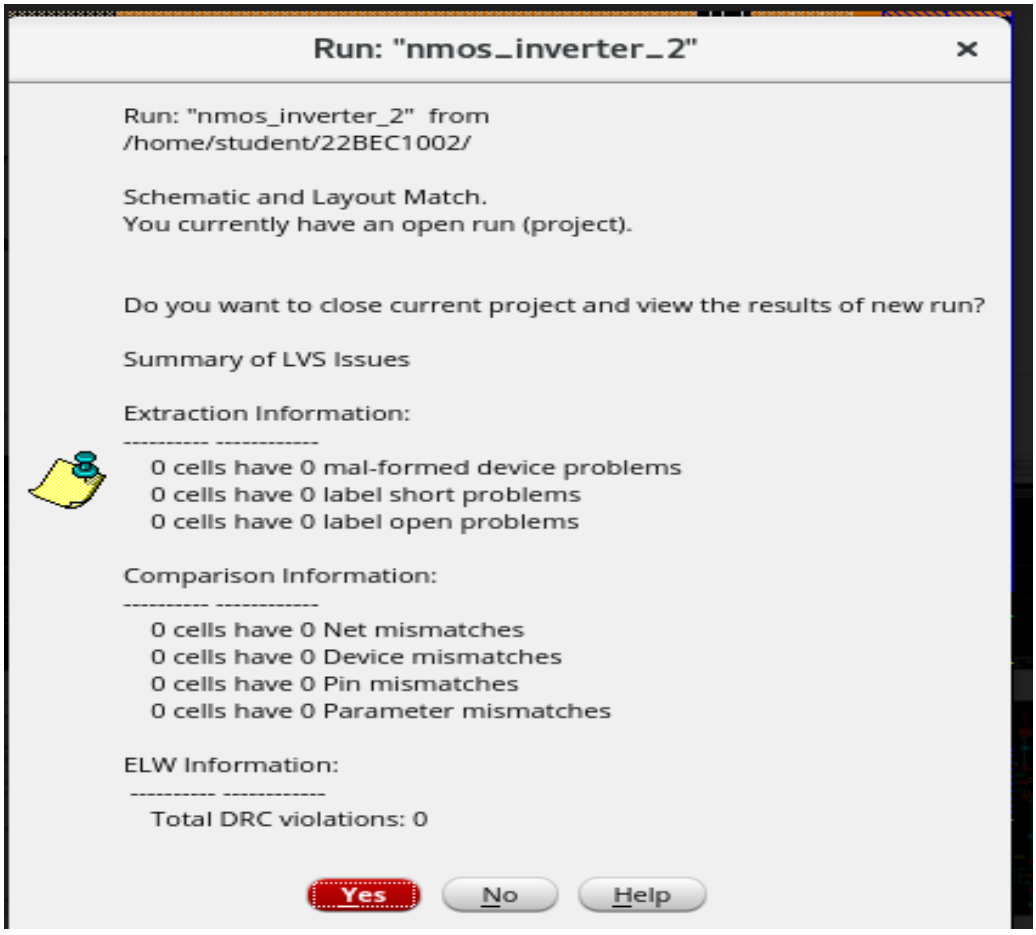
2. **LAYOUT OF A CMOS INVERTER WITH APPROPRIATE SIGNAL AND POWER ROUTING:**



3. ENSURING NO DRC ERRORS:



4. ENSURING NO LVS ERRORS:



INFERENCE:

1. The stick diagram is the intermediate between circuit and layout design.
2. DRC testing is used to check the spacing, width and overlapping.
3. LVS testing (Layout vs schematic) is used to correct interconnections which are left out or added extra.