

POWER AND DELAY CALCULATION FOR CMOS CIRCUITS:

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AIM:

To find delay and power for:

- a) Inverter circuit
- b) 2 input NAND gate.**

TOOLS:

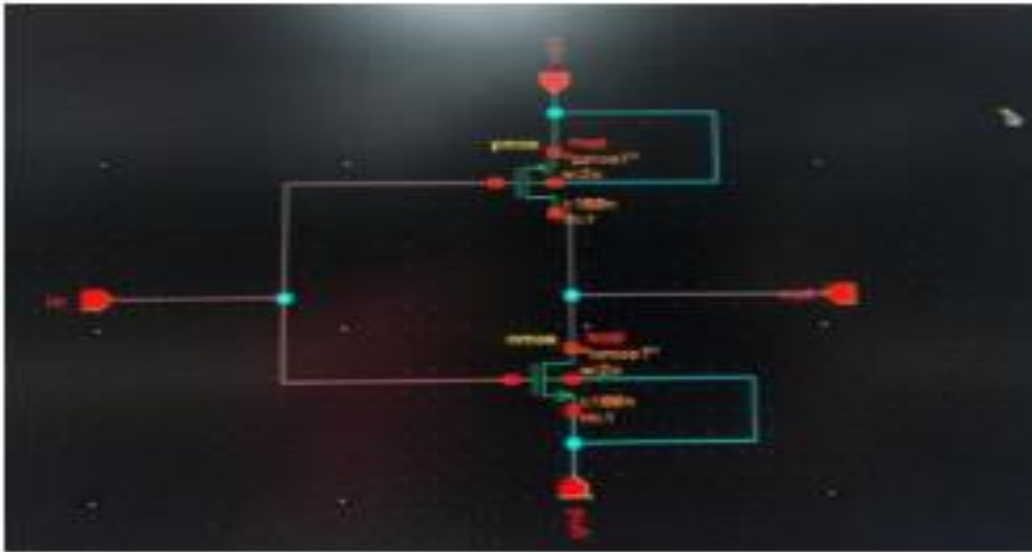
Linux operated computing system, Cadence® Virtuoso, gpdtk 180nm technology library.

PROCEDURE:

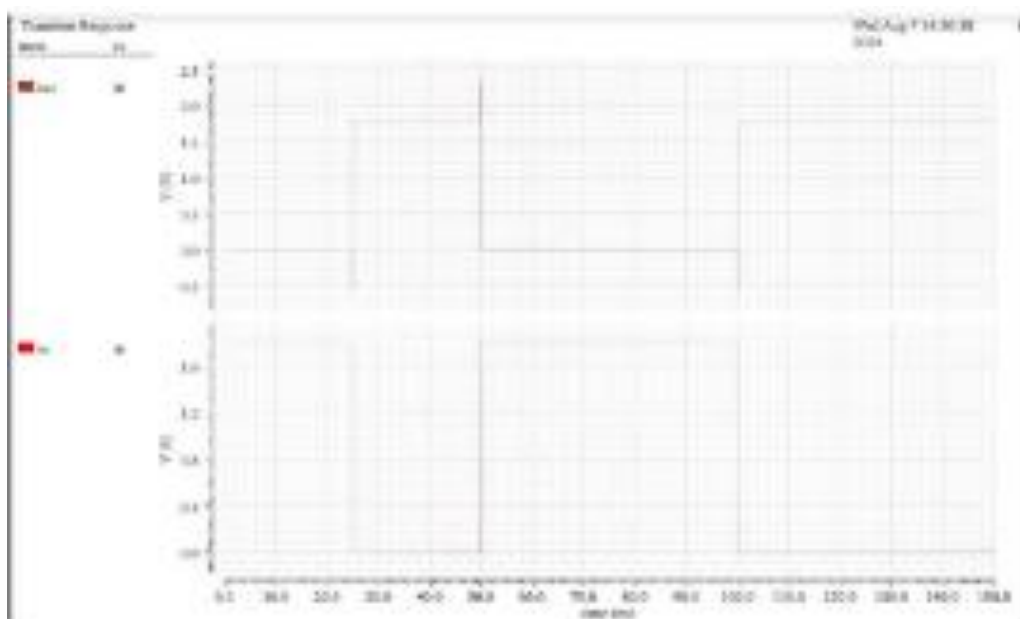
1. Design an inverter circuit and find the transient analysis.
2. Calculate the delay (rising and falling) using calculator.
3. Calculate the power from transient analysis.
4. For the 2 input, NAND gate, for both rising and falling, calculate the best and worst cases delay and the power.

SCREENSHOTS AND DELAY:

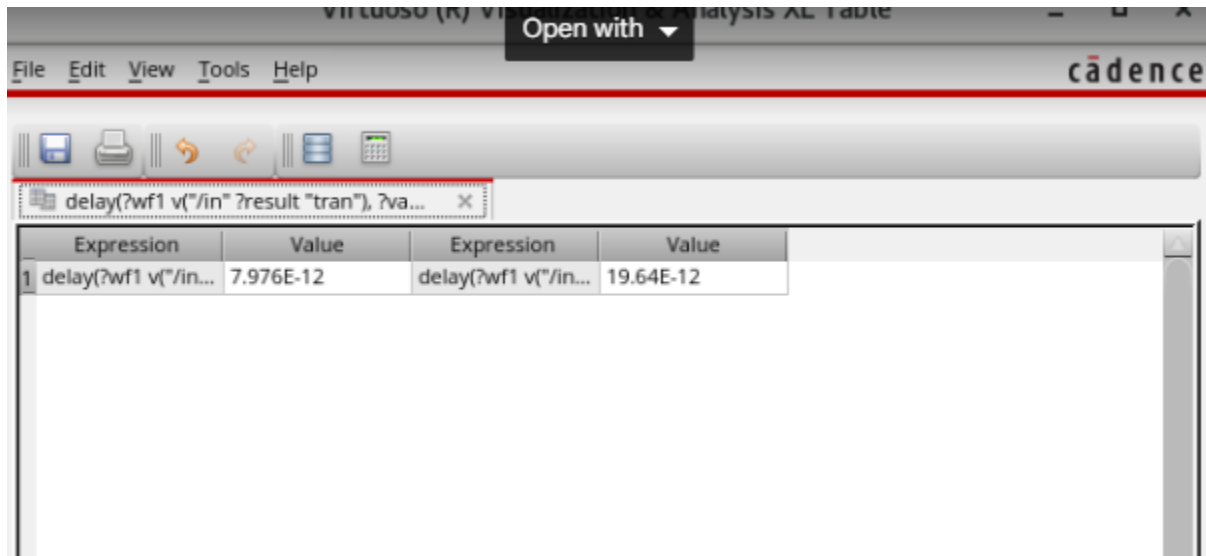
1. INVERTER CIRCUIT:



2. TRANSIENT ANALYSIS:



3. DELAY:



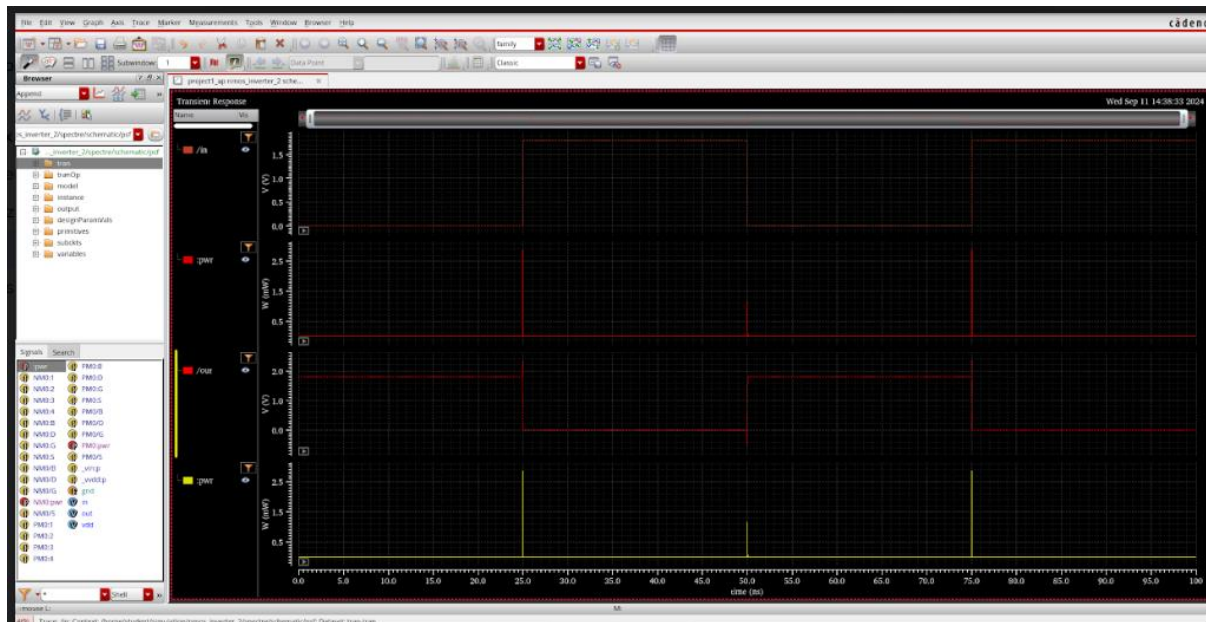
The screenshot shows the Cadence Virtuoso interface with a table of delay values. The table has four columns: Expression, Value, Expression, and Value. The first row contains the expression 'delay(?wf1 v("/in" ?result "tran"), ?va...' and the value '7.976E-12'. The second row contains the expression 'delay(?wf1 v("/in" ?result "tran"), ?va...' and the value '19.64E-12'.

Expression	Value	Expression	Value
1 delay(?wf1 v("/in" ?result "tran"), ?va...	7.976E-12	delay(?wf1 v("/in" ?result "tran"), ?va...	19.64E-12

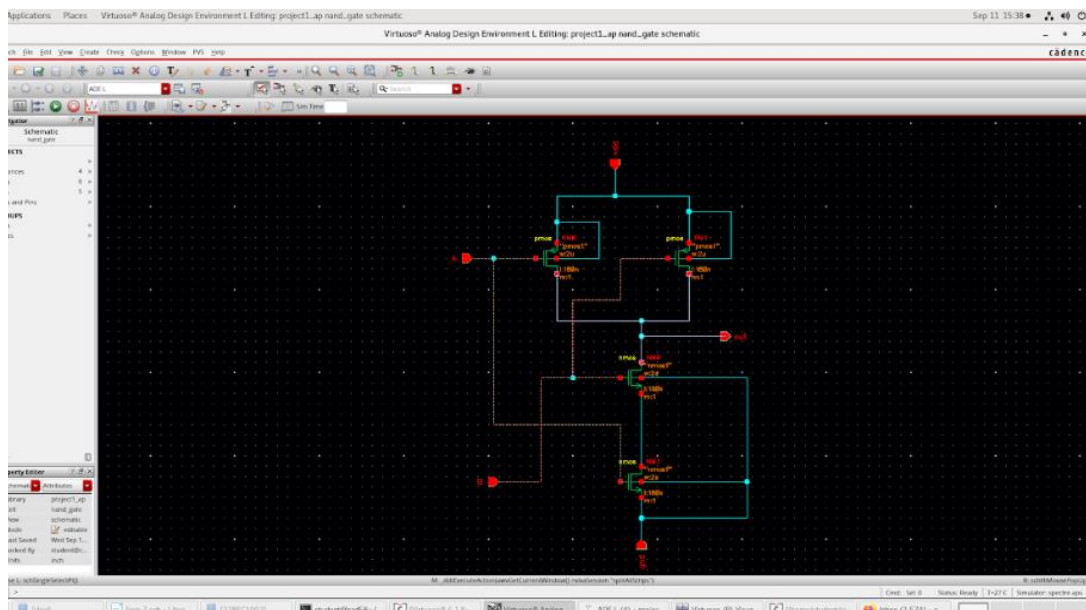
FALLING: 7.976ps

RISING: 19.64ps

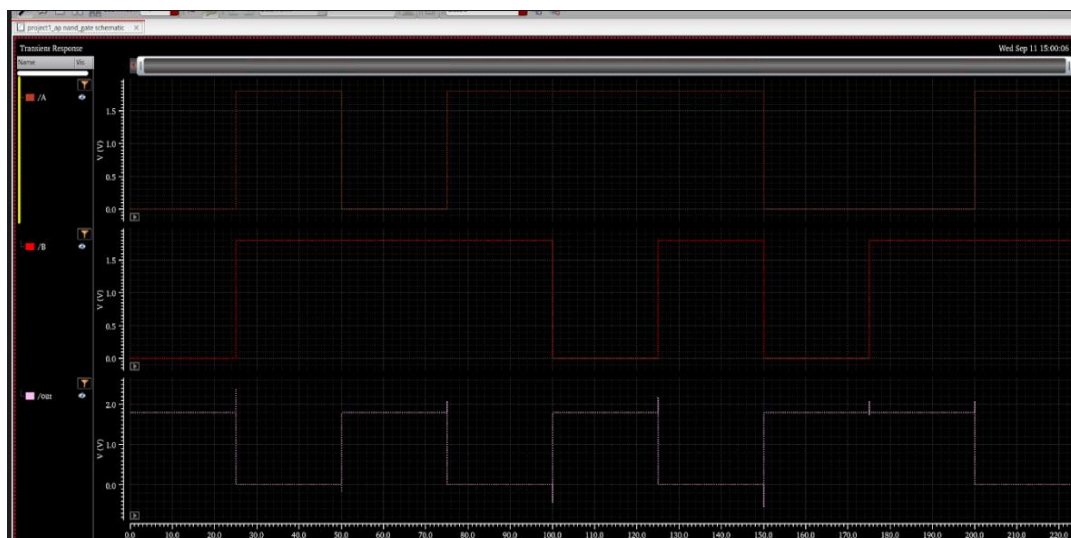
4. POWER:



5. NAND SCHEMATIC:



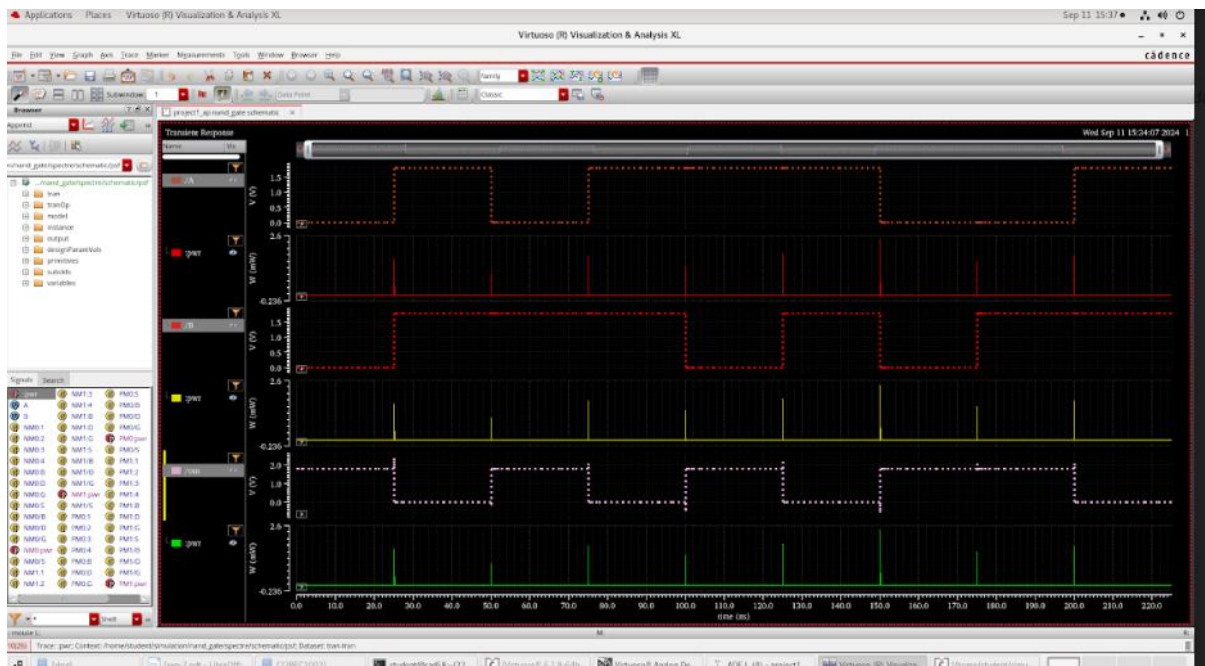
6. TRANSIENT ANALYSIS:



7. DELAY:

Pattern	Input	Output	Rise/fall	Delay(ps)
10	B(1f)	2r	rising	25.82(worst)
00	B(2f)	3r	rising	15.23(best)
11	A(3r)	1f	falling	21.5(worst)
11	A(1r)	4f	falling	21.10(best)

8. POWER:



INFERENCE:

1. Truth table is verified by giving different input values for the variables for the combinational circuit.
2. The transient analysis is performed to verify the CMOS circuit.
3. The delay and power for sum and carry is calculated for all values and best and worst cases delay are analysed.