STATIC CMOS CIRCUITS- COMBINATIONAL AND SR LATCH

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AIM:

To Construct static CMOS circuit diagrams for given expression of combinational circuit and SR Latch.

TOOLS:

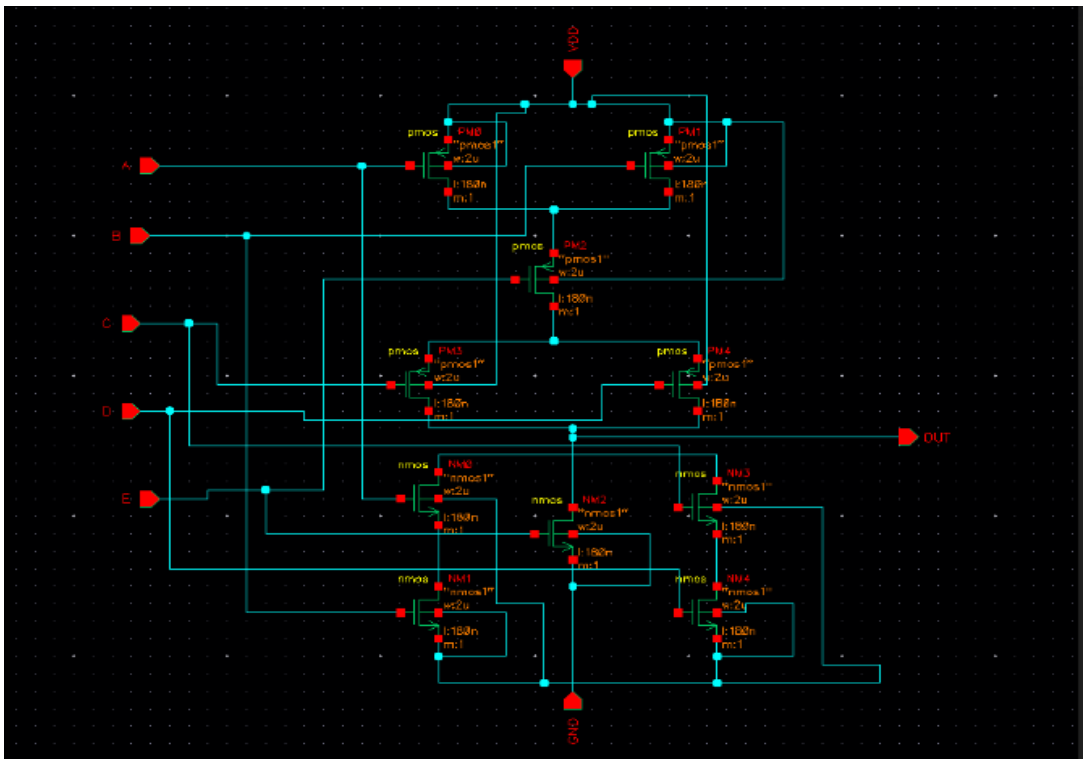
Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology library.

PROCEDURE:

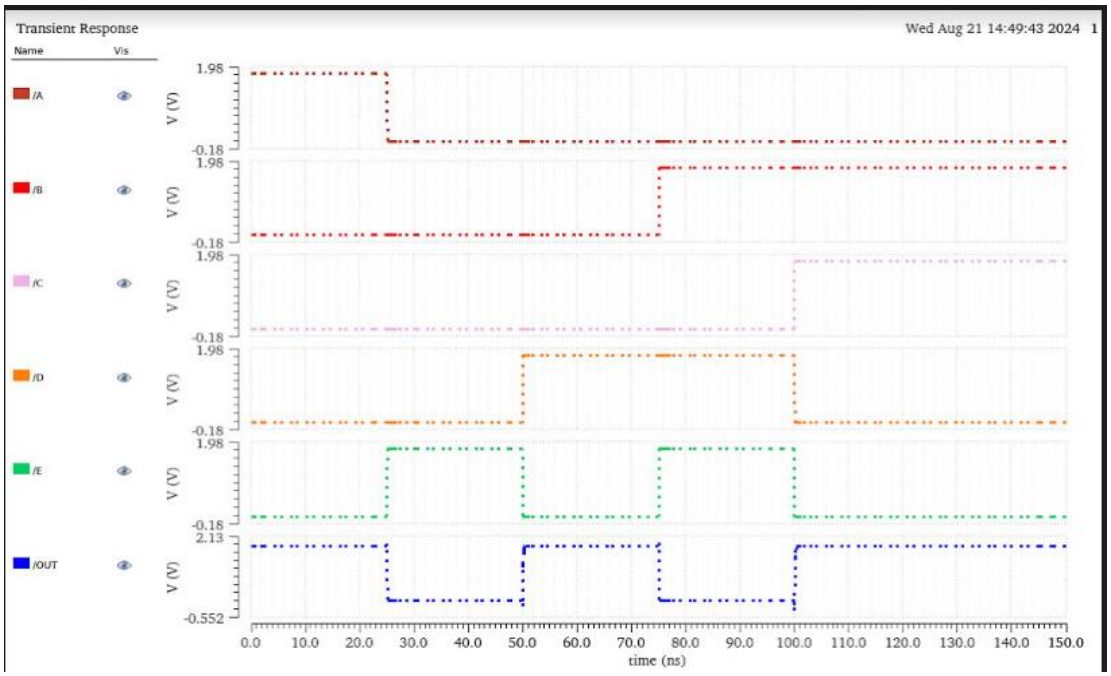
1. Consider the expression $F=\overline{AB+E+CD}$ combinational circuit.
2. Draw static CMOS diagram for the given expression using PMOS and NMOS.
3. Verify the truth table.
4. Also, draw SR Latch using NOR gates using CMOS.
5. Verify the truth table.

SCREENSHOTS:

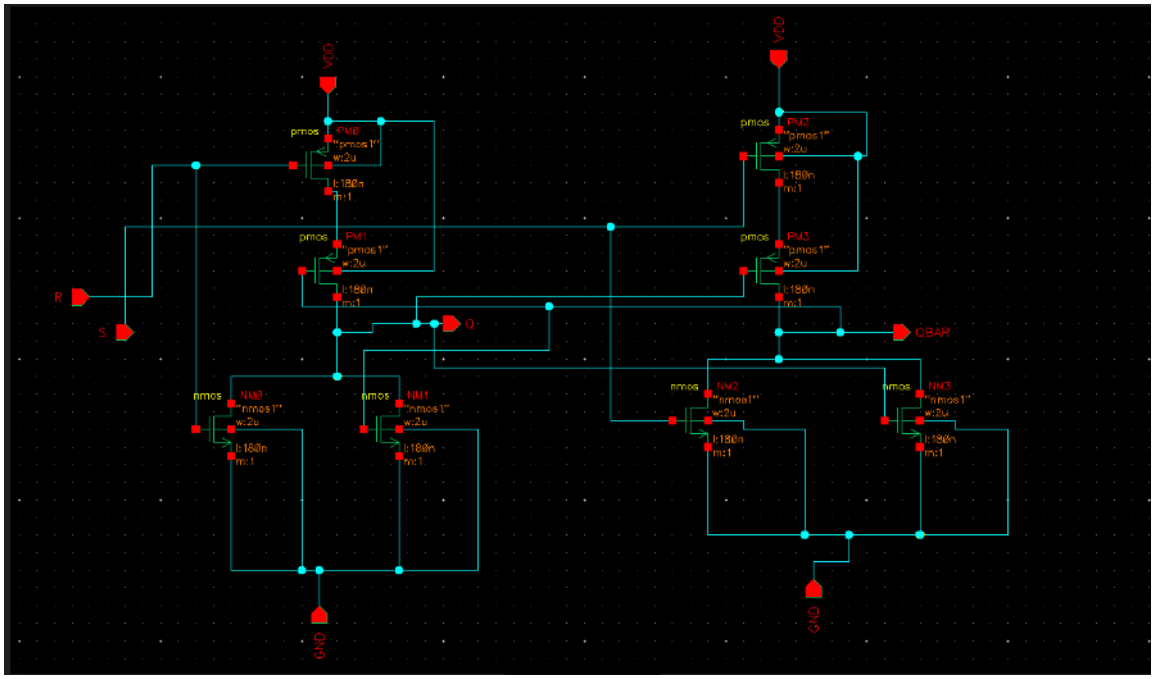
1. CMOS DIAGRAM FOR COMBINATIONAL CIRCUIT:



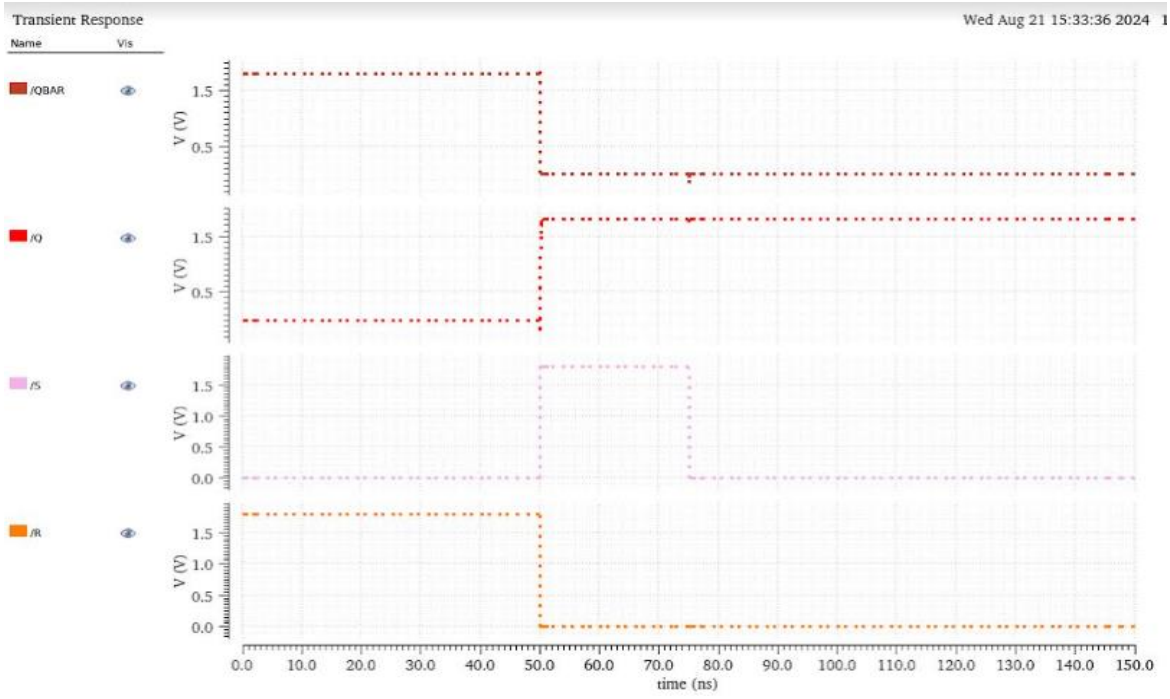
2. TRANSIENT ANALYSIS:



3. SR LATCH USING NOR GATE:



4. TRANSIENT ANALYSIS:



INFERENCE:

1. Truth table is verified by giving different input values for the variables for the combinational circuit.
2. The transient analysis is performed for SR Latch using NOR gates CMOS circuit.