

VLSI EXPERIMENT 1: NMOS, PMOS

CHARACTERISTICS

AMIRTHA PRASAD

22BEC1002

OBJECTIVE:

To analyze the V-I characteristics of NMOS and PMOS transistors.

TOOLS:

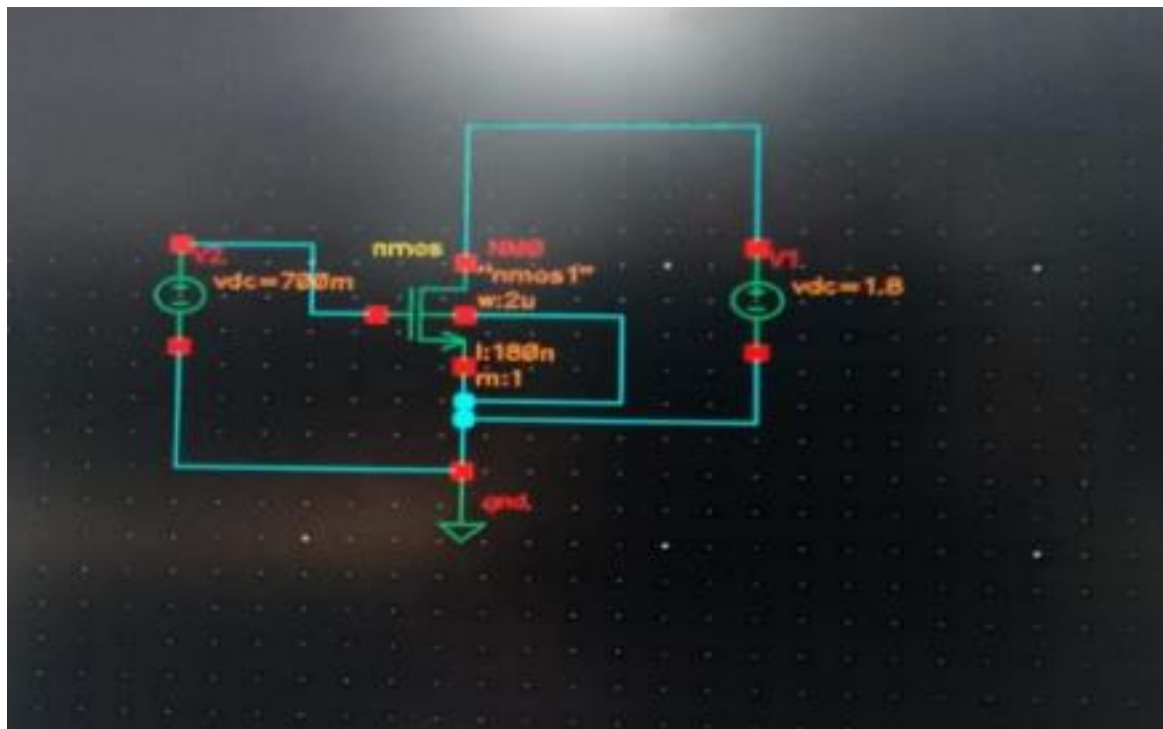
Linux operated computing system, Cadence® Virtuoso, gpdK 180nm technology library.

PROCEDURE FOR NMOS:

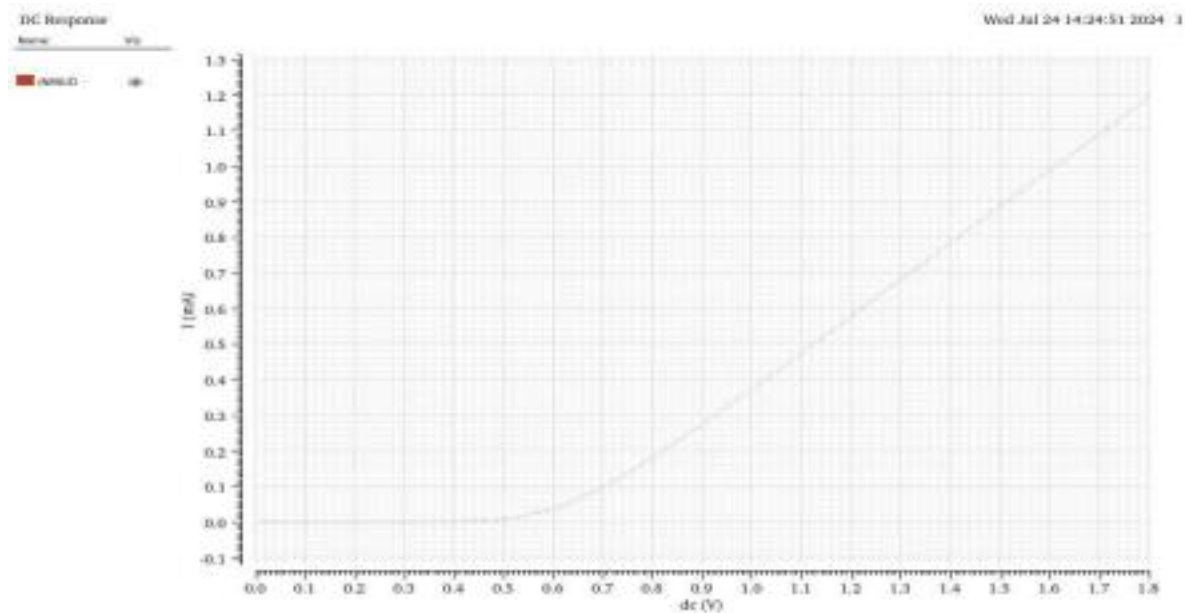
1. Create a schematic.
2. Configure DC Analysis with the input gate voltage V_{gs} as the component parameter and sweep range of 0 to 1.8V
 - a) Plot the drain current I_d .
3. Define the input gate voltage V_{GS} as a variable parameter "x"
 - a) Configure dc analysis for various drain source voltage V_{ds} by defining it as the component parameter and sweep range of 0 to 1.8V.
 - b) Plot the drain current I_d .
 - c) Perform the parametric analysis for various values of V_{gs} which is defined as "x".
4. Vary the width of the NMOS as "w" and plot input characteristics for 7 different potentials using parametric analysis.

SCREENSHOTS:

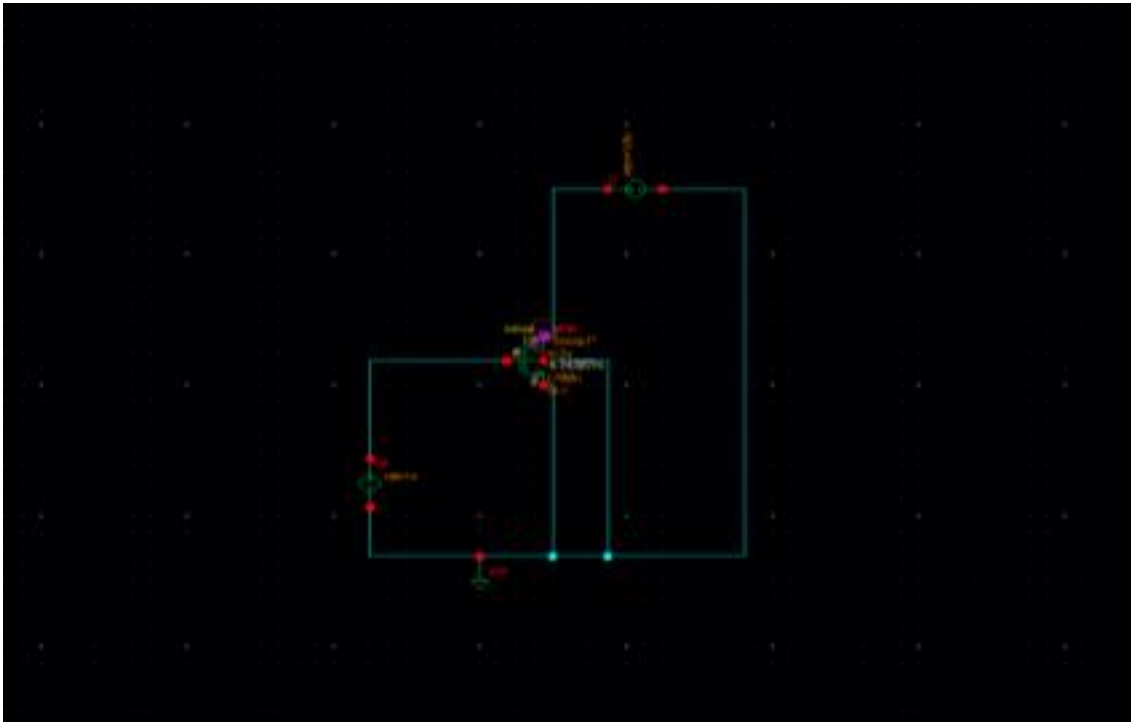
1. NMOS SCHEMATIC:



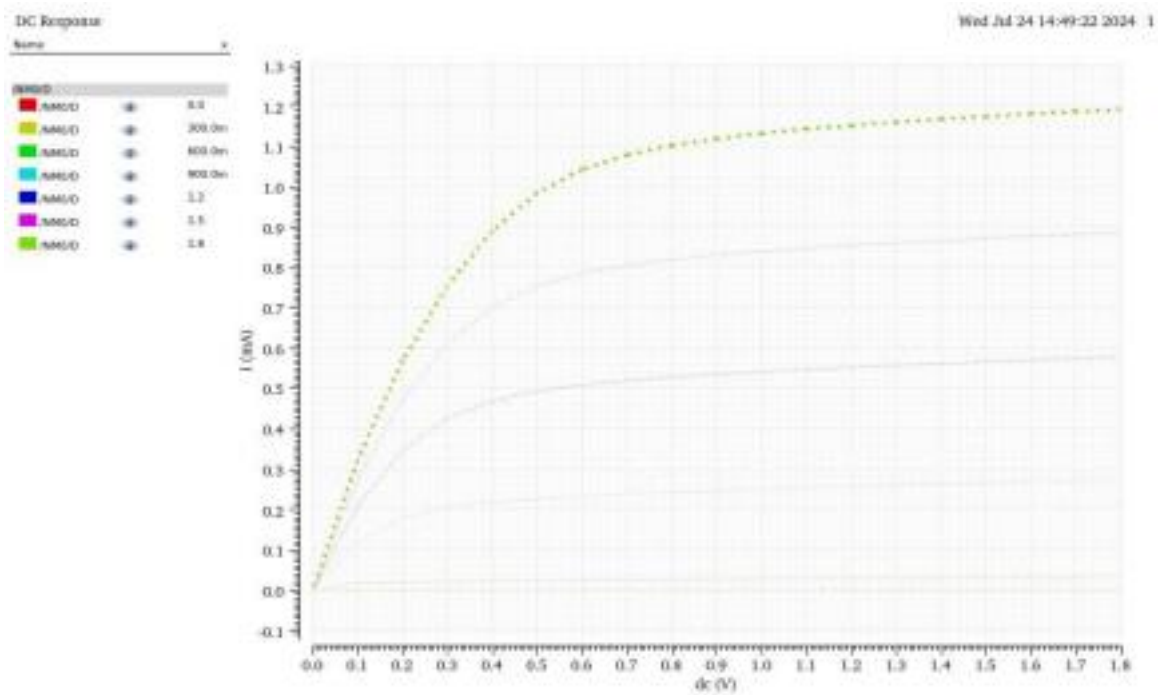
2. NMOS INPUT CHARACTERISTICS (V_{gs} vs I_d):



3. NMOS PARAMETRIC ANALYSIS:



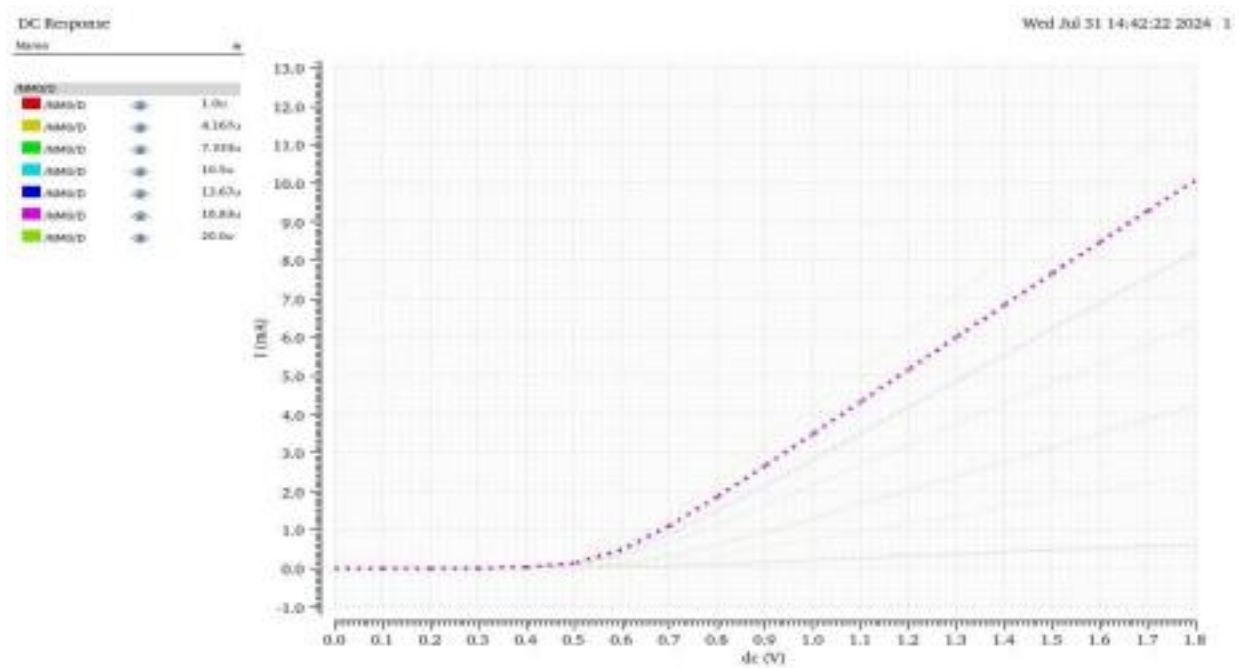
4. NMOS OUTPUT CHARACTERISTICS (V_{ds} vs I_d):



5. NMOS CHARACTERISTICS FOR VARIABLE WIDTH OF MOSFET:



6. CHARACTERISTICS OF ABOVE SCHEMATIC:



INFERENCE:

Characteristics of NMOS transistors were analyzed by visualizing the output graphs of I_d v/s V_{gs} and I_d v/s V_{ds} .

As we can see from the observed graphs,

a) In the cut off region, $V_{gs} < V_{tn}$ and $I_d=0$

b) In the saturation mode,

$$V_{gs} > V_{tn}$$

$$V_{ds} \geq (V_{gs} - V_{tn})$$

$$I_d = \frac{1}{2}(\mu * C_{ox} * W/L) (V_{gs} - V_{tn})^2$$

c) In the triode mode,

$$V_{gs} > V_{tn},$$

$$V_{ds} < (V_{gs} - V_{tn}),$$

$$I_d = (\mu * C_{ox} * W/L) [V_{gs} - V_{tn} - (V_{ds}/2)] V_{ds}$$

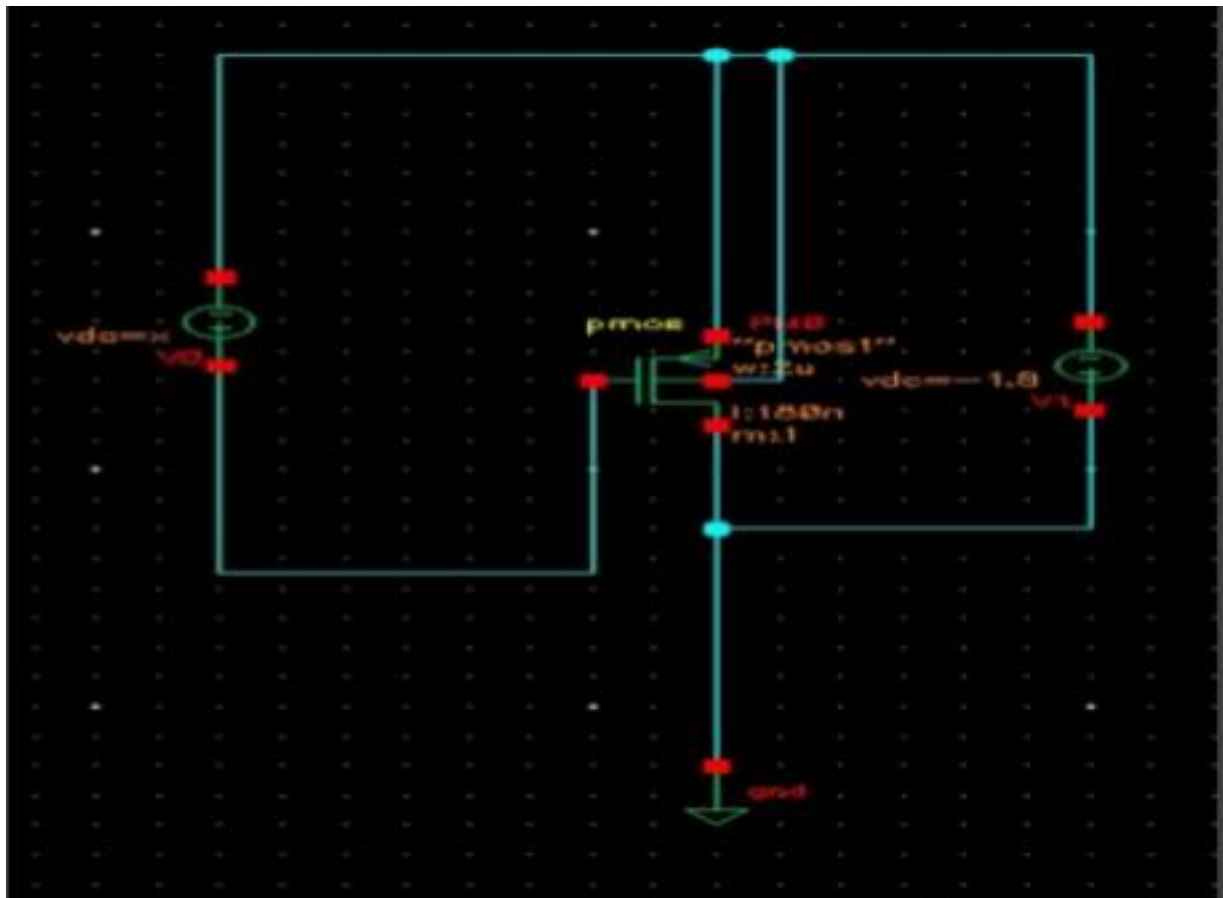
d) If width (w) is increased, I_d increases for each potential of V_{gs} once it becomes greater than V_{tn} .

PROCEDURE FOR PMOS:

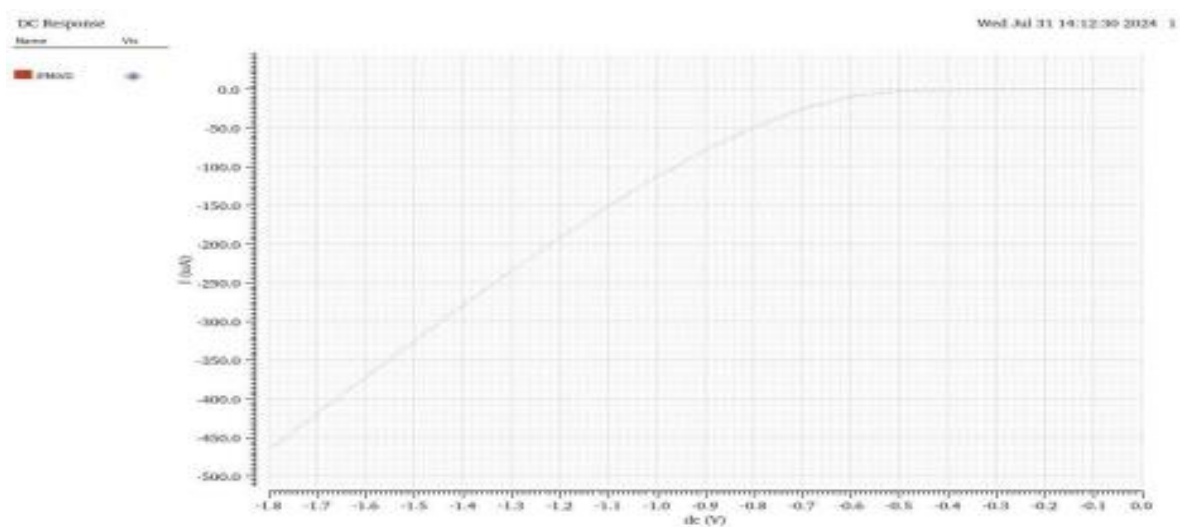
1. Create a schematic.
2. Configure DC Analysis with the input gate voltage V_{sg} as the component parameter and sweep range of 0 to 1.8V
 - a) Plot the drain current I_d .
 - b) Define the input gate voltage V_{sg} as a variable parameter "x". c) Configure dc analysis for various drain source voltage V_{sd} by defining it as the component parameter and sweep range of 0 to 1.8V.
 - d) Plot the drain current I_d .
 - e) Perform the parametric analysis for various values of V_{sg} is defined as "x".

SCREENSHOTS:

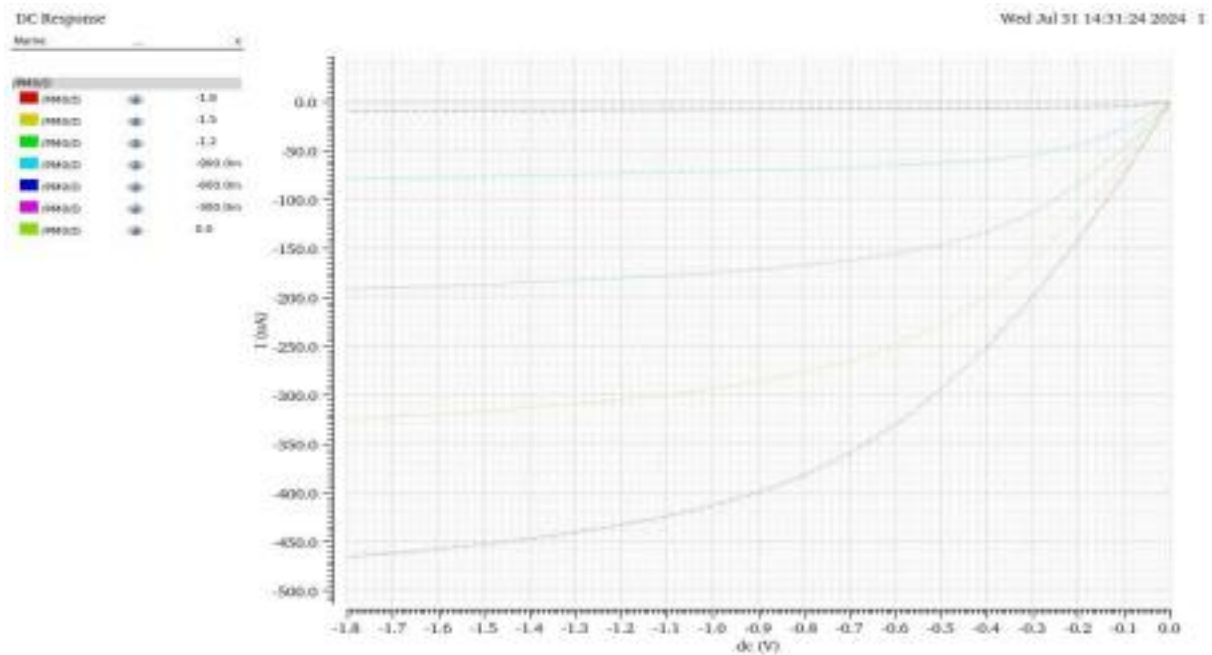
1. SCHEMATIC:



2. INPUT CHARACTERISTICS (V_{sg} vs I_d):



3. OUTPUT CHARACTERISTICS (V_{sd} vs I_d):



INFERENCE:

Characteristics of PMOS transistors were analyzed by visualizing the output graphs of I_d v/s V_{sg} and I_d v/s V_{sd} .

As we can see from the observed graphs,

a) In the cut off region, $V_{sg} < (-V_{tp})$ and $I_d = 0$

b) In the saturation mode,

$$V_{sg} > (-V_{tp})$$

$$V_{sd} \geq (V_{sg} + V_{tp}),$$

$$I_d = \frac{1}{2} (\mu * C_{ox} * W/L) (V_{sg} - V_{tp})^2$$

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c) In the triode mode,

$$V_{sg} > (-V_{tp}),$$

$$V_{sd} < (V_{sg} + V_{tp}),$$

$$I_d = (\mu * C_{ox} * W/L) [V_{sg} - V_{tp} - V_{sd}/2] V_{sd}$$