CHALLENGING EXPERIMENT STATIC CMOS CIRCUIT

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22BEC1002

AIM:

To draw a static CMOS circuit of given Boolean expressions and verify the truth table using transient analysis.

TOOLS:

Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology library.

PROCEDURE:

1. Consider the expressions C = ((A + B) Cin + AB) and S = ((A + B + Cin) C + ABCin) which are expressions of sum and carry of a full adder combinational circuit.
2. Draw a static CMOS diagram for the given expression using PMOS and NMOS.
3. Verify the truth table using transient analysis.
4. Calculate delay and power for Sum and carry.

SCREENSHOTS AND TABULAR COLUMN:

Delay calculation for sum:

Values	Input signal	Output signal	rise/fall	delay(ps)
001	**Cin(1r)**	**Sum**	**rise**	**105.8**
010	**Cin(1f)**	**Sum**	**rise**	**88.11**
111	**Cin(2r)**	**Sum**	**rise**	**105.6**
100	**Cin(2f)**	**Sum**	**rise**	**88.08**
011	**B(1r)**	**Sum**	**fall**	**247.0**
110	**A(1r)**	**Sum**	**fall**	**137.4**
101	**B(1f)**	**Sum**	**fall**	**230.6**
000	**A(1f)**	**Sum**	**fall**	**119.4**

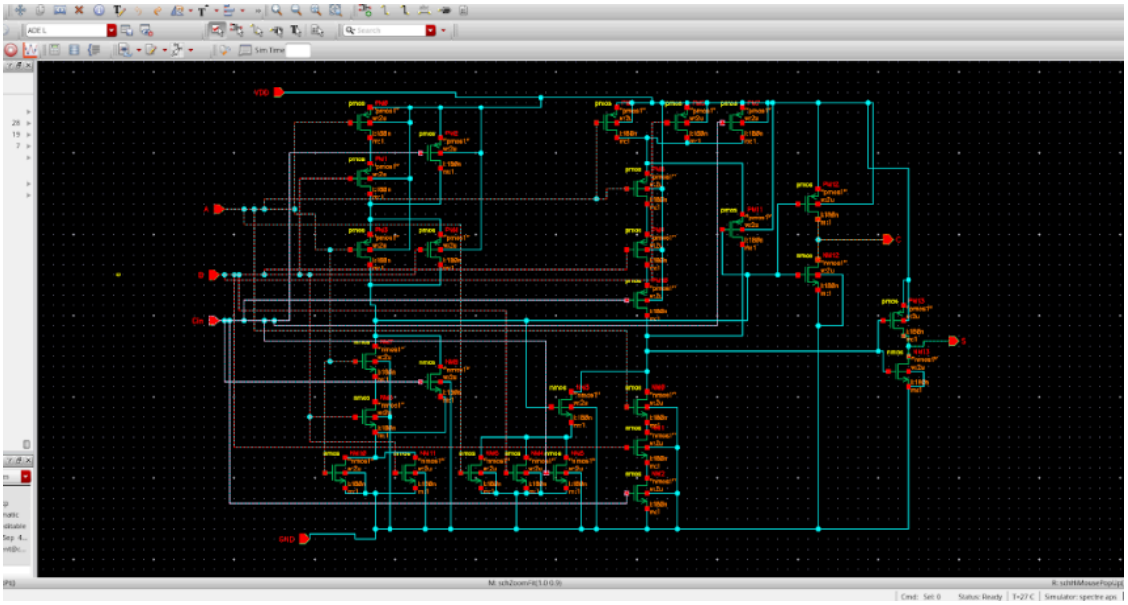
1. For rising:
    a) Best case delay: 88.08ps (100)
    b) Worst case delay: 105.8ps (001)
2. For falling:
    a) Best case delay: 119.4ps (000)
    b) Worst case delay: 247.0ps (011)

Delay calculation for carry:

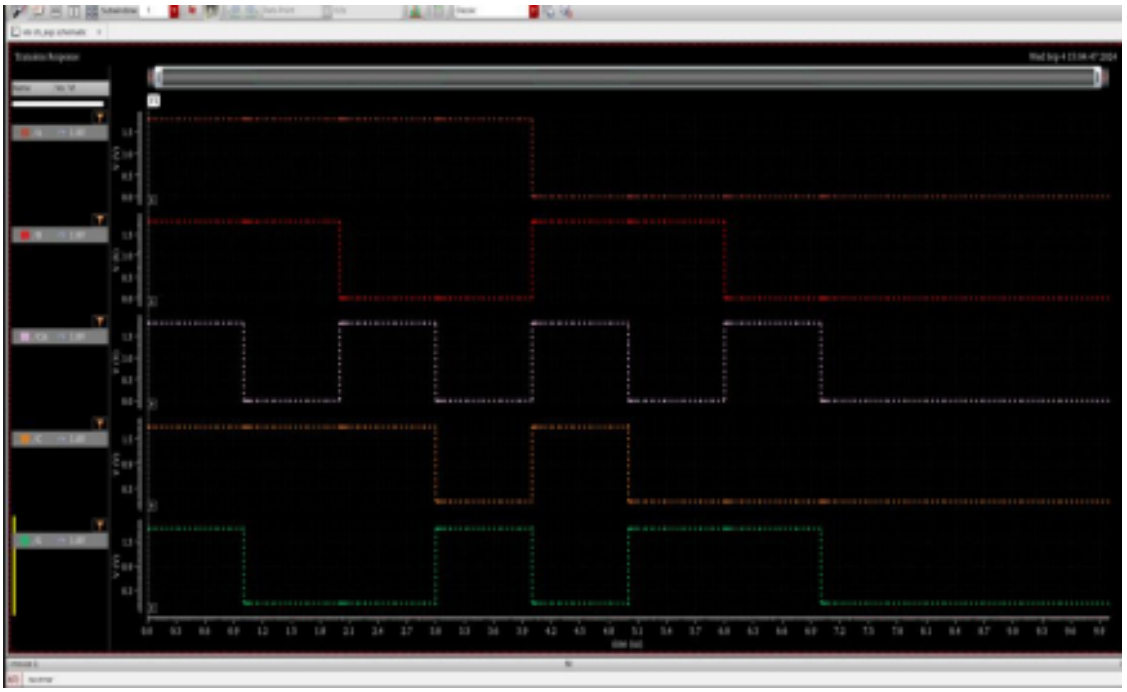
Values	Input signal	Output signal	rise/fall	delay(ps)
011	**B(1r)**	**C**	**rise**	**196.3**
110	**A(1r)**	**C**	**rise**	**165.3**
101	**Cin(3r)**	**C**	**rise**	**198.1**
111	**B(4r)**	**C**	**rise**	**73.79**
001	**Cin(1r)**	**C**	**fall**	**80.07**
010	**Cin(1f)**	**C**	**fall**	**46.37**
100	**B(2f)**	**C**	**fall**	**75.11**
000	**Cin(4f)**	**C**	**fall**	**80.21**

1. For rising:
    a) Best case delay: 73.79ps (111)
    b) Worst case delay: 198.1ps (101)
2. For falling:
    a) Best case delay: 46.37ps (010)
    b) Worst case delay: 80.21ps (000)

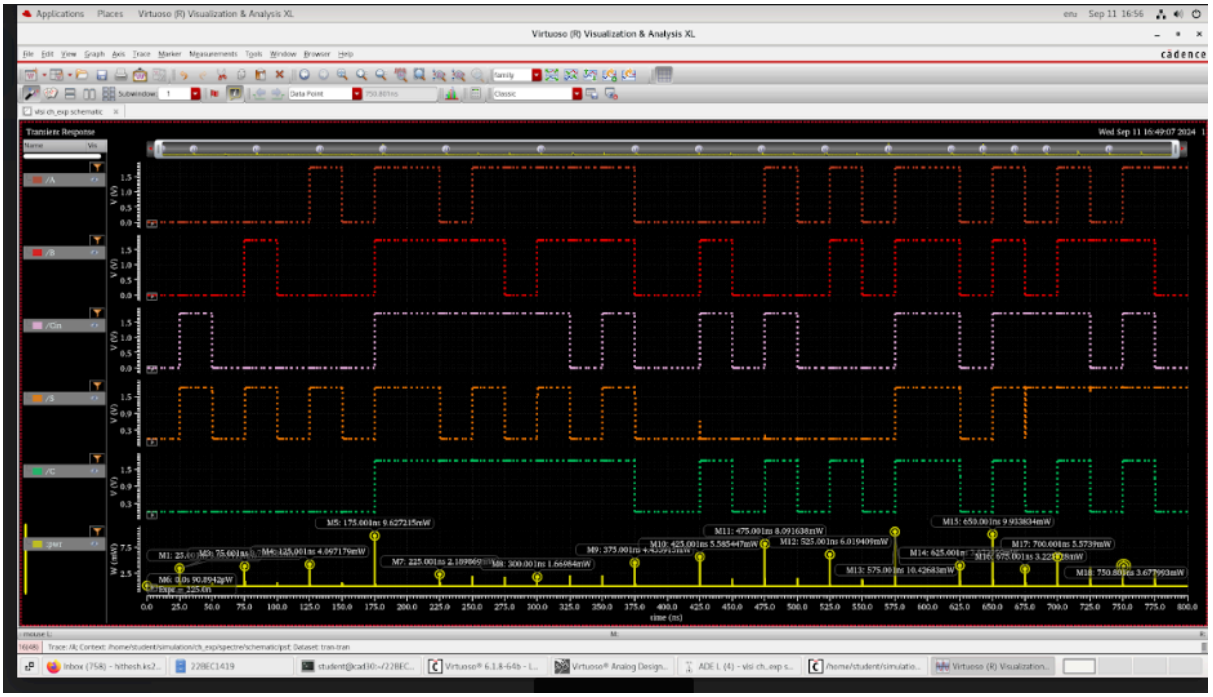
1. SCHEMATIC OF CMOS CIRCUIT:



2. TRANSIENT ANALYSIS:



3. POWER CALCULATION:



INFERENCE:

1. Truth table is verified by giving different input values for the variables for the combinational circuit.
2. The transient analysis is performed to verify the CMOS circuit.
3. The delay and power for sum and carry is calculated for all values and best and worst cases delay are analyzed.