NMOS AND CMOS INVERTER CHARACTERISTICS

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AIM:

To analyze the characteristics of NMOS inverter with resistive load and CMOS inverter.

TOOLS REQUIRED:

Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology library

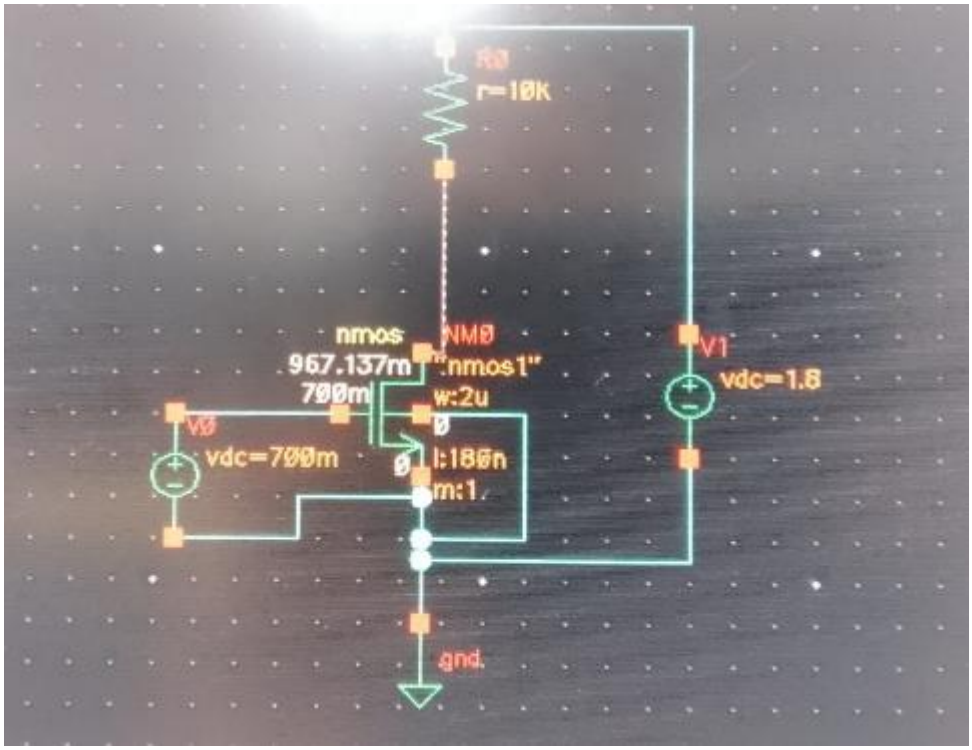
NMOS INVERTER:

PROCEDURE:

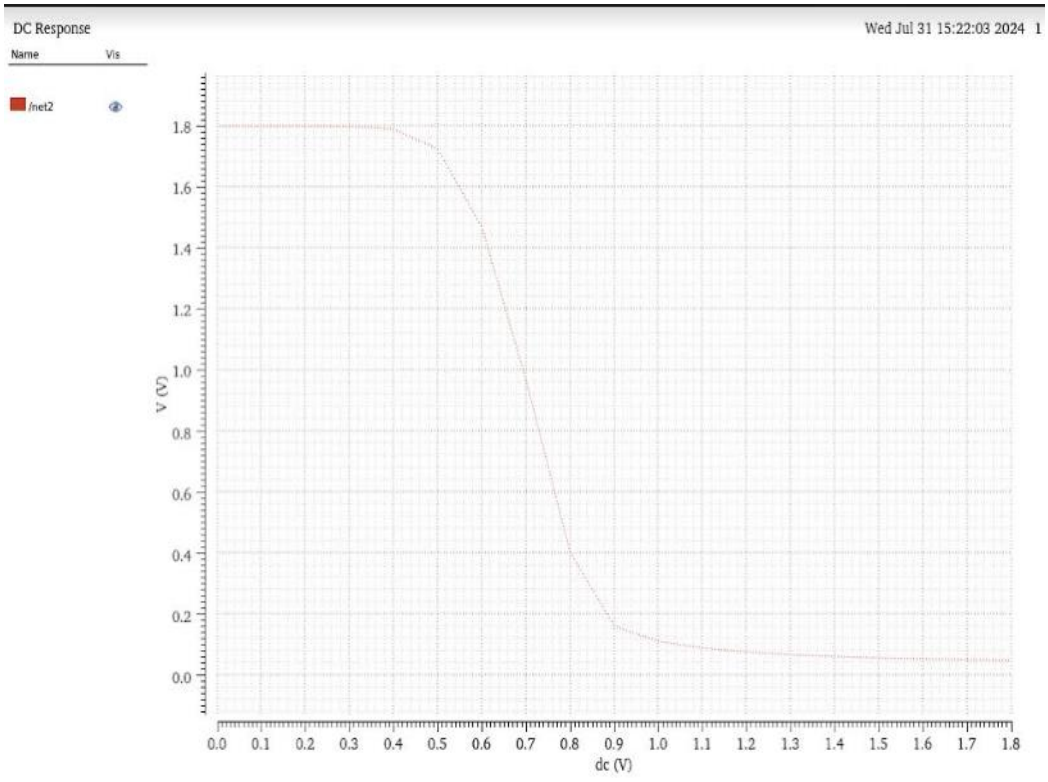
1. Create a schematic.
2. Configure DC Analysis with the input gate voltage Vgs as the component parameter and sweep range of 0 to 1.8V
    - Plot the drain current ID.
3. Define the resistance R as a variable parameter “x”
    - Configure dc analysis for various drain source voltage Vds by defining it as the component parameter and sweep range of 0 to 1.8V
    - Plot the drain current ID
    - Perform the parametric analysis for various values of R which is defined as “x”.

SCREENSHOTS:

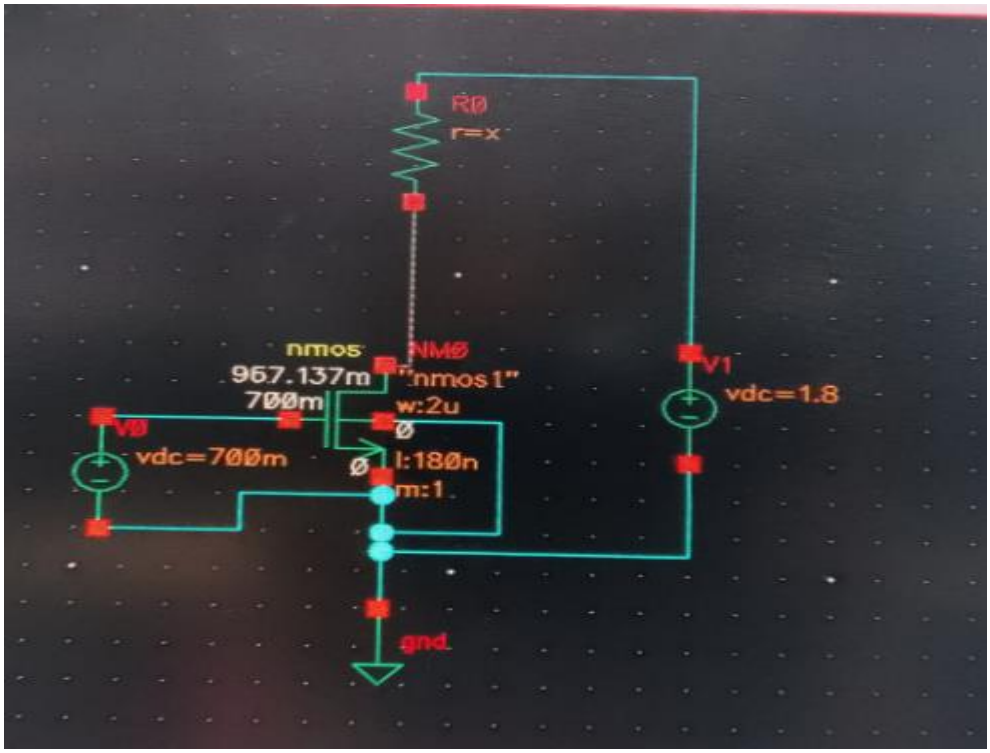
1. NMOS INVERTER CIRCUIT WITH RESISTIVE LOAD:



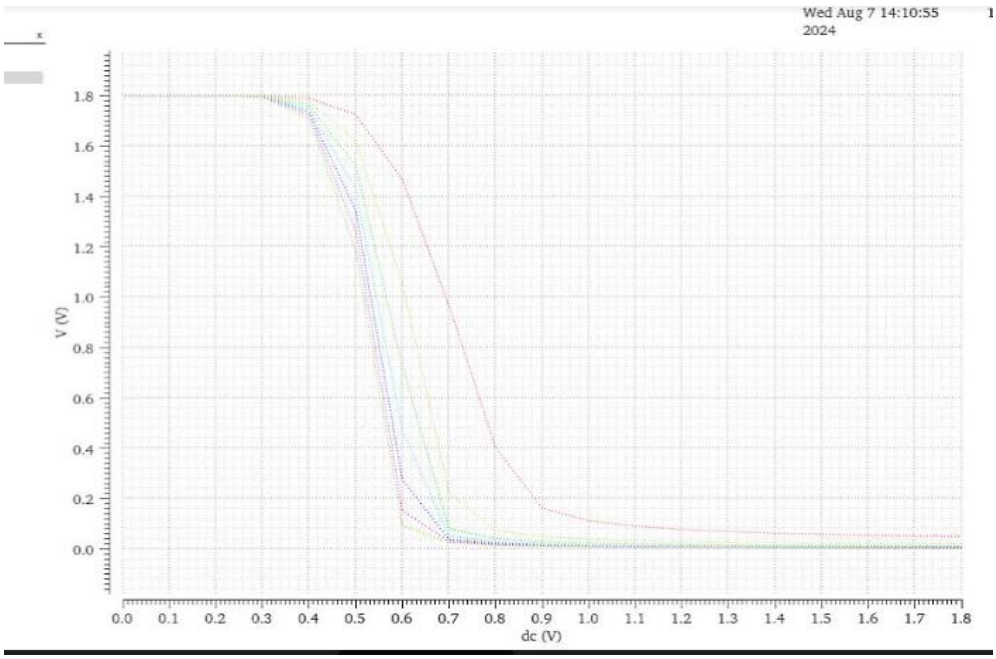
2. CHARACTERISTICS:



3. INVERTER WITH VARIABLE RESISTOR:



4. PARAMETRIC ANALYSIS:



INFERENCE:

1. From the graphs, till Vgs<Vth in cut-off region, (input: logic 0) it is seen that NMOS does not conduct. Hence no current and voltage drop across resistance is 0. Vout=Vdd. Output logic: 1.
2. If Vgs is slightly greater than Vth, (linear), there is a potential drop in resistance and device starts conducting. This si called transition period and Vout<Vdd(slightly).
3. In saturation region where Vgs>>Vth input logic is 1. Increase in Id results in very high potential drop in resistance. Vout is close to 0.
4. Disadvantage of NMOS inverter is that to get ideal characteristics, we need high value of resistance which will take up large area.

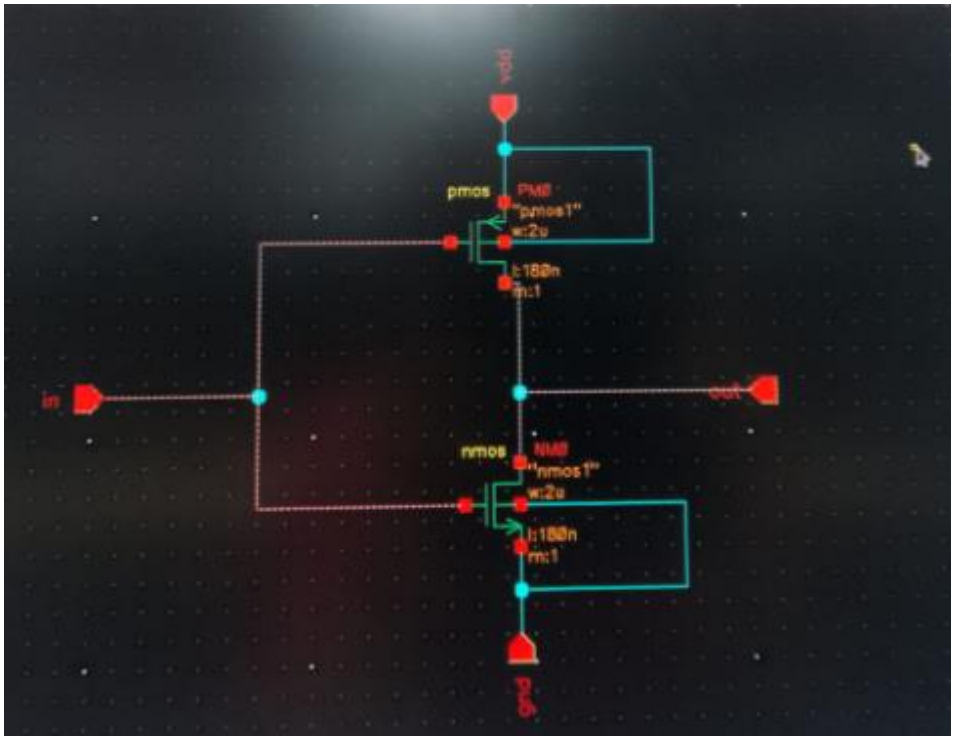
CMOS CHARACTERISTICS:

PROCEDURE:

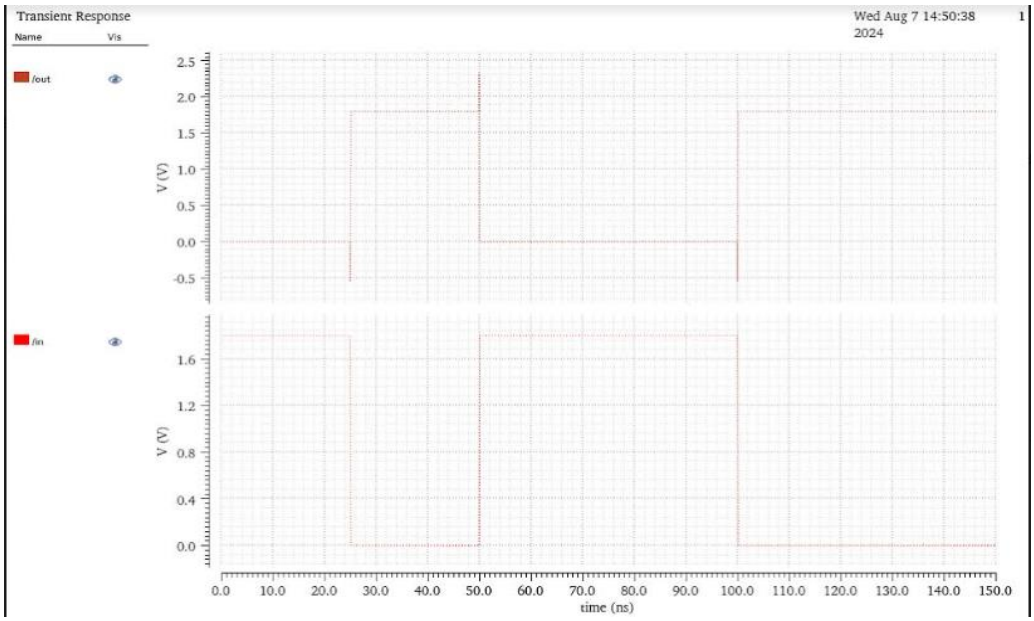
1. Create a schematic and define the input pattern as
   - One value=1.8
   - Zero value=0
   - Rise time=1ps
   - Fall time=1ps
   - Period = 25 ns
   - Source type= bit
   - Pattern parameter=10110
   - Apply → OK
2. Perform transient analysis and obtain the transient signals
3. Perform dc analysis and varying it from 0 to 1.8V and the output to be plotted as the output voltage.
4. Create the symbol of inverters and do transient analysis.

SCREENSHOTS:

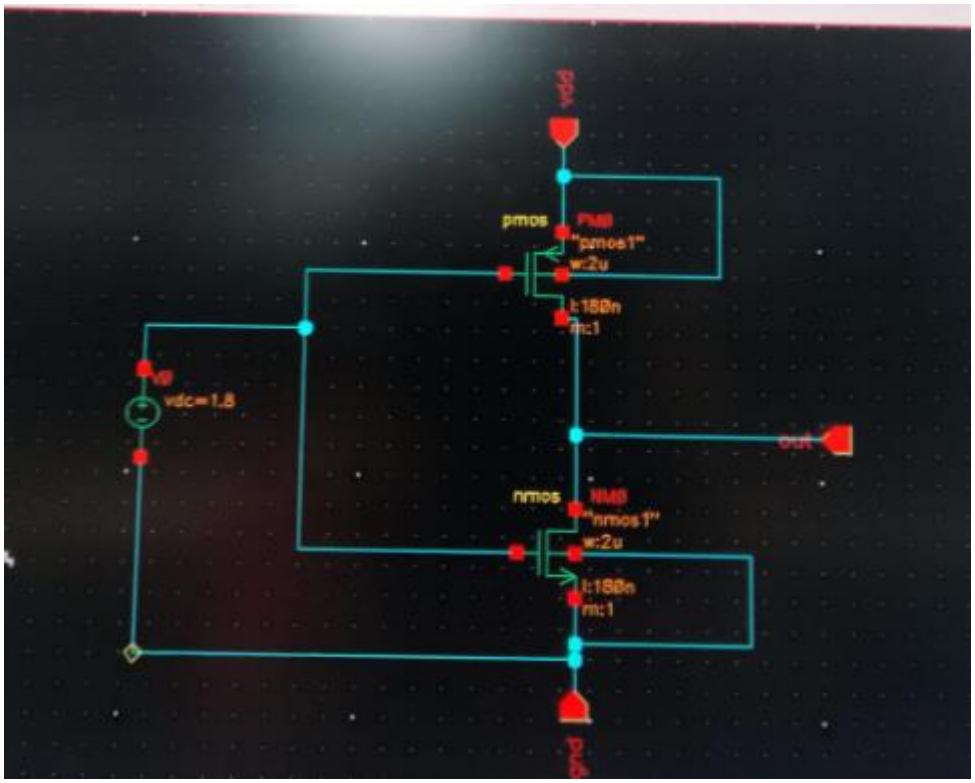
1. SCHEMATIC FOR TRANSIENT ANALYSIS:



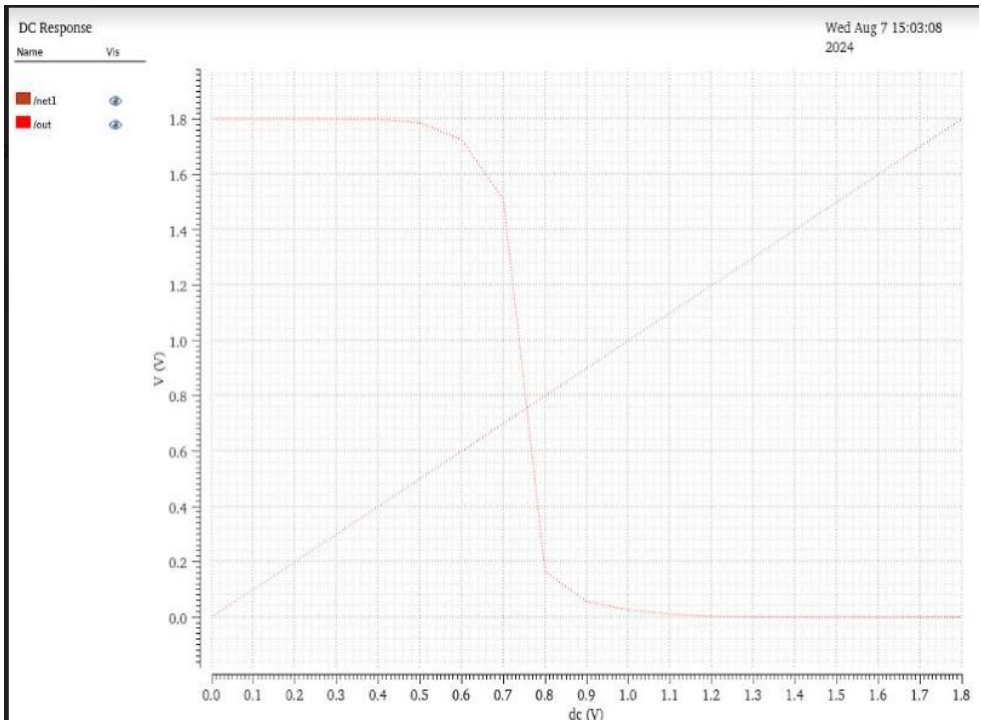
2. TRANSIENT ANALYSIS:



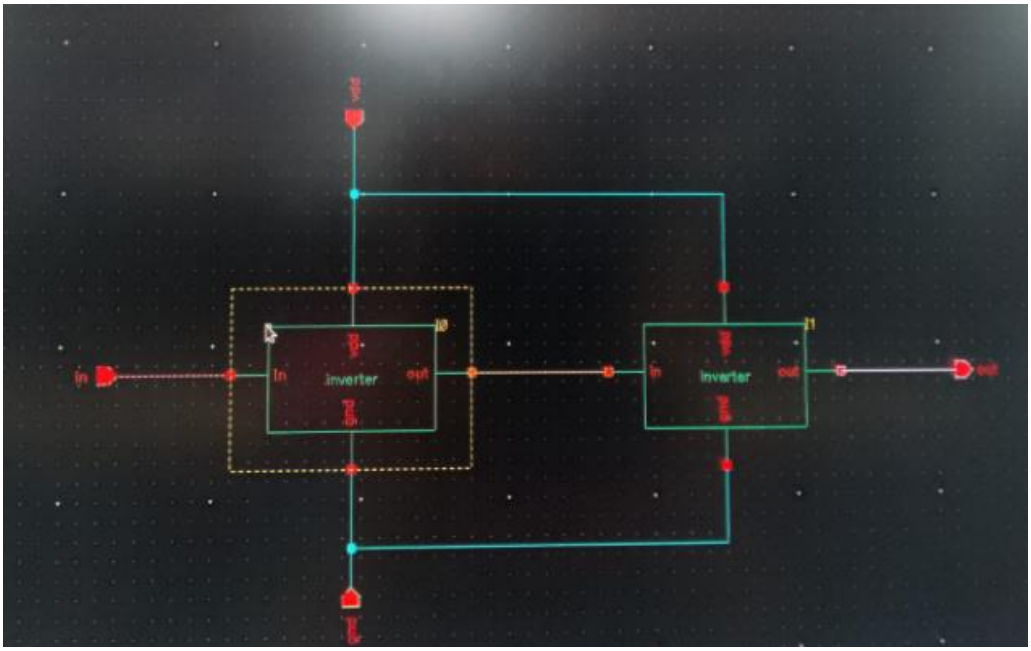
3. DC ANALYSIS SCHEMATIC:



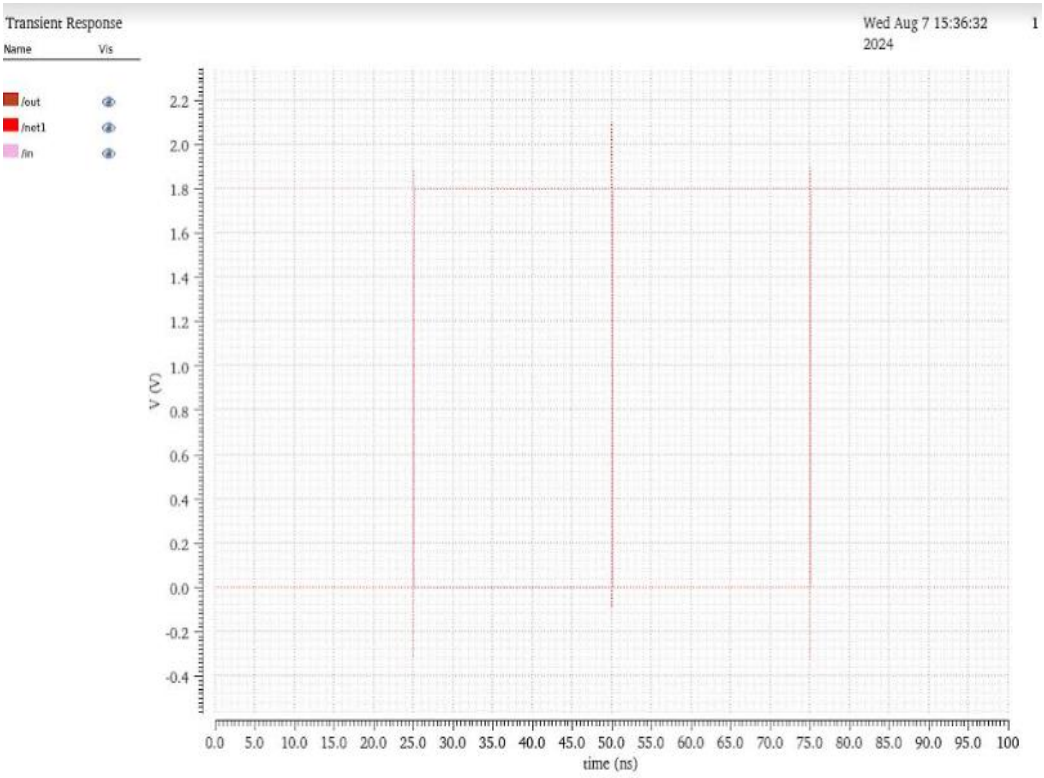
4. DC CHARACTERISTICS:



5. SYMBOL CREATION FOR INVERTER:



6. TRANSIENT ANALYSIS:



INFERENCES:

1. CMOS inverter solves the problem in NMOS since it does not have a resistance.
2. If logic 1 is given, NMOS is switched on and switch is closed between S and D. Since both S and D are grounded, output is 0 (pull-down).
3. If logic 0 is given, PMOS is switched on and S and D are connected to each other giving Vout=Vdd, in other words, logic 1 output is obtained (pull-up).