DESIGN OF NAND & NOR GATES AND SYMBOL CREATION

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22BEC1002

AIM:

To design 2 input NOR Gate and 2 input NAND Gate circuits and create symbols and check the functionality using a Boolean expression.

TOOLS:

Linux operated computing system, Cadence® Virtuoso, gpdk 180nm technology library

PROCEDURE:

1. Create a schematic for NOR and NAND gate giving inputs A: 0011 and B: 0101.
2. Obtain the transient analysis output.
3. Ensure the functionality of the circuit and save it.
4. For symbol creation: Create cell view from cell view
5. Assign the input and output pins positions
6. Edit the opened symbol (default rectangle) according to the gate using polygon and circle options.
7. Save the symbol and in a new schematic can check the functionality by using the symbol as an instance.
8. Use the equation $\overline{(A+B)+CD}$ with values:

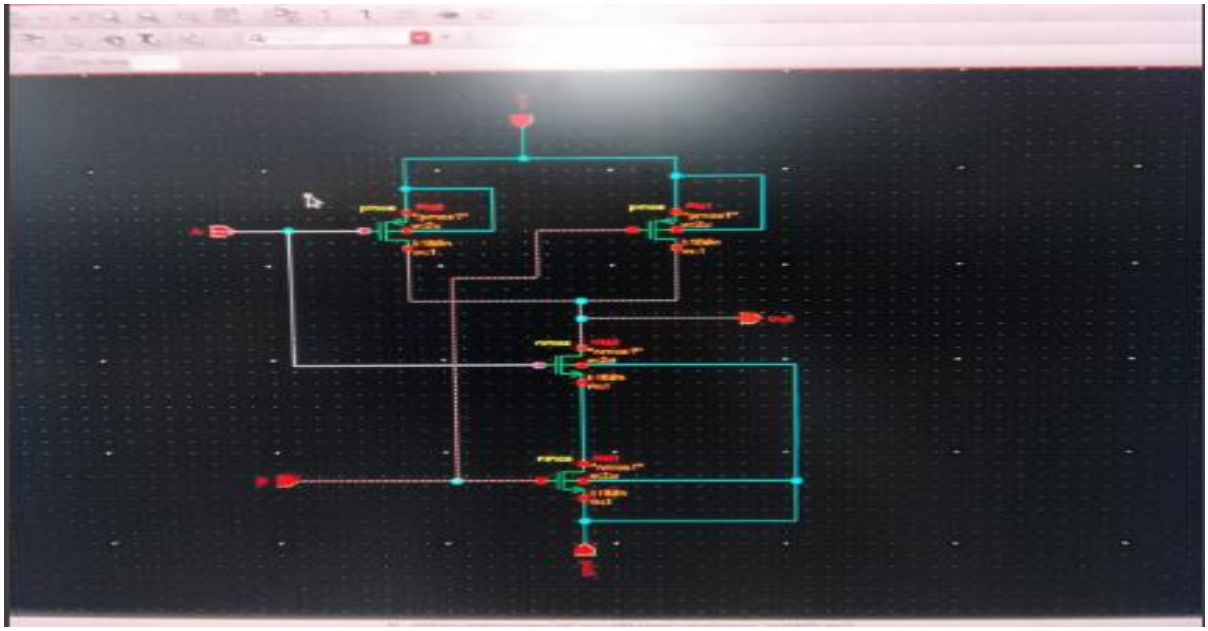
   a) A: 00000 b) B: 00001 c) C: 00110

   d) D: 01010

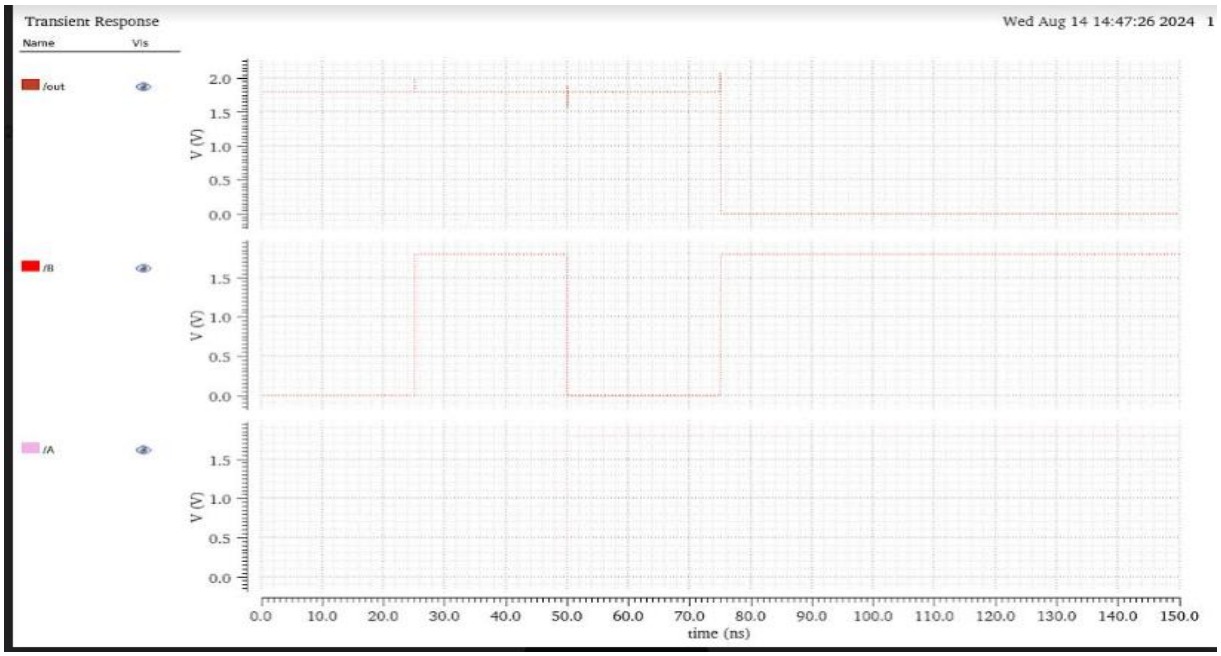
to verify the symbols.

SCREENSHOTS:

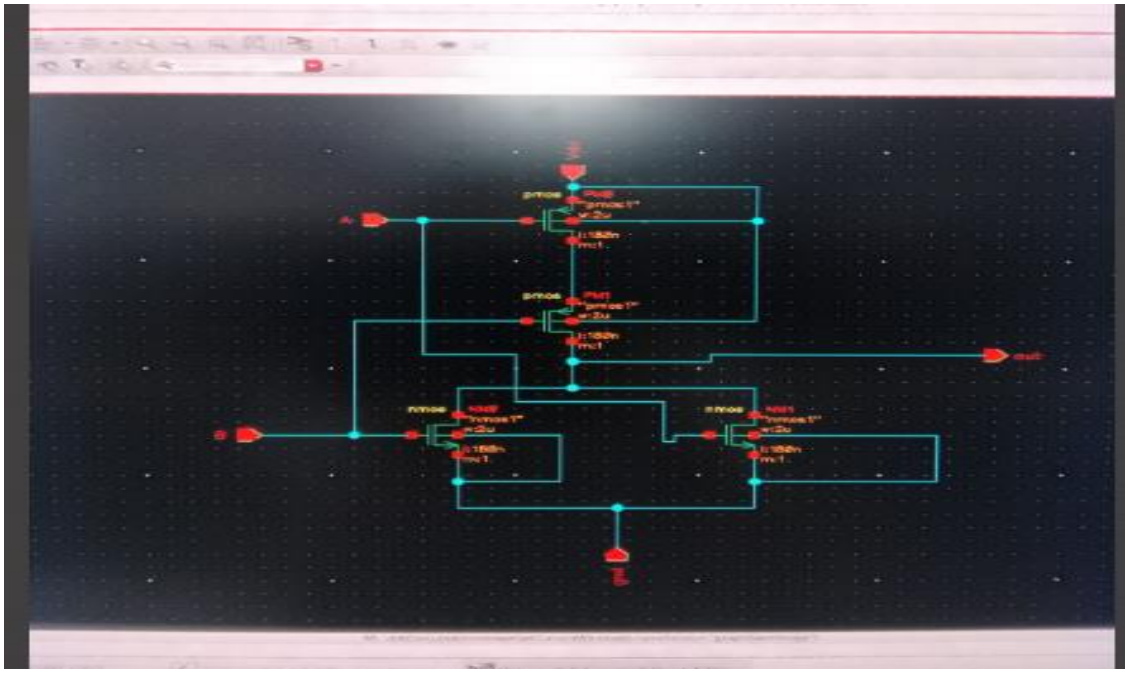
1. **NAND GATE SCHEMATIC:**



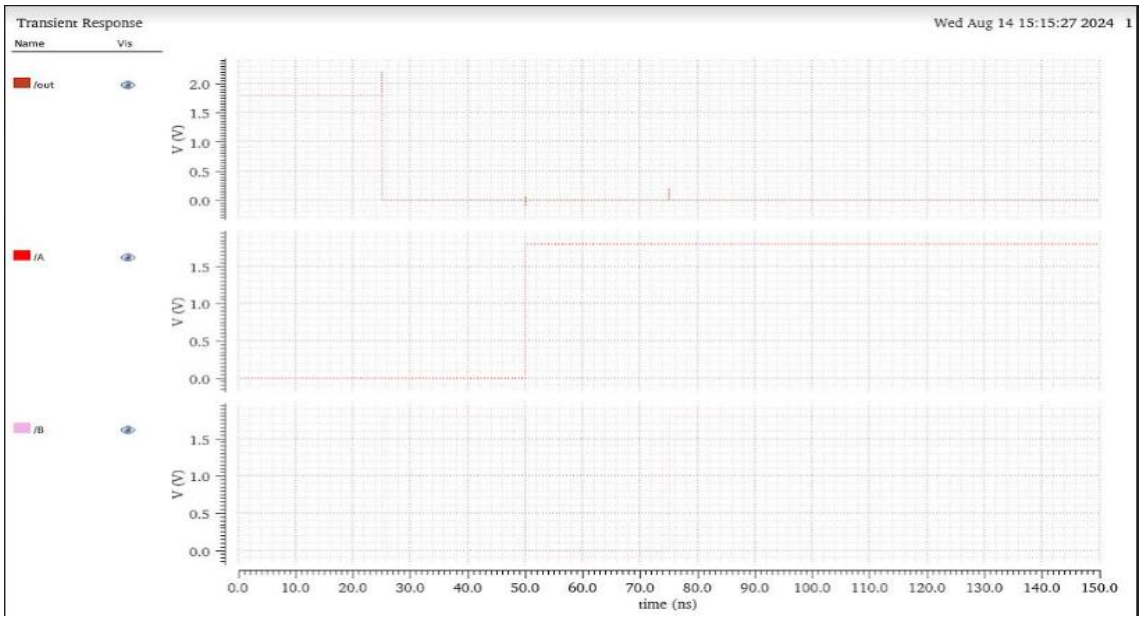
2. **TRANSIENT ANALYSIS:**



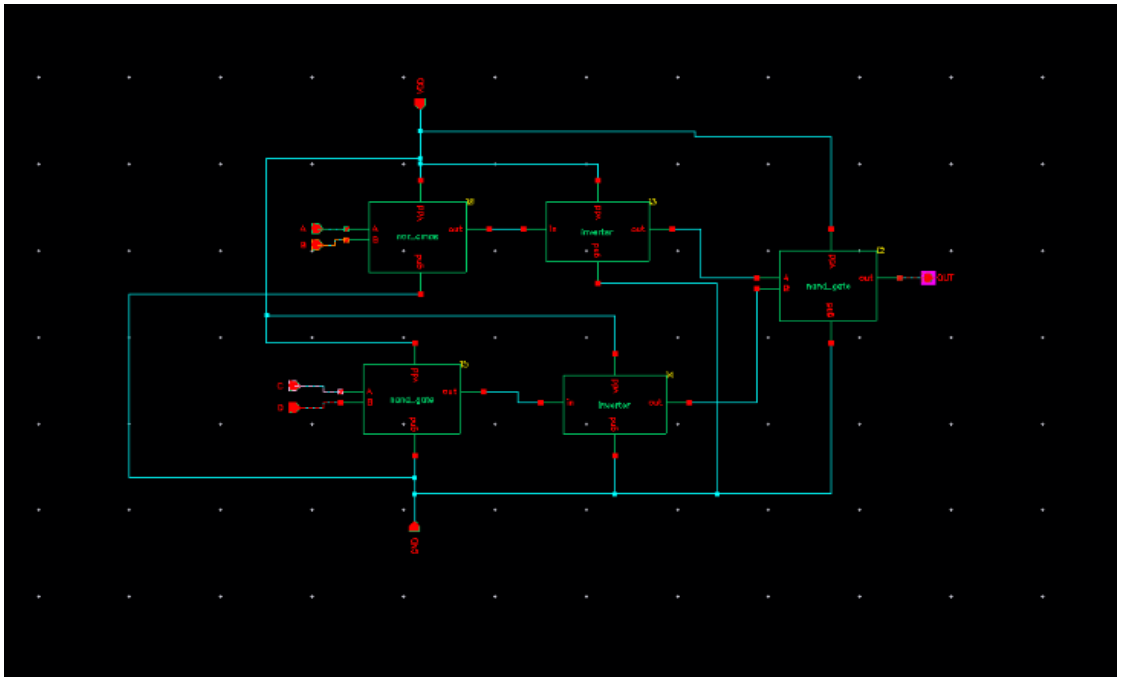
3. NOR GATE SCHEMATIC:



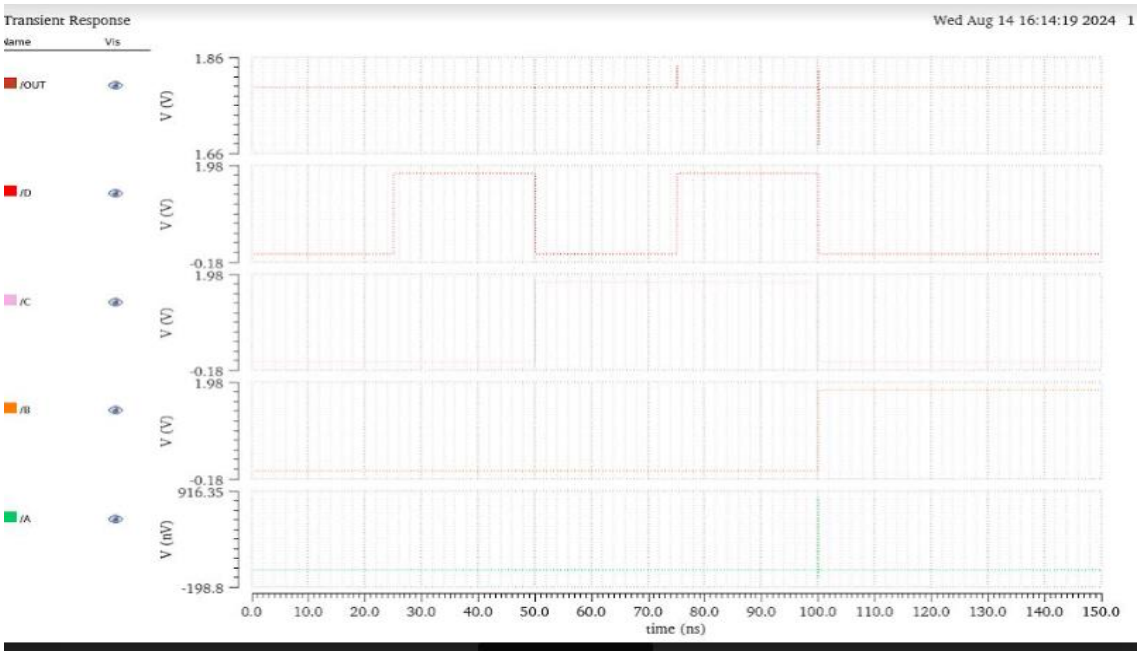
4. TRANSIENT ANALYSIS:



5. SCHEMATIC OF EQUATION USING SYMBOLS:



6. TRANSIENT ANALYSIS:



INFERENCES:

1. **For pull down network, ‘.’ Represents series and ‘+’ represents parallel connections.**
2. **The connections are opposite for pull up network.**
3. **The required outputs were obtained and analysed with the truth table.**