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Low Power Digital System Design

Circuit-Level LPD Techniques (Cont.)

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Dual-V_{DD} Circuits

- Dual V_{DD} technique is used mainly for dealing with the switching power problem.
  - V_{DD} reduction =>
    - Switching Power decreases quadratically
    - Sub-threshold Leakage Power deceases linearly
  - V_{th} reduction =>
    - Does not have any impact on switching energy
    - Increases Sub-threshold Leakage Power exponentially

Impact on Circuit Performance

$$P_{SW} = \alpha C_L V_{DD}^2 f \qquad V_{DD} \downarrow \Rightarrow P_{SW} \downarrow$$

$$Delay \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \qquad V_{DD} \downarrow \Rightarrow Delay \uparrow$$

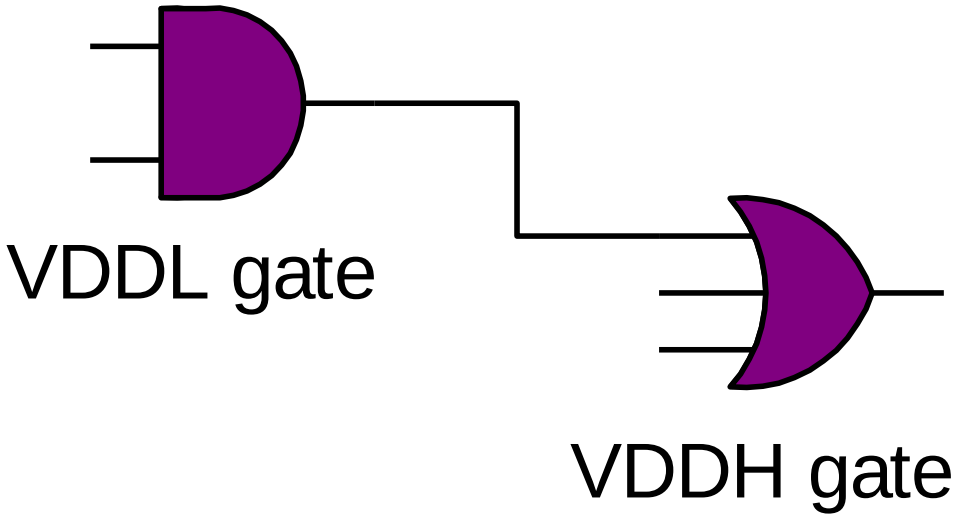
Dual-V_{DD} Circuits

- Main Idea: Similar to dual-V_{th} circuits
  - The circuit part off the critical path is made to operate at the reduced voltage V_{DDL}, while the part on the critical path is made to operate at the original voltage V_{DDH}.

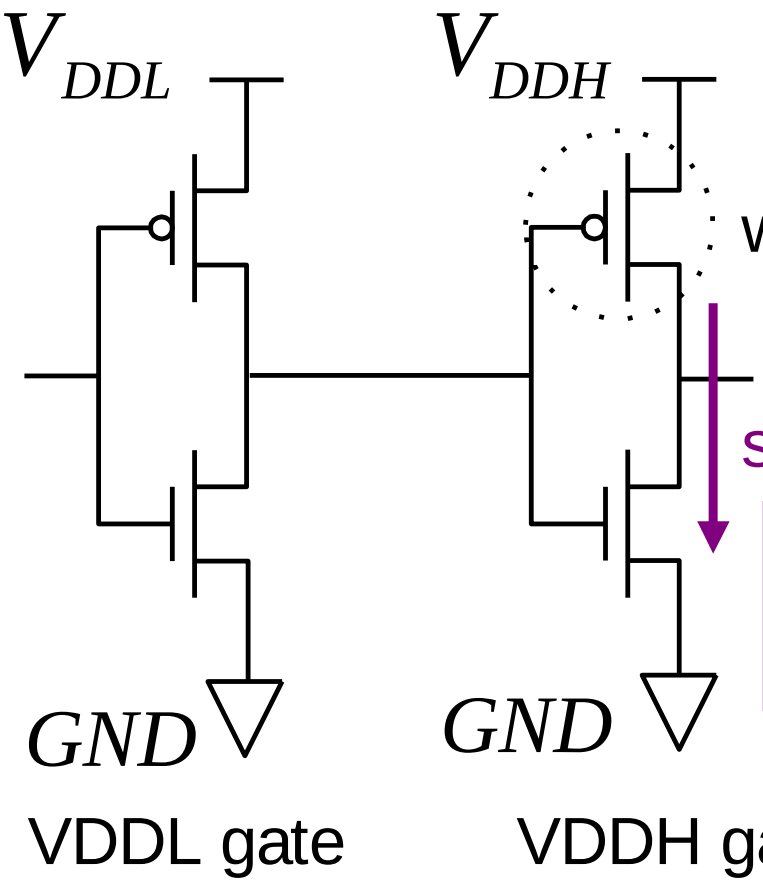
- Not all the gates in non-critical paths can be assigned V_{DDL}, otherwise, the critical path may change.

A Serious Problem in Multi-V_{DD} Circuits

- Occurs due to the direct connection of a VDDL gate to a VDDH one.
  - Short Circuit Static Power
  - Noise Sensitivity Problem



Short Circuit Static Power Problem



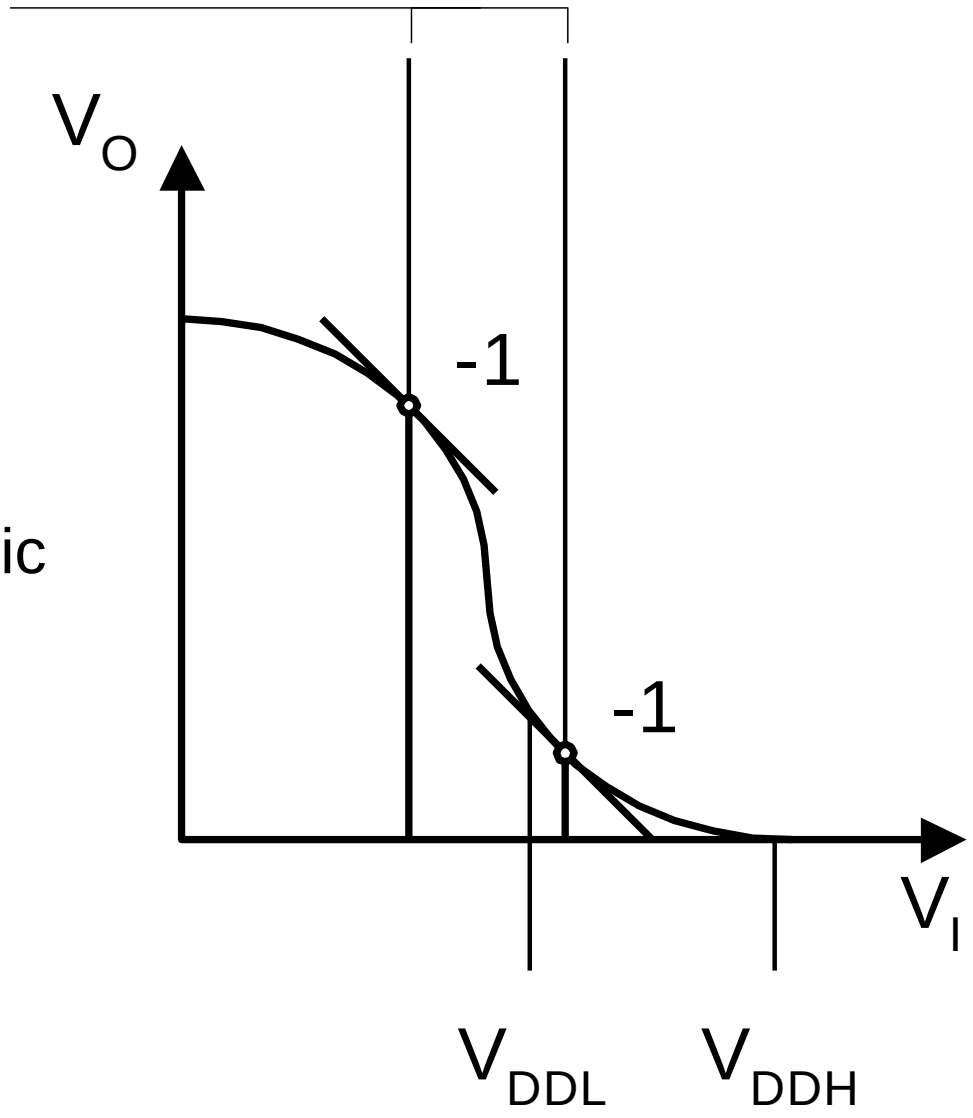
$$I_{SC-Static} = \frac{\beta_p}{2}(V_{DDH} - V_{DDL} + V_{tp})^2$$

- Note: This problem is much more serious than the similar problem in the reduced voltage swing technique used in on-chip interconnects.

Noise Sensitivity

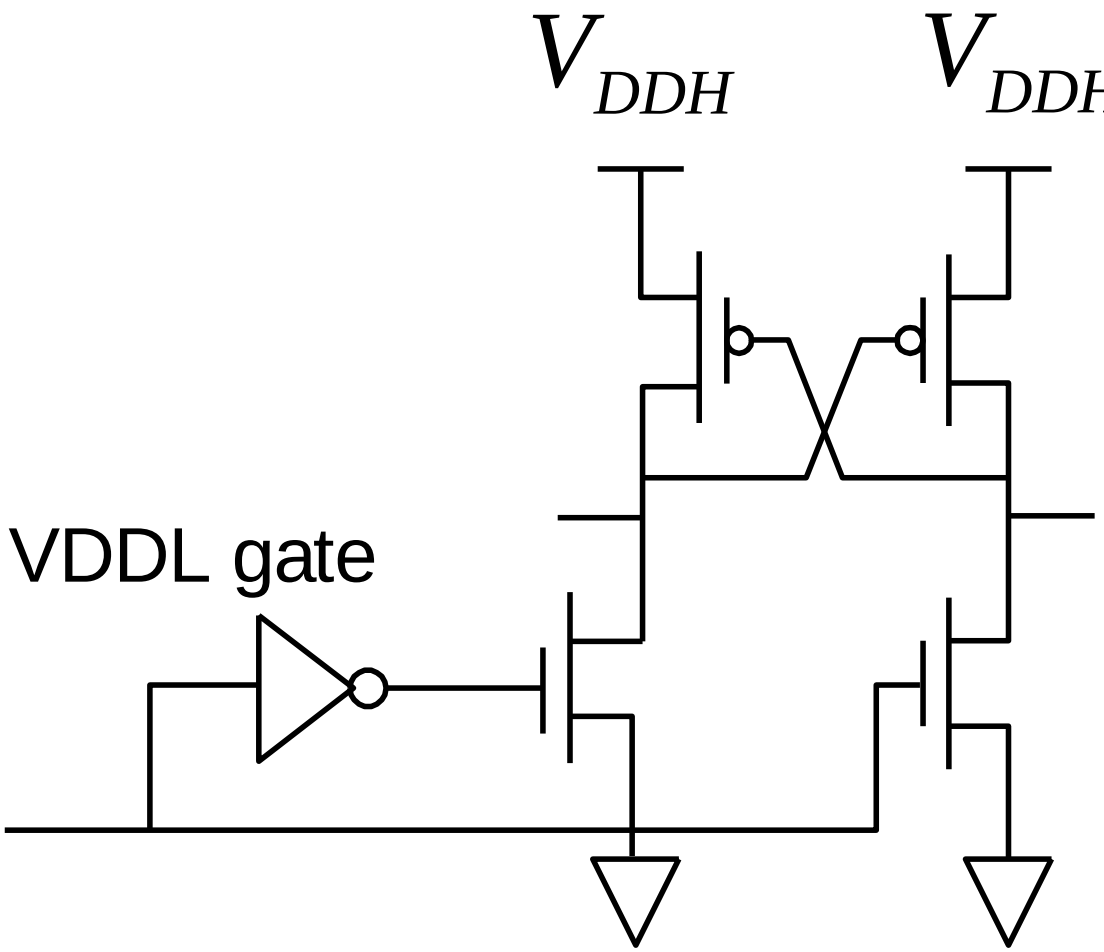
Operates as an amplifier

CMOS Inverter:
Transfer characteristic



Solution: SDCVSL Level Converter

- Static Differential Cascode Voltage Switch Logic
  - pMOS transistors are not connected to the gate inputs.



Problems in Dual-V_{DD} Technique

- Area and power overhead of level converters.
  - Problem Formulation: choose VDDL gates and/or FFs such that
    - minimize the number of level converters
    - minimize the entire power
    - meet the timing constraints
- Placement and routing problem.

Clustered Voltage Scaling Structure

- In the CVS structure the possible connection pattern among gates is any of the following:

  1) inter-VDDH gates

  2) inter-VDDL gates

  3) a VDDH gate to a VDDL gate

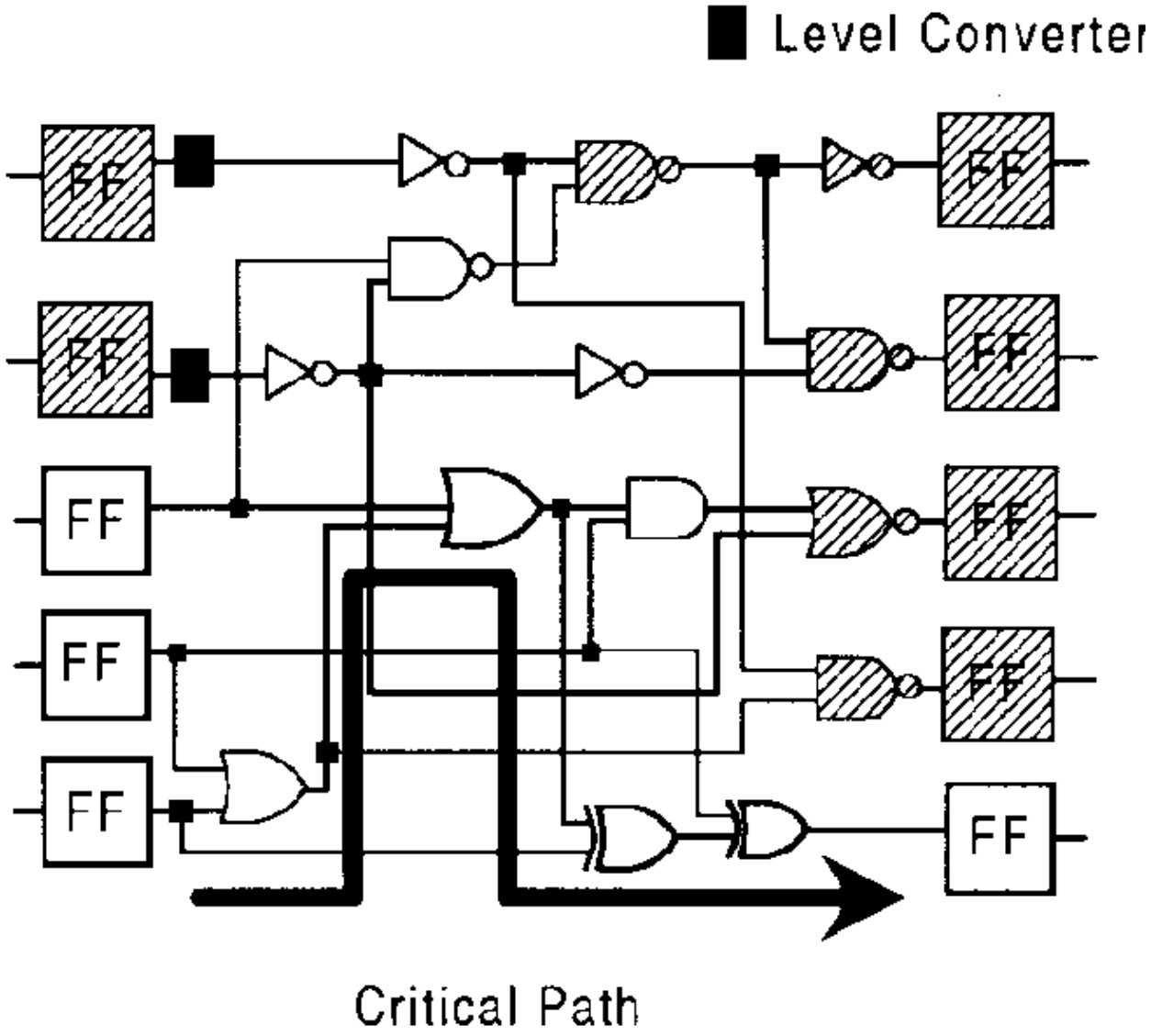
- The only portions requiring level converters:

  - a VDDL FF to a VDDH gate

CVS Structure

- Objectives:
  - Reduce the number of level converters
    - the number of needed level converters is at most the same as the number of VDDL flip-flops.
  - Keep VDDL gates together and connected also keep VDDH gates together and connected.
    - Ameliorate placement and routing problems.
- Note: CVS is not the best solution but it is simple yet effective.

CVS Structure: Example



Optimal Voltage of V_{DDL}

- Lower V_{DDL} =>
  - Smaller number of VDDL gates
  - More power reduction at a single VDDL gate
- Higher V_{DDL} =>
  - Larger number of VDDL gates
  - Less power reduction at a single VDDL gate
- The optimal V_{DDL} voltage varies from circuit to circuit.
  - Several CVS structures are obtained for the same circuit with different V_{DDL} values.
  - The power dissipation of the circuit structures are evaluated and compared.

References

L. Wei, et. al., "Design and Optimization of Dual-Threshold Circuits for Low-Voltage Low-Power Applications", *IEEE Transactions on VLSI*, 1999.

K. Usami, et. al., "Automated Low-Power Technique Exploiting Multiple Supply Voltages Applied to a Media Processor", *IEEE Journal of Solid-State Circuits*, 1998.