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Low Power Digital System Design

Circuit-Level Techniques (Cont.)

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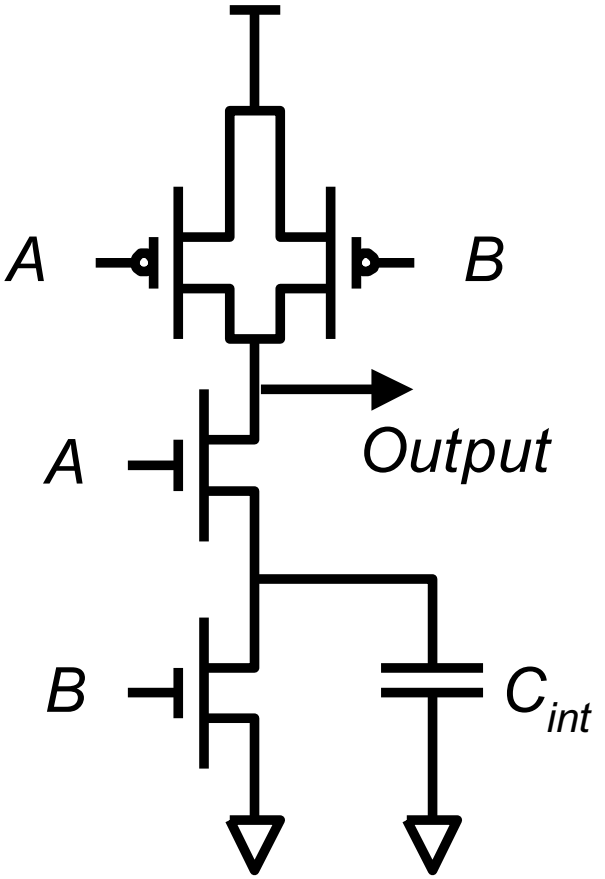
Input reordering at the circuit level

- Exhaustive enumeration method
  - All possible orders are checked to determine the best input ordering.
    - Simulation
    - Analytical methods
  - Suitable for a gate with a small number of transistors.
- Heuristic reordering method
  - Deducing reordering rules from the relationship of input characteristics to power consumption.
  - It does not provide the best solution.
  - Suitable for a gate with a large number of transistors.

Activity of an Internal Node

All Possible Input Values				Impact on C_{int}
A_n	B_n	A_{n+1}	B_{n+1}	
0	0	0	0	-
0	0	0	1	Cond. Discharge
0	0	1	0	Cond. Charge
0	0	1	1	Cond. Discharge
0	1	0	0	-
0	1	0	1	-
0	1	1	0	Charge
0	1	1	1	-
1	0	0	0	-
1	0	0	1	Discharge
1	0	1	0	-
1	0	1	1	Discharge
1	1	0	0	-
1	1	0	1	-
1	1	1	0	Charge
1	1	1	1	-



$$P(C_{\text{int}}\, 1 \rightarrow 0) = P(A_1) \cdot P(B_{01}) + P(A_0) \cdot P(B_{01}) \cdot P(C_{\text{int}} : 1)$$

$$P(C_{\text{int}}\, 0 \rightarrow 1) = P(A_1) \cdot P(B_{10}) + P(A_{01}) \cdot P(B_{00}) \cdot P(C_{\text{int}} : 0)$$

Activity of an Internal Node

$$P(C_{\text{int}}\,1 \rightarrow 0) = \underbrace{P(A_1) \cdot P(B_{01})}_{\text{Dominant Factor}} + P(A_0) \cdot P(B_{01}) \cdot P(C_{\text{int}} : 1)$$

$$P(C_{\text{int}}\,0 \rightarrow 1) = \underbrace{P(A_1) \cdot P(B_{10})}_{\text{Dominant Factor}} + P(A_{01}) \cdot P(B_{00}) \cdot P(C_{\text{int}} : 0)$$

- Why is $P(A_1)P(B_{01})$ the dominant factor?
  - In general, the probability of joint events decreases as the number of the individual events increases.
- Heuristic reordering method is used to reduce the dominant factor.

Heuristic Reordering Method

- Objective: minimize $P(A_1)P(B_{01})$
  - Note:
    - A: Placed nearest the output
    - B: Placed nearest the supply node

- Rules for input ordering (transistor ordering):
  - Signals with a high probability of switching are placed nearest the output.
  - Signals with a low probability of switching are placed nearest the supply node.
  - Signals with a high probability of being off are placed nearest the output .
  - Signals with high probability of being on are placed nearest the supply node.

Heuristic Reordering Method

- Note: Input reordering at the circuit level does not have any impact on the switching activity of a logic gate output.

- Efficiency of the heuristic reordering method: an average 10% saving in power was found between the worst and best orderings.