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Low Power Digital System Design

Clock Gating

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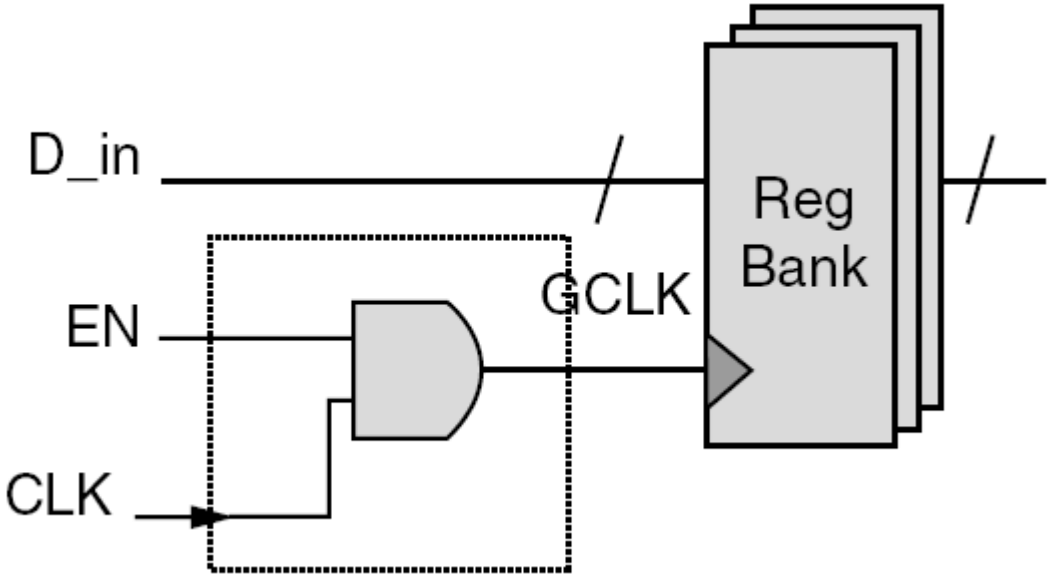
Clock Gating

- Clocks typically consume a large fraction of overall power in synchronous systems (30%–40%).
- Clock transitions initiate signal transitions in combinational logic.

Clock Gating (Cont.)

- Clock gating involves dynamically shutting off the clock to portions of a design that are idle or are not performing useful computation.



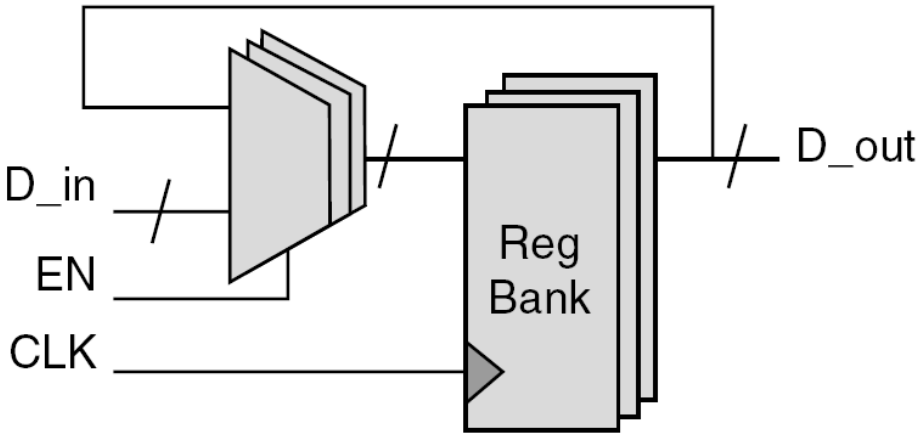
Granularity of the Gated-Clock Blocks

- Module-Level Clock Gating
  - This involves shutting off an entire block or module in the design.
- Register-Level Clock Gating
  - The clock to a single register or set of registers is gated.
- Cell-Level Clock Gating
  - The cell designer usually introduces cell-level clock gating.

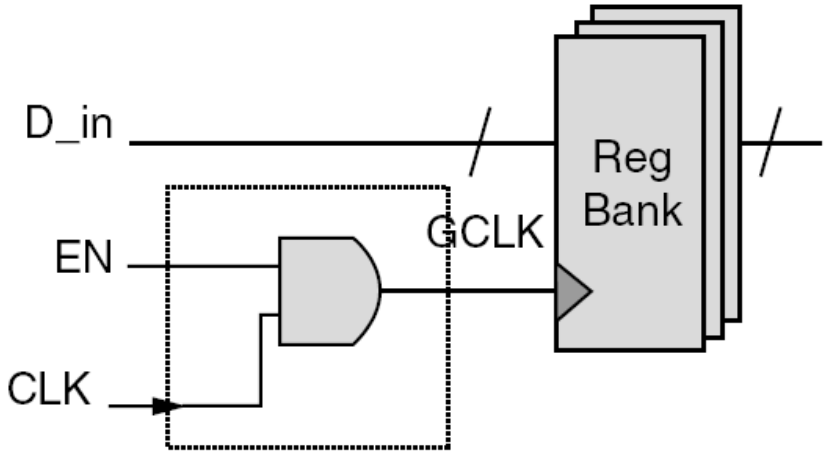
Module-Level Clock Gating

- Usually used by the system or RTL designer.
  - RT-level technique: this kind of clock gating must be incorporated into the RTL code.
- This technique is very effective especially when a block is used only for a specific mode of operation.
- Example:
  - Transceiver: the receiver can be shut off during transmit stages or vice versa.

Register-Level Clock Gating



Traditional Implementation



Clock-gated Implementation

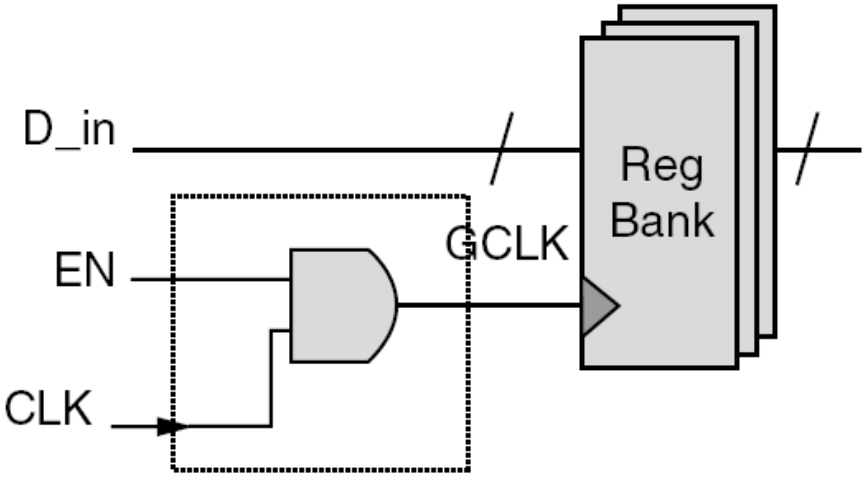
A Comparison Between Clock-Gating Techniques

	Clock Gating	
	Module-Level	**Register-Level**
Power saving per clock-gate	High	Low
Opportunities to shut off clocks	Less	More
Insertion of clock-gates	Human effort	Automated

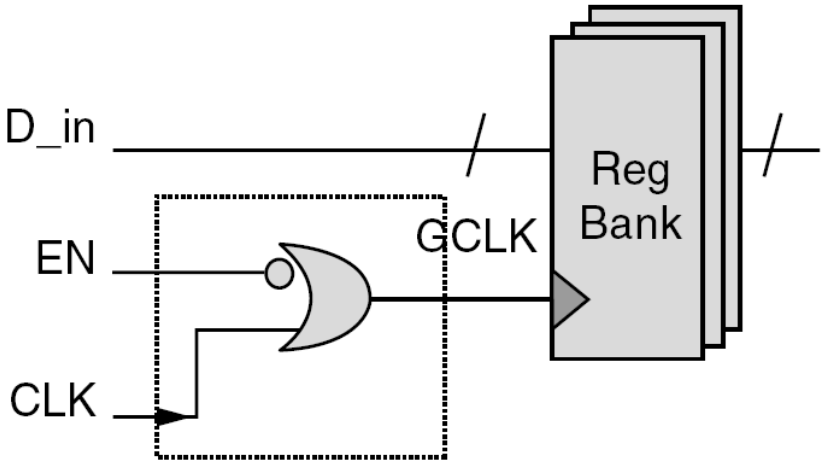
Difficulties in Clock Gating

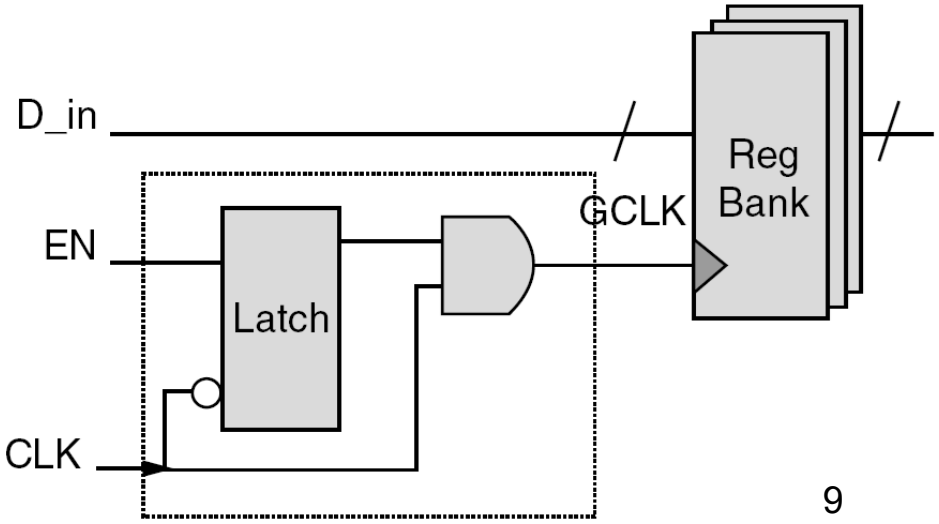
- Clock gating can cause serious clocking problems:
  - Glitches on the enable signal
    - Glitches on FF clock input
  - Clock skew
    - Timing errors

Glitches on the enable signal



- Solutions:



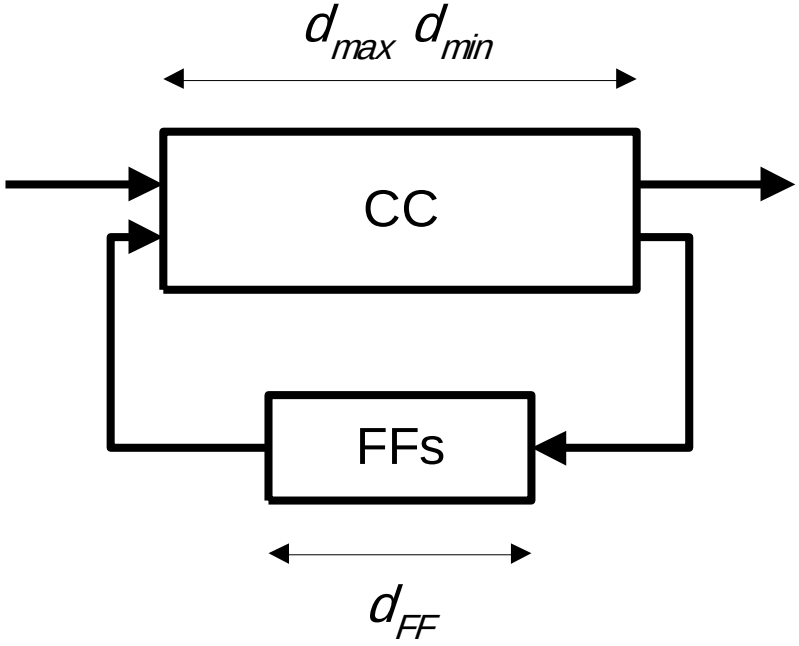


Skew problem in the gate-based architecture

Time constraints (without Skew):

$$d_{FF} + d_{\max} < T - t_S$$

$$d_{FF} + d_{\min} > t_H$$



Time constraints (with Skew):

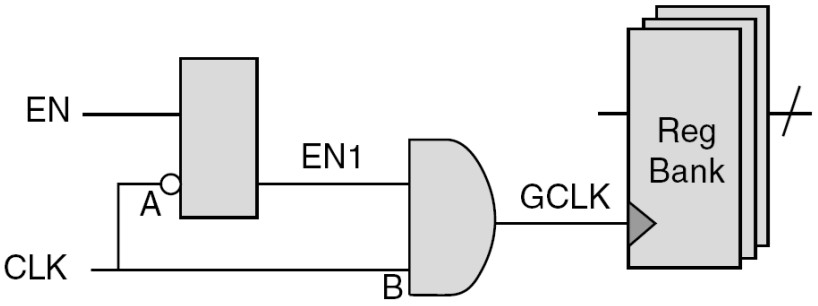
$$d_{FF} + d_{\max} < T - t_S - C_S$$

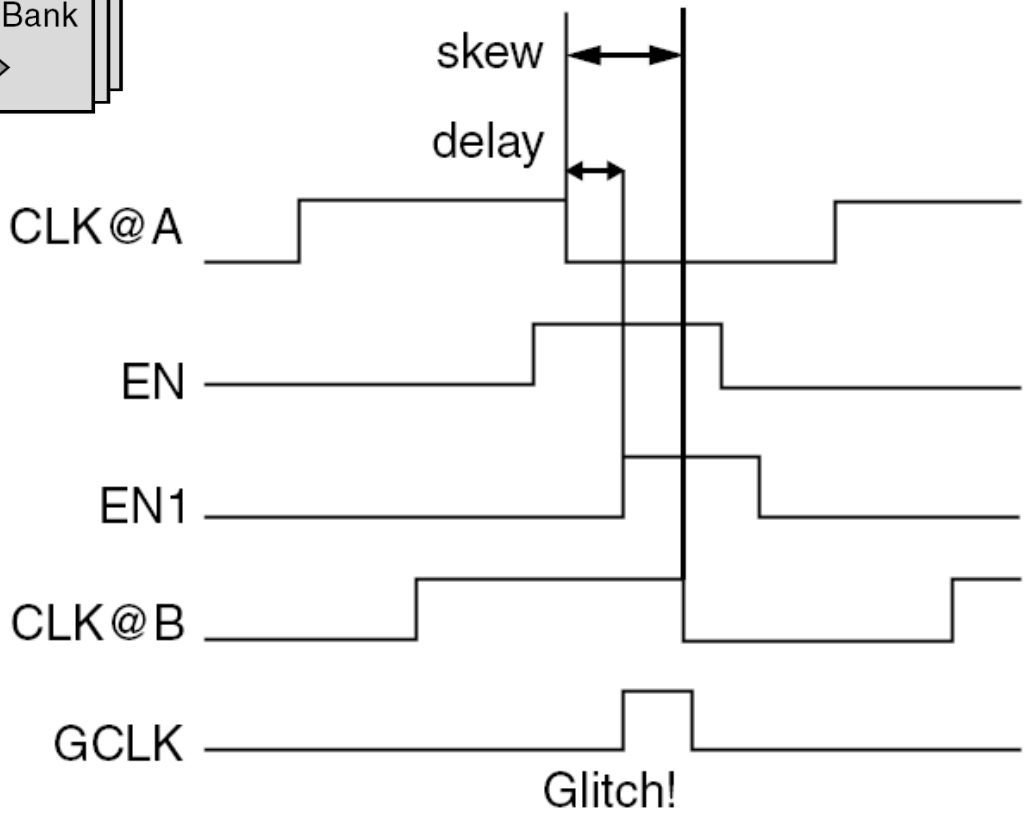
$$d_{FF} + d_{\min} > t_H + C_S$$

t_S= Setup Time
t_H=Hold Time
C_S=Clock Skew

- Clock gating increases C_S.

Skew problem in the latch-based architecture

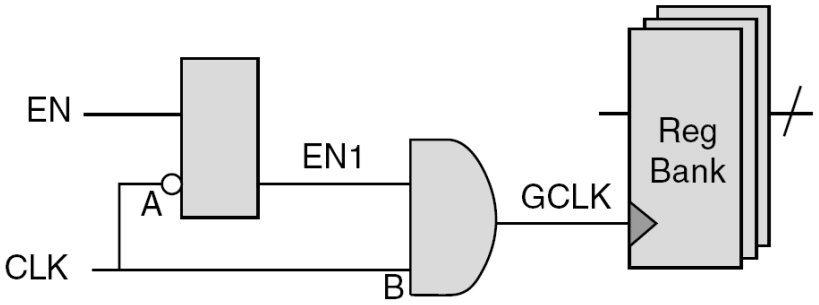


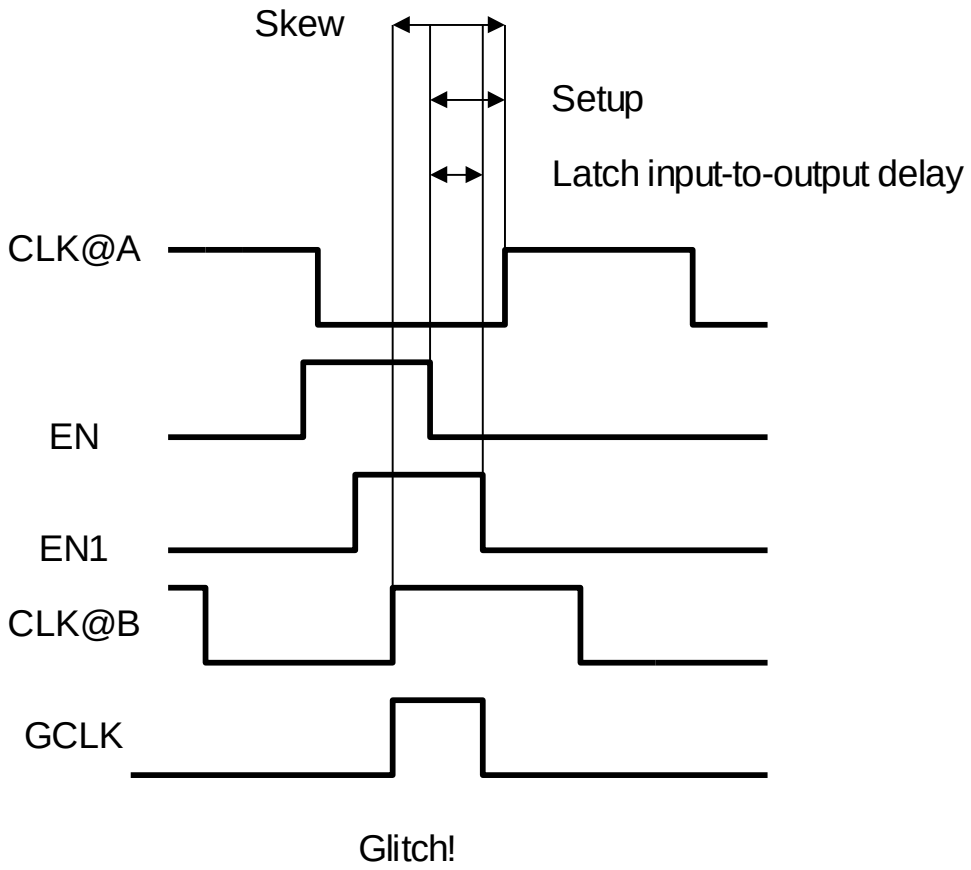


$$C_S < d_{CLK}$$

d_{CLK}= clock-to-output delay of the latch

Skew problem in the latch-based architecture (Cont.)





$$C_S < t_S - d_{in}$$

d_{in}= input-to-output delay of the latch

References

- Bill Moyer, "Low-Power Design for Embedded Processors", *Proceedings of the IEEE*, 2001.
- W.-Z. Shen, et. al., "Transistor Reordering Rules for Power Reduction in CMOS Gates", *ASPDAC*, 1995.
- C. Piguet, *Low-Power CMOS Circuits*, *Technology, Logic Design and CAD Tools*, Chapter 11, 2006.