Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2009-2010

Final Examination - SOLUTION

CLOSED BOOK

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Date: December 17, 2009
Place: Room 3444 Engineering Hall
Time: 10:05 AM - 12:05 PM
Duration: 120 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	Test Economics	8	
2	Modeling and Test Definition	8	
3	Test Generation	15	
4	Testability Analysis	10	
5	Memory Test	10	
6	Full scan	15	
7	Pseudo-exhaustive test	12	
8	BIST	12	
9	Boundary Scan	10	
TOTAL		100	

Name: (Please Print in Capitals)

Last Name: SOLUTION _____

First Name: _____

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam. **Use extra sheets if you need more space to write**

1. (**8 points**) **Test Economics**

   Yield equation used by a fab house is different from those we discussed in class and is given below:

   $$Y = [1 + a(1 - e^{-cf})]^{-b}$$

   In this equation a, b and c are process parameters and f is fault coverage.

   (a) (**4 points**) For the process parameters $a = 1.8$; $b = 0.7$; $c = 2.8$ and fault coverage $f = 90\%$ determine the yield of the process.

   Plug in the values in the equations you obtain Y = 0.5048

   (b) (**4 points**) The definition of yield is the ratio of devices that are tested good to the total number of devices fabricated. Note the devices that are found to be good after testing may include some bad devices in general. However, in the yield equation given above it is assumed that for the fault coverage of 100% the yield will be true yield containing no bad devices. Determine the defect level for the conditions given in part (a) assume that the test is such that it will never fail a good device. Note that defect level is defined as the ratio of potentially bad devices in a batch to the total devices tested good.

   First compute the true yield by setting $f = 100\%$. We obtain $Y_{true} = 0.5001$

   Now we can obtain Defect level DL = (0.5048 - 0.5001)/0.5048 = 0.93% or 9300 ppm

2. (**8 points**) **Modeling the Test Definition**

(a) (**6 points**) BDD representation of a circuit with three inputs, A, B, and C, and one output is given below in Figure 1.

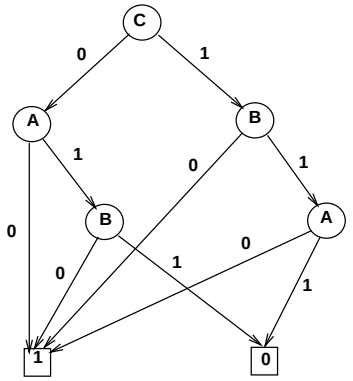

Figure 1: BDD for fault detection.

i. (**2 points**) Will the input A B C = 0 0 0 detect the fault A/1 (input A stuck-at-1) in the realization of the function represented by the above BDD? Explain your answer briefly in the space provided.

It is not a test because the function output in both cases ABC = 0 0 0 and ABC = 1 0 0 is logic 1.

ii. (**4 points**) Find all test vectors that will detect the fault B/1 (input B stuck at 1) in the circuit.

There are two test and these are A B C = 1 0 x

(b) (**2 points**) A vector 0x1x detects a set of faults, say S, in a circuit with four inputs. If the vector 0x11 is simulated on the circuit, will it detect all the faults in S, or will it detect more faults or fewer faults than those in S? Explain your answer.

All faults in S will indeed be detected. It *may* also detect more faults but never fewer faults.

3. (**15 points**) **Test Generation**

Consider the circuit given in Figure 2.

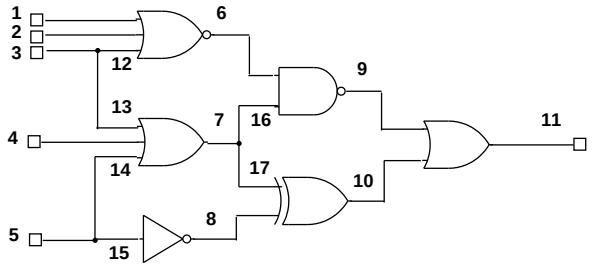

Figure 2: PODEM based test generation.

A test is to be generated for the fault *line 16 stuck-at 0* using a PODEM like test generator. The assignment of PIs and the values to PIs follow the rules given below:

```
The PIs are chosen for assignment in the order 3 5 4 2 1.
Thus if at some stage PIs 3 and 5 have already been
assigned values, then the next PI chosen for assigning a
value is PI 4.

When a back track occurs, always the complimentary value is tried

A 1 is assigned before a 0
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(a) (**10 points**) I have completed the first assignment and its implications. Complete the remaining test generation process.

Objective	Decision	Implication	D-frontier	Comments
16 = 1	3 = 1	6 = 0 7,9,11,12,13,17 = 1 16 = D	-	Fault excited, test not possible backtrack
	3 = 0	-	-	fault not yet excited
16 = 1	5 = 1	8 = 0 7,10,11,14,15,17 = 1 16 = D	9	Fault excited, test not possible backtrack
	5 = 0	14,15 = 0 8 = 1	-	fault not yet excited
16 = 1	4 = 1	10 = 0 7,17 = 1 16 = D	9	Fault excited
6 = 1	2 = 1	6=0, 9,11=1	-	test not possible backtrack
6 = 1	2 = 0	-	9	
6 = 1	1 = 1	6 = 0, 9,11=1	-	test not possible backtrack
6 = 1	1 = 0	6 = 1 9,11 = $\overline{D}$	-	Success

(b) (**3 points**) Draw the decision tree for the above test generation.

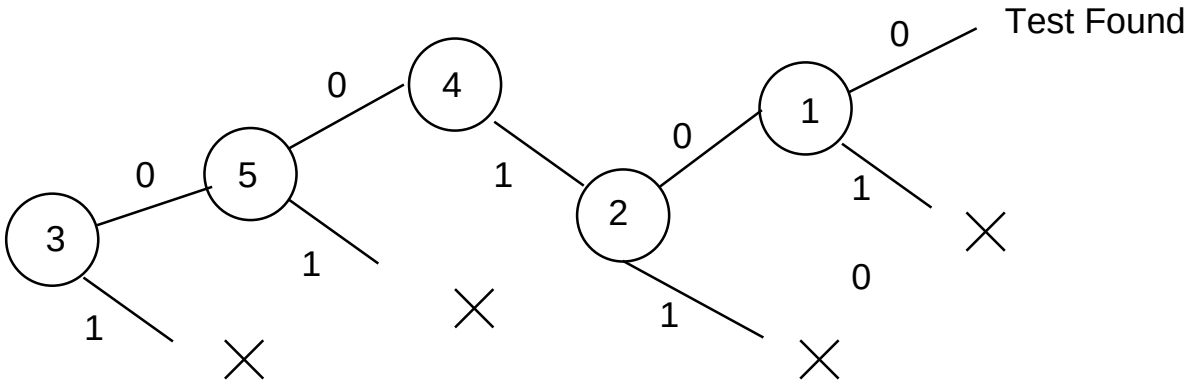

Figure 3: Decision Tree.

(c) (**2 points**) What is the generated test?
Generated test is 1 2 3 4 5 = 0 0 0 1 0

4. (**10 points**) **Testability Analysis**

For the circuit in Figure 4, compute the SCOAP controllability and observability values for each line listed in the table below. I have assigned the CC values to the PIs and CO values to the POs.

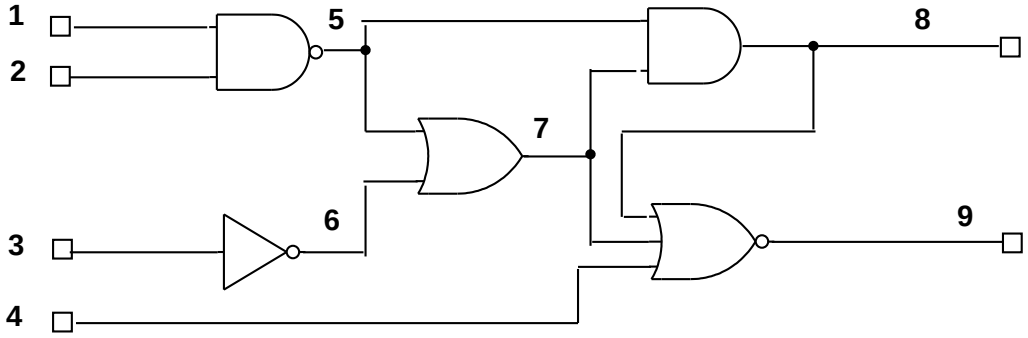

Figure 4: Testability analysis values

Line #	CC0	CC1	CO	Line #	CC0	CC1	CO
1	40	35	75	6	43	12	122
2	23	50	60	7	130	13	35
3	11	42	123	8	87	38	10
4	21	10	233	9	11	239	15
5	86	24	24				

5. (**10 points**) **Memory testing**

A MATS+ test for an n-bit RAM consists of three march elements M1, M2 and M3. The test algorithm is:

$$\underset{\text{M1}}{\{\Uparrow (w1);} \quad \underset{\text{M2}}{\Uparrow (r1, w0);} \quad \underset{\text{M3}}{\Downarrow (r0, w1)\}}$$

While answering the following, identify the march element, the value of i, and the operation. If a fault is not excited or detected by this test, then indicate so.

(a) (**2 points**) Consider the fault: cell 27 stuck-at 0.

i. (**1 points**) When is this fault excited?

The fault is excited in M1. It will again be excited in M3 - which is of no consequence.

ii. (**1 points**) When is this fault detected?

The fault is detected in M2

(b) (**4 points**) Consider a toggle fault between cell 73 and cell 50 such that any transition (up or down) in cell 73 causes the contents of cell 50 to change (complement) its value. Can the above march test detect this fault? If yes in what step and how and if not why not.

This fault may be exited in M1 provided on boot-up the bit 73 has a value 0 in it. In such a case the fault will be detected in M2.

However, if the bit 73 on startup has a value 1 in it, the fault will be excited in M2 and then again in M3 before cell 50 is read, therefore the fault will be masked and will not be detected.

Therefore, this fault is at best a **potential detect** fault with this algorithm.

(c) (**4 points**) Consider a toggle fault between cell 35 and cell 150 such that a transition (up or down) in cell 35 causes the contents of cell 150 to change (complement) its value.

i. (**2 points**) When is this fault excited?

The fault will be excited in M2

ii. (**2 points**) When is this fault detected?

It will be detected in M2

6. (**15 points**) **Full Scan**

Block diagram level description of an embedded circuit is shown in Figure 5. The R's are registers consisting of flip-flops, and CL's are combinational logic blocks. A scan path, to test the combinational logic blocks shown in the figure, is also identified. The number of inputs and outputs of each combinational block are also shown in the figure.

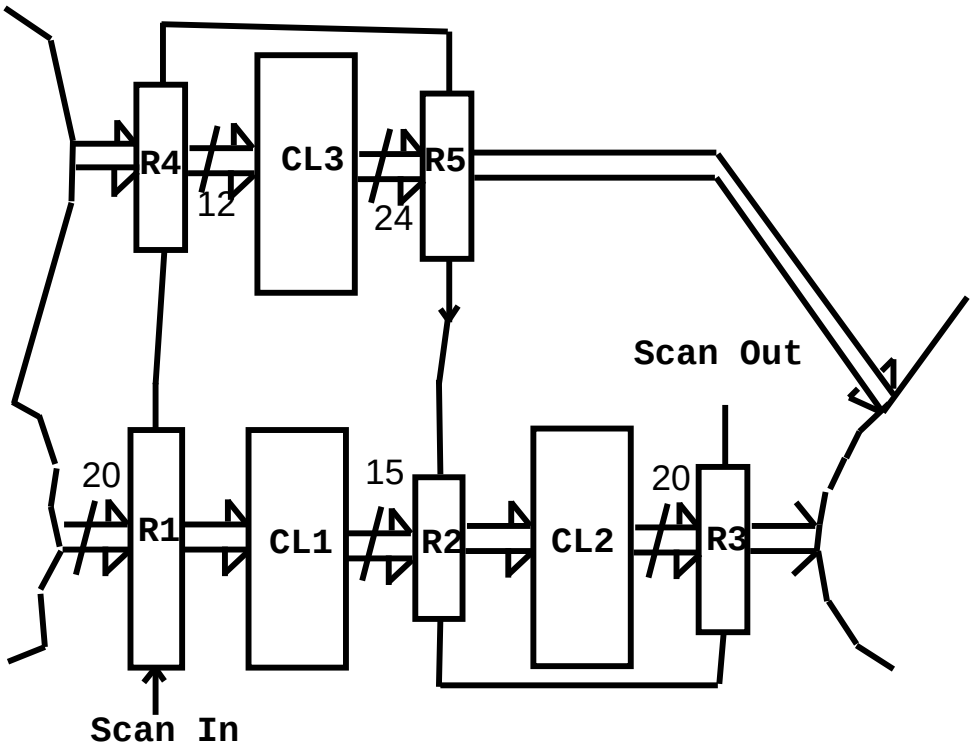

Figure 5: Circuit with Full Scan.

Now answer the following:

(a) (**1 points**) How many scan clocks will it take to scan-in one test vector for testing the combinational block CL1.

20 Clocks

(b) (**1 points**) How many scan clocks will it take to scan-in one test vector for testing the complete circuit (all three combinational blocks.)

Length of registers R1, R4, R5, and R2. Note we need not scan in R3. Hence it is 71 Clocks

(c) (**1 points**) How many scan clocks will it take to scan-out the results of one test vector applied to the combinational block CL3.

We need to scan out R5 - hence 24+15+20 = 59 Clocks

(d) (**1 points**) How many scan clocks will it take to scan-out the results of one test vector applied to the complete circuit.

In this case R1 and R4 need not be scanned out. Hence 59 Clocks

(e) (**4 points**) Assuming that the number of tests to test each combinational block are 30, determine the the total number of clocks (scan clocks and system clocks) required to apply all tests using scan testing. You must include a brief explanation for your answer.

Scan in needs 71 Clocks. Scan out needs 59 Clocks. To overlap these must used 71 Clocks but overlap is not needed for the last vectors. Hence the total Clocks are:
30(71+1) + 59 = 2219 Clocks

(f) (**7 points**) Now assume that the number of tests required to test CL1 is 100 while CL2 and CL3 can be tested using only 30 test vectors each. Devise a scan based test strategy to completely test this circuit in as few clock cycles as possible. List the number of clock cycles required to test the circuit using your strategy.

For the first 30 vectors we use the approach as if testing full circuit. Though 30th vector will be scanned out in 59 Clocks. After these 30 vectors, CL2 and CL3 are tested. Now to text CL1 we need scan in of 20 clocks and scan out of 35 clocks. Hence overlap will require 35 Clocks.
Thus total clocks = 30(71+1) + 59 + 1 + 69(35+1) + 35 = 4739 Clocks

7. (**12 points**) **Pseudo-exhaustive testing**

Consider the combinational circuit shown in Figure 6

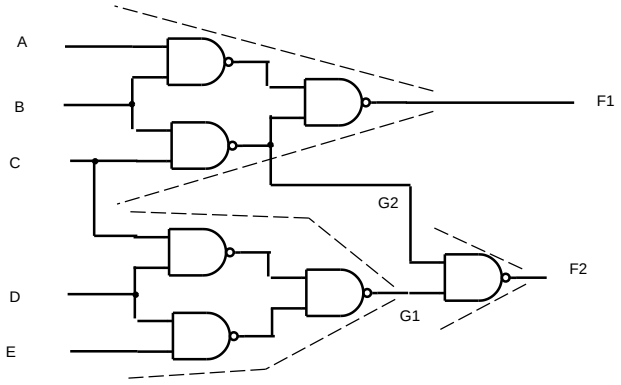

Figure 6: Circuit for pseudo-exhaustive testing.

(a) (**2 points**) What is the size of exhaustive test to test this circuit.
32 vectors

(b) (**3 points**) What is the size of minimum pseudo-exhaustive test to test this circuit using partitions consisting of cones behind the outputs F1 and F2 (note that these cones are NOT shown in the figure).
F1 depends on 3 inputs, F2 depends on 4 inputs. The max in this case is 16 (F1 can fully overlap testing F2)

(c) (**7 points**) Derive a minimum pseudo-exhaustive test set using sensitized partitioning for the circuit partitions shown in the figure. For your convenience the exhaustive test for the partition F1 with inputs A, B, C is already shown in the table below.

A	B	C	D	E	G1	G2	F1	F2
0	0	0	0	0	0	1	0	
0	0	1	0	0	0	1	0	
0	1	0	0	1	0	1	0	
0	1	1	0	x	0	0	1	
1	0	0	1	0	0	1	0	
1	0	1	0	1	0	1	0	
1	1	0	1	1	1	1	1	
1	1	1	1	x	1	0	1	
0	0	1	1	0		1		
0	0	1	1	1		1		

8. (**12 points**) **BIST**

(a) (**6 points**) Consider the characteristic polynomial given below and answer each of the following questions.

$$F(x) = x^5 + x^2 + x + 1$$

i. (**3 points**) Give the standard (external EOR) LFSR realization of this polynomial.

Label the 5 FFs from left to right as x4, x3, x2, x1, x0. Now tap the outputs of x0, x1, and x2 - EOR them and feed that to the input of x4

ii. (**3 points**) Give the modular (internal EOR) LFSR realization of this polynomial.

Label the 5 FFs from left to right as x0, x1, x2, x3, x4. Now insert the EORs at the inputs of FF x1 and x2. Feed the output of x4 to in input of x0 and to the two EORs.

(b) (**3 points**) Does the polynomial $x^2 + x + 1$ divide the polynomial $x^9 + x^6 + x + 1$? Show your work and write the quotient and the remainder.

The quotient will be $x^7 + x^6$ and remainder will be $x + 1$

(c) (**3 points**) Consider the companion matrix of some 3-bit LFSR given below. Find its characteristic polynomial.

$$\begin{bmatrix} X_0(t+1) \\ X_1(t+1) \\ X_2(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_0(t) \\ X_1(t) \\ X_2(t) \end{bmatrix}$$

The characteristic polynomial is $x^3 + 1$.

9. (**10 points**) **Boundary scan and general problems**

   (a) (**3 points**) Name the five IEEE 1149.1 (Boundary Scan Standard) interface signals?

   Five interface signals are:
   TMS - Test Mode Select
   TCKL - Test Clock
   TDI - Test Data Input
   TDO - Test Data Output
   TRST - Test Reset - this is an optional signal

   (b) (**3 points**) Describe the function of any two of these IEEE 1149.1 interface signals?

   evident from the names of the signal and often discussed.

   (c) (**2 points**) Why does boundary scan standard insist on having its own clock signal instead of using the system clock signal that may already be available.

   Several reasons: tester does not have to conform to the system/device clock frequency, clock synchronization problems are avoided, boundary scan glitches avoided in the boundary scan design.

   (d) (**2 points**) Two of the required "test data registers" in boundary scan are "boundary scan register" and "bypass register". However. there is no limit on "optional test data registers". Suggest two possible "optional test data registers" that may be useful and suggest their usefulness.

   Device ID register
   Manufacturer ID
   Design version and design related information
   Information about test and design features