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Embedded System Design

Energy Management (17)

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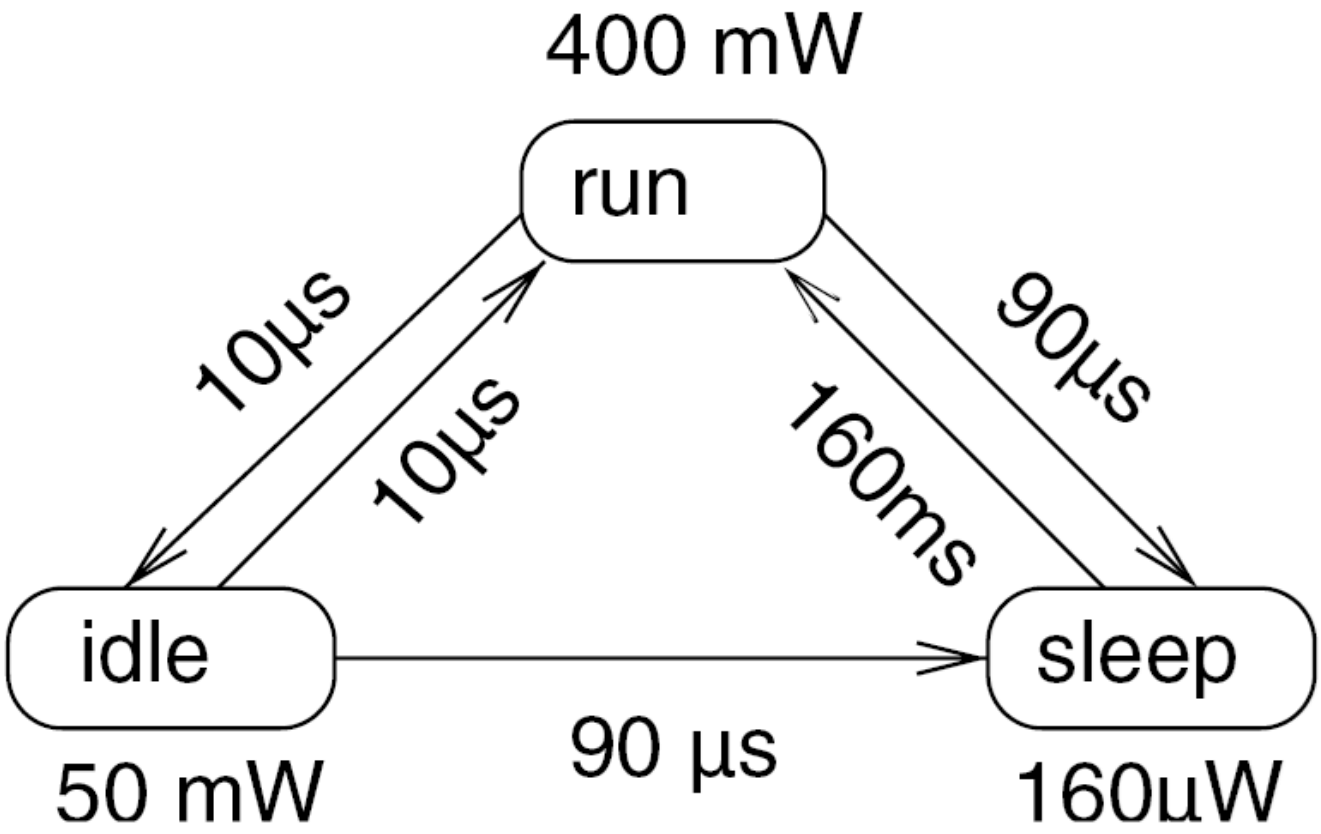
Dynamic Power Management

- **Main Idea: the shutdown of idle system components.**
- **An advantage of DPM is its generality, which allows its usage not only for digital circuitry, but also for other system components such as displays, and hard drives.**

Example: StrongArm SA 1100



Example: StrongArm SA 1100

- The processor is fully operational in the run state.
- In the idle state, it is just monitoring the interrupt inputs.
  - reactive nature of ES
- In the sleep state, all on-chip activity is shutdown.

DVS-Enabled Processors

- **DVS-enabled processors have the ability to dynamically change their supply voltage and operational frequency settings during run-time of the application.**

$$P_{SW} = \alpha C_L V_{DD}^2 f \qquad Delay \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

Example 1: Crusoe Processor

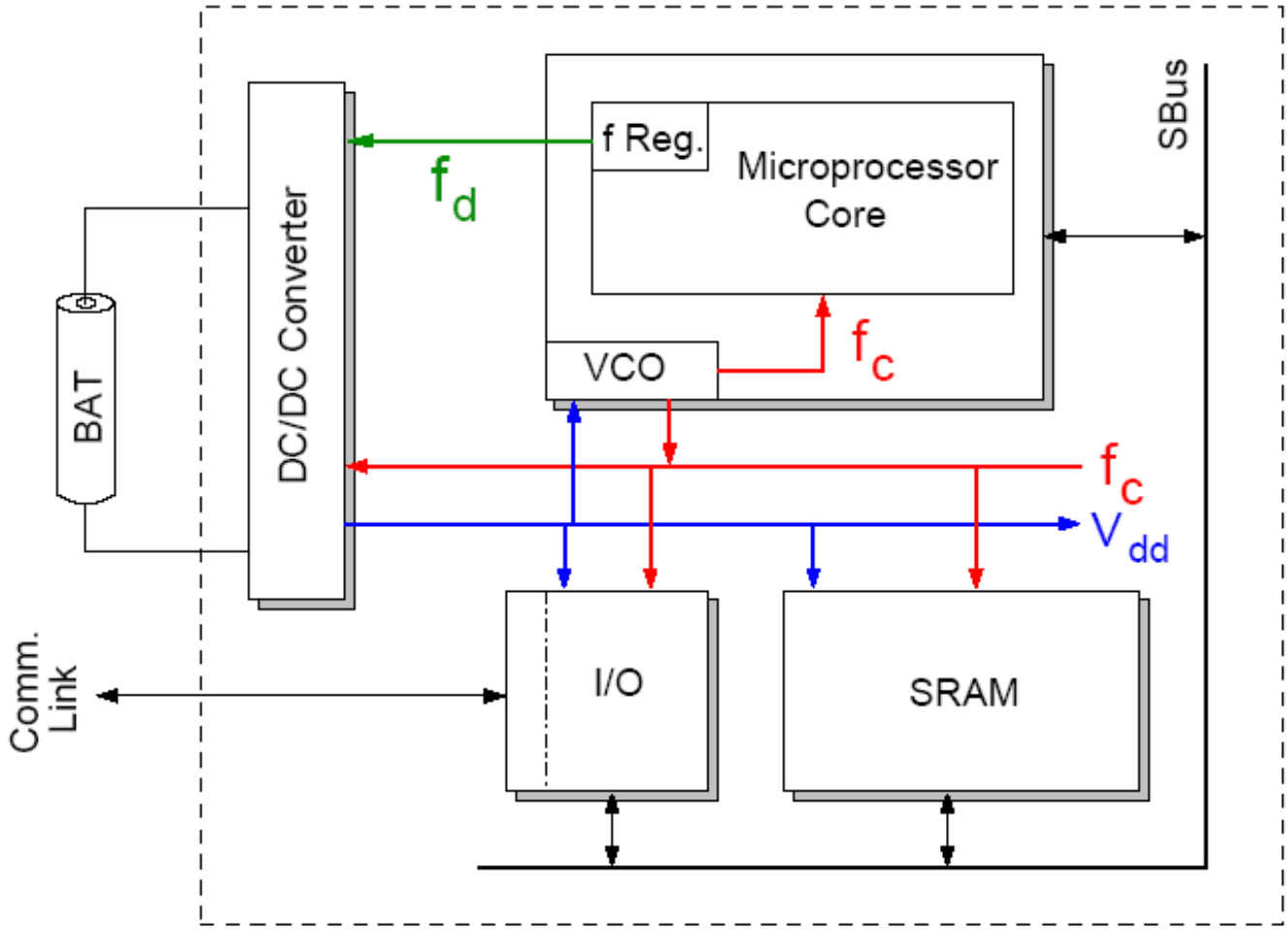
- By Transmeta
- 32 voltage levels between 1.1 and 1.6 volts
- Clock can be varied between 200 MHz and 700 MHz in increments of 33 MHz
- Transitions from one voltage/frequency pair to the next takes about 20 ms.

Example 2: Mobile Pentium III

- **Two different speed/voltage pairs are provided**
- **Intel SpeedStep Technology**

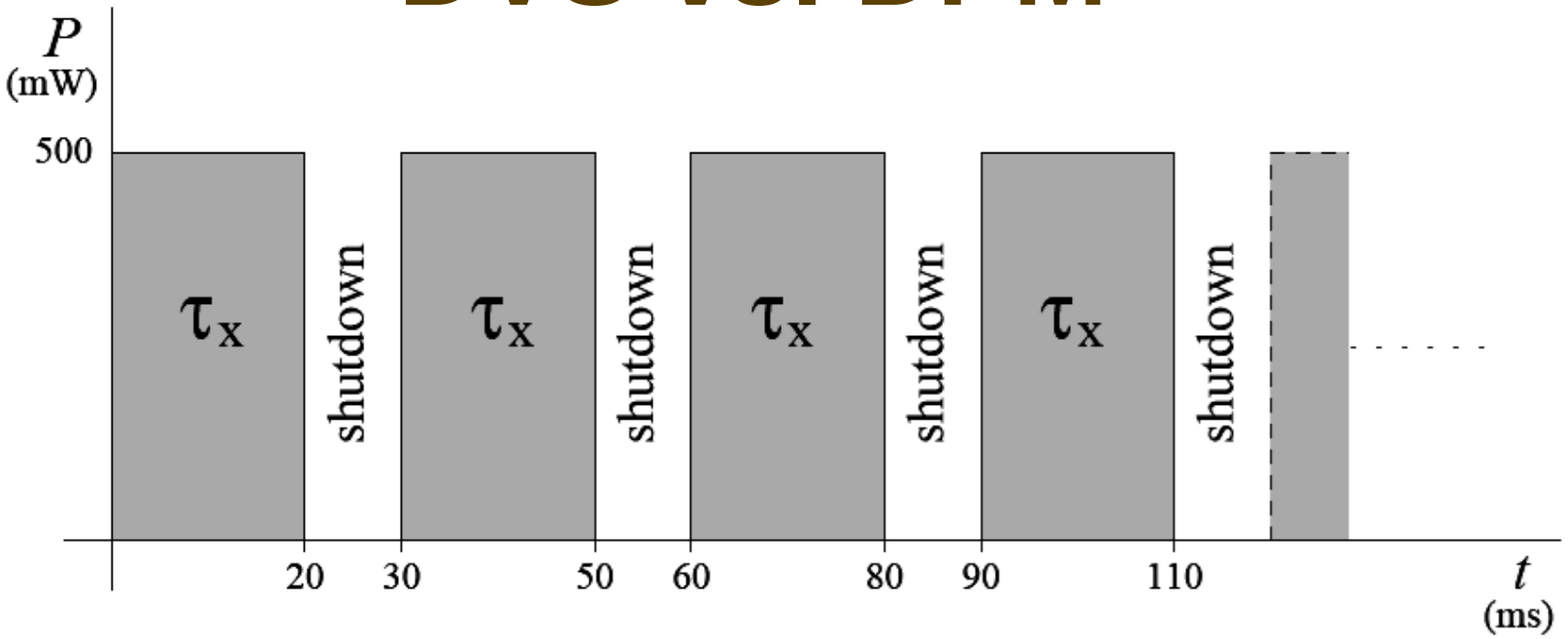
DVS-Enabled Processors

$$f \propto V_{DD}$$



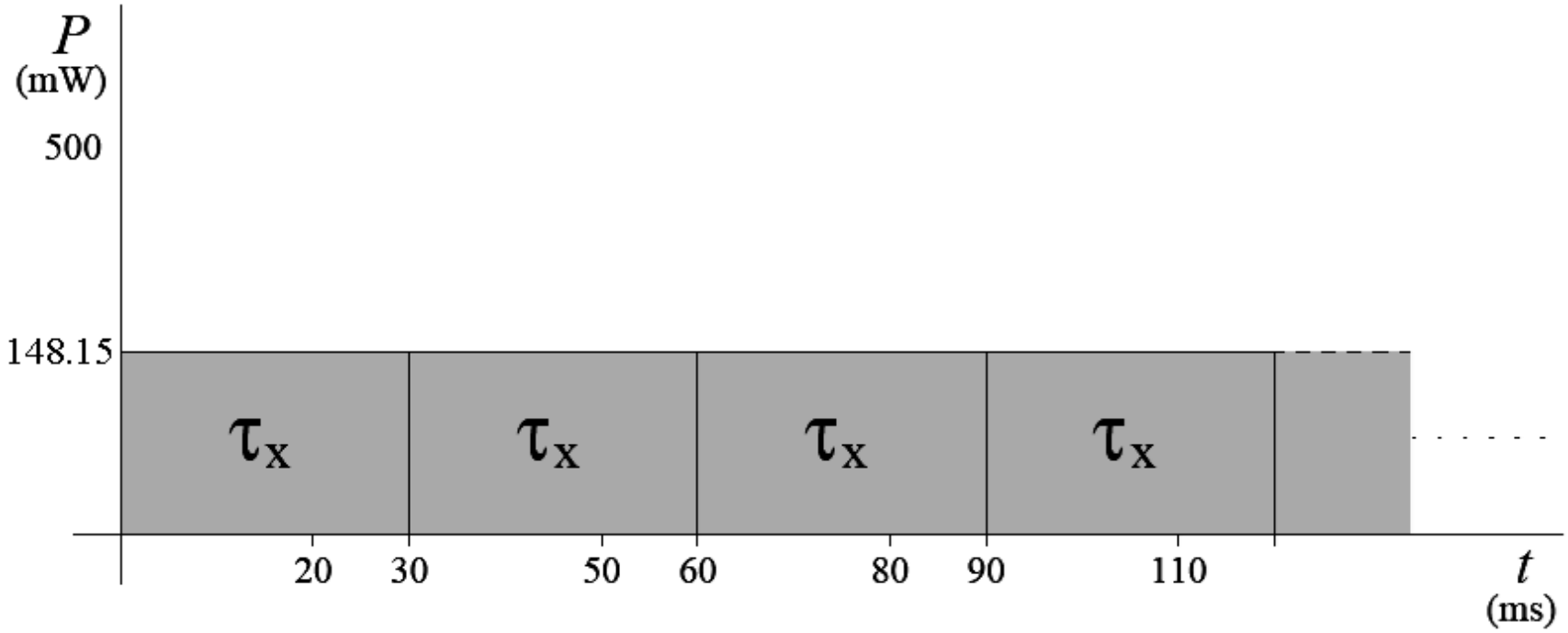
- VCO: voltage controlled oscillator
- Note that the frequency register is under software control.

DVS vs. DPM



- **Example:**
  - **DPM**
    - **Execution time= 20 ms**
    - ***F*= 33MHz, *Vdd*= 3.3V**
    - **Power dissipation = 500 mW**
    - **P_{AV}=(2/3)*500 mW= 333.333 mW**
    - **Period= 30 ms**

DVS vs. DPM



- **Example:**
  - **DVS**
    - **Execution time= 20 ms -> 30 ms**
    - ***F*= 33MHz -> 22MHz, *Vdd*= 3.3V -> 2.2V**
    - **Power dissipation = 500 mW -> $(2/3)^3$*500 mW =148.15mW = P_{AV}**
    - **Period= 30 ms**

Single Event Upsets (SEU)

- **Bit-flips due to the impact of particles on flip-flops.**

$$\lambda_{SEU} \propto \exp(-Q_{CRIT})$$

$$Q_{CRIT} = V_{DD}.C_L$$

- **DVS has a negative impact on SEU rate**