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Low Power Digital System Design

Gate-Level Techniques (Cont.)

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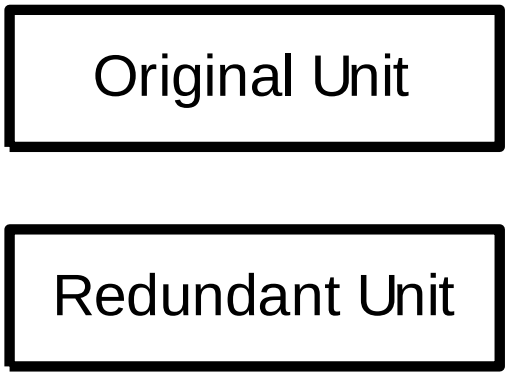
Concurrency and Redundancy

- Basic Idea: Using concurrency and redundancy to improve performance and then to trade this performance for lower power by reducing the voltage supply.
- This technique can be used at any level of abstraction.

$$P_{SW} = \alpha C_L V_{DD}^2 f$$



$$P'_{SW} = 2 \times [\alpha C_L (\frac{V_{DD}}{2})^2 \frac{f}{2}] = \frac{P_{SW}}{4}$$

Impact of Supply Voltage on *PDP*

$$PDP = P_{SW} \times delay = \alpha C_L V_{DD}^2 f \times \frac{1}{f} = \alpha C_L V_{DD}^2$$

$$V_{DD} \downarrow \Rightarrow PDP \downarrow$$

- As V_{DD} decreases *PDP* decreases quadratically.
- Note that *PDP* can be interpreted as “Energy per Cycle” (Energy per Result).

Concurrency and Redundancy at the Gate-Level

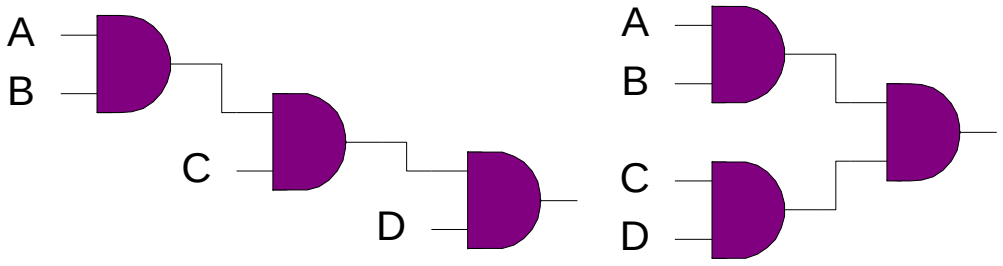
- From a performance point of view:
  - It is not beneficial to improve the speed of the circuit part off the critical path.

- From a power consumption point of view:
  - It is quite beneficial to improve the speed of the circuit part off the critical path and then trade this speed for lower power: (Dual V_{DD})

Concurrency and Redundancy at the Gate-Level (Cont.)

- Two-step technique:
  - Reduce the circuit depth (Concurrency).
    - This can result in increased number of gates (Redundancy)
  - Apply the Dual V_{DD} technique to the circuit.

- Note: Concurrency is desirable but redundancy is not desirable. Sometimes, we can increase the concurrency without incurring any redundancy.
  - Example:

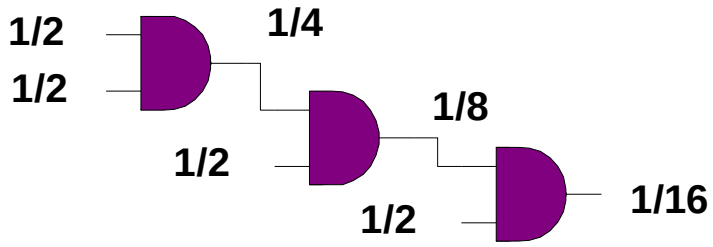


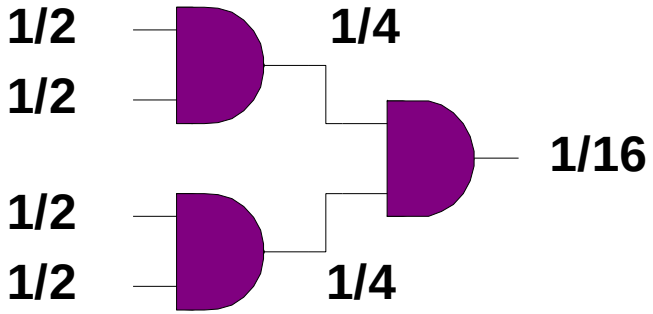
Redundancy: The Penalty for Using Concurrency

- In the concurrency and redundancy technique, redundancy usually refers to hardware redundancy.
  - Area penalty, which in turn results in an increase in power dissipation.
- However careful consideration must be given to other types of penalties.
  - Example: increase in switching activity.
- Solution: The concept of effective capacitance

Example: Other types of penalties

- In this example, the penalty for using concurrency is not a redundant hardware, rather it is an increase in switching activity.





Switching Activity=347/256

Switching Activity=367/256

$$P_{SW} = \frac{347}{256} C_L V_{DD}^2 f$$

$$P'_{SW} = \frac{367}{256} C_L (\frac{2}{3} V_{DD})^2 \frac{2f}{3} \cong 0.31 P_{SW}$$

Effective Capacitance

- Effective capacitance represents the average capacitance switched every clock cycle.
  - Effective capacitance = Switched capacitance=C_{eff}

$$P_{SW} = C_{eff} V_{DD}^2 f \qquad C_{eff} = \alpha C_L$$

- Any increase in effective capacitance can be considered as redundancy.