Sharif University of Technology
Department of Computer Engineering

Low Power Digital System Design

Gate-Level Techniques

A. Ejlali

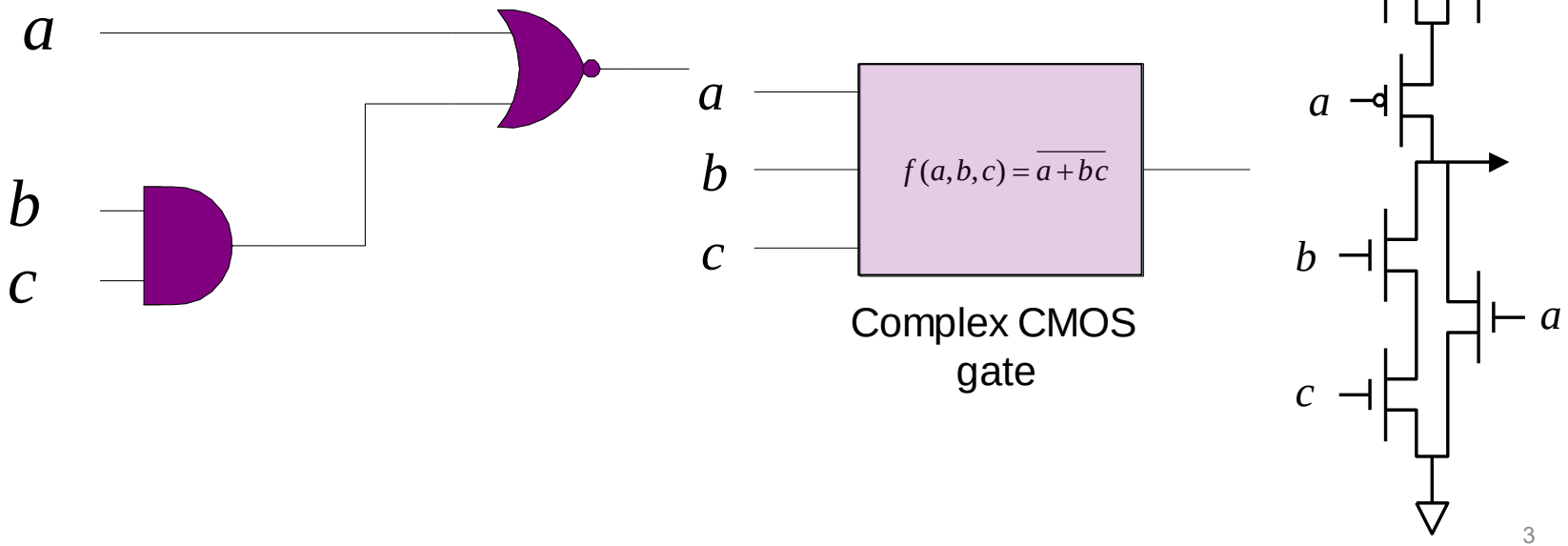
Gate-Level LPD Techniques

- Technology Decomposition and Mapping
- Activity Postponement
- Glitch Reduction
- Concurrency and Redundancy

Technology Decomposition and Mapping

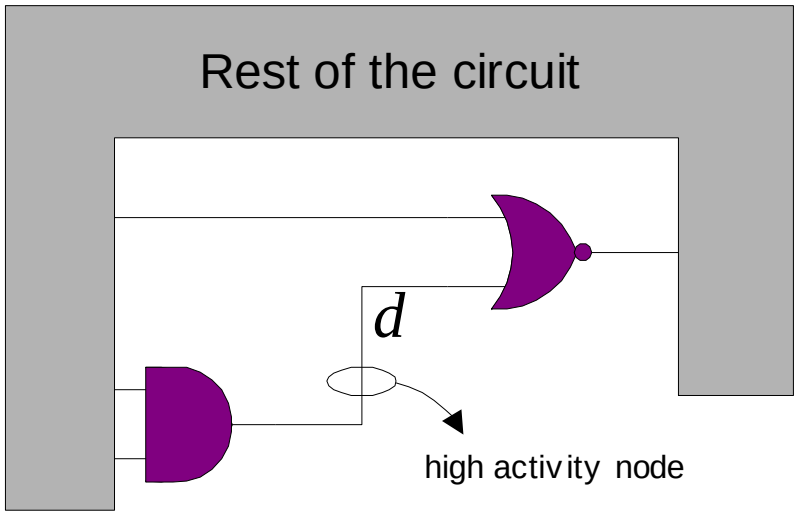
- Realization of Boolean Functions
  - Switch-Level: Results in complex CMOS gates
  - Gate-Level: Results in networks of simple CMOS gates
- Example:

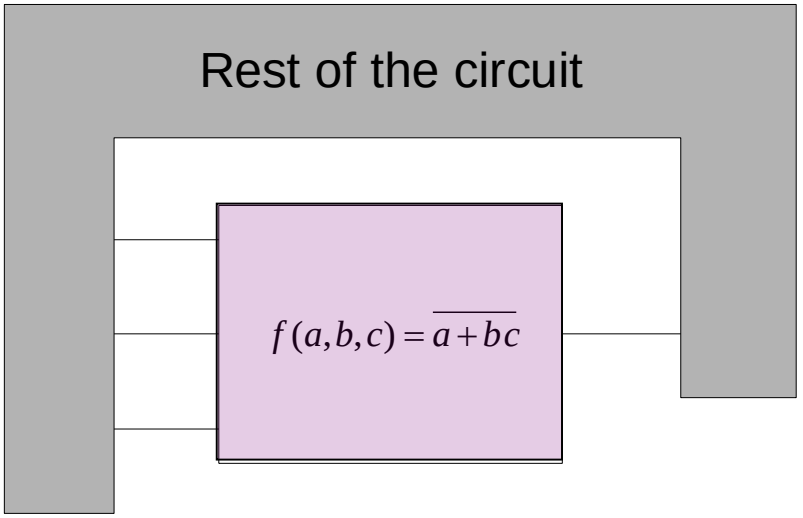
$$f(a,b,c) = \overline{a + bc}$$



Technology Decomposition and Mapping

- Main Idea: hide high activity nodes inside complex CMOS gates.
- Example:

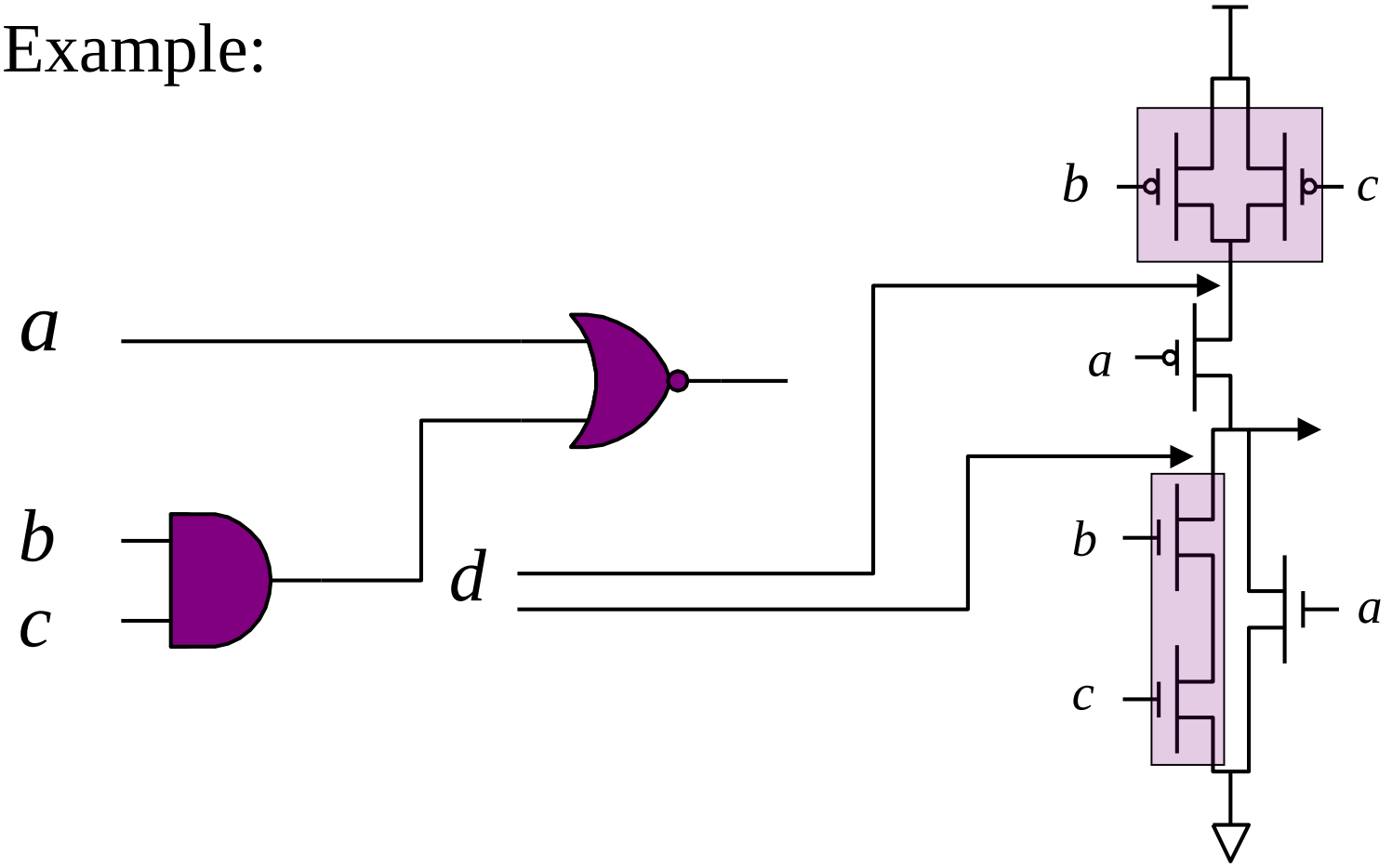




d is hidden inside a complex gate

Technology Decomposition and Mapping

- Rapidly switching signals are mapped to the low capacitance internal nodes.
- Example:



Technology Decomposition and Mapping
Impact on Performance

- Making a gate too complex can slow the circuit, resulting in a trade-off of performance for power.
  - Stacked transistors in the gates with large C_L
  - Decreased concurrency

- Solution: Be careful of the circuit critical path.

Estimation of Transition Probabilities

- Analytical Techniques
  - Certain kinds of input distributions
  - Re-convergent Fan-out Problem
- Circuit Simulation
  - Time-consuming
  - Realistic input stimulus

Calculation of Probabilities

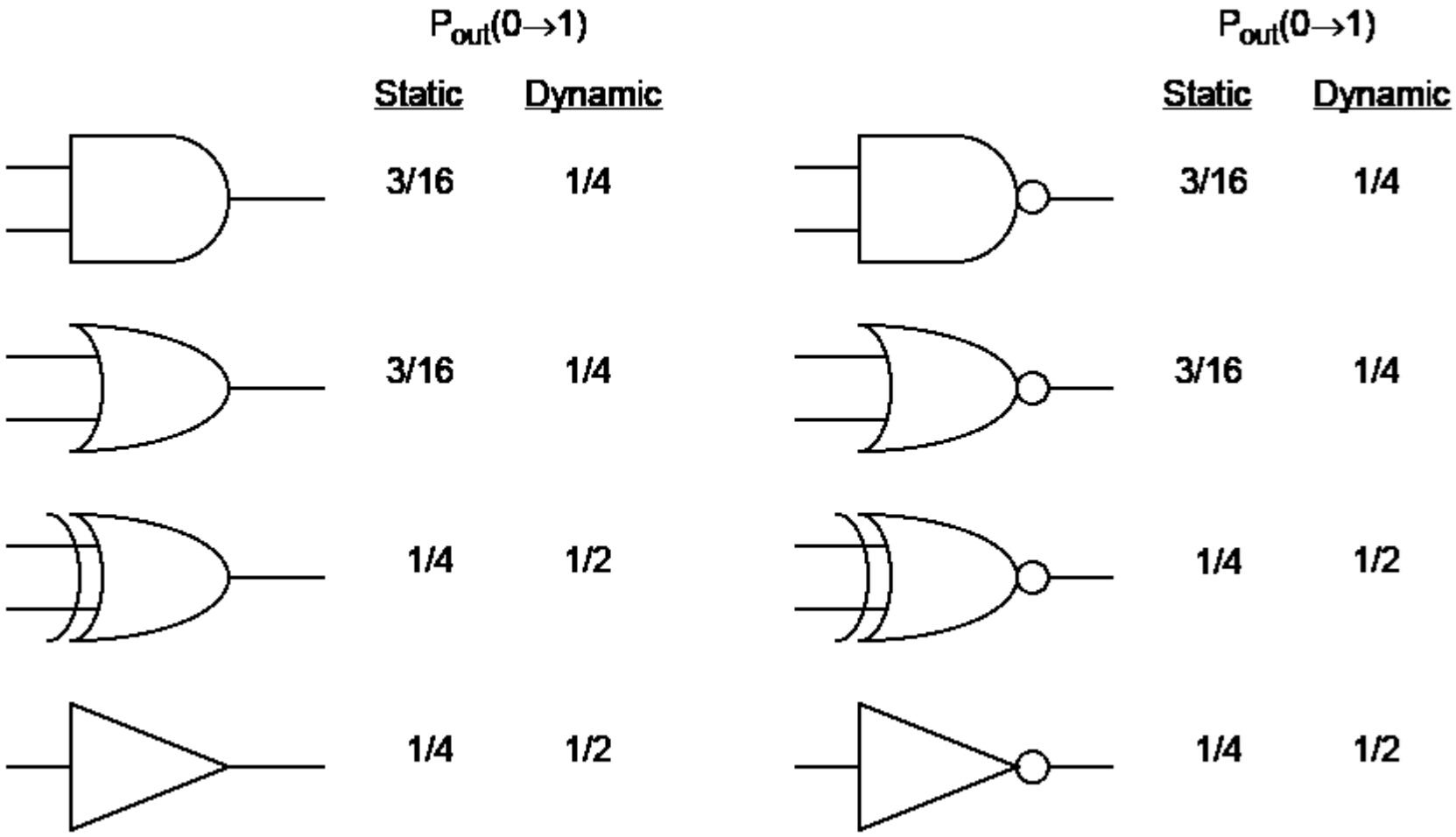
- Zero delay model (ignore glitching)
- Primary inputs are uncorrelated
- Present input value is independent of the previous value

$$P(W_{0\to1}) = P(W_{1\to0}) = P(W_0) \cdot P(W_1)$$

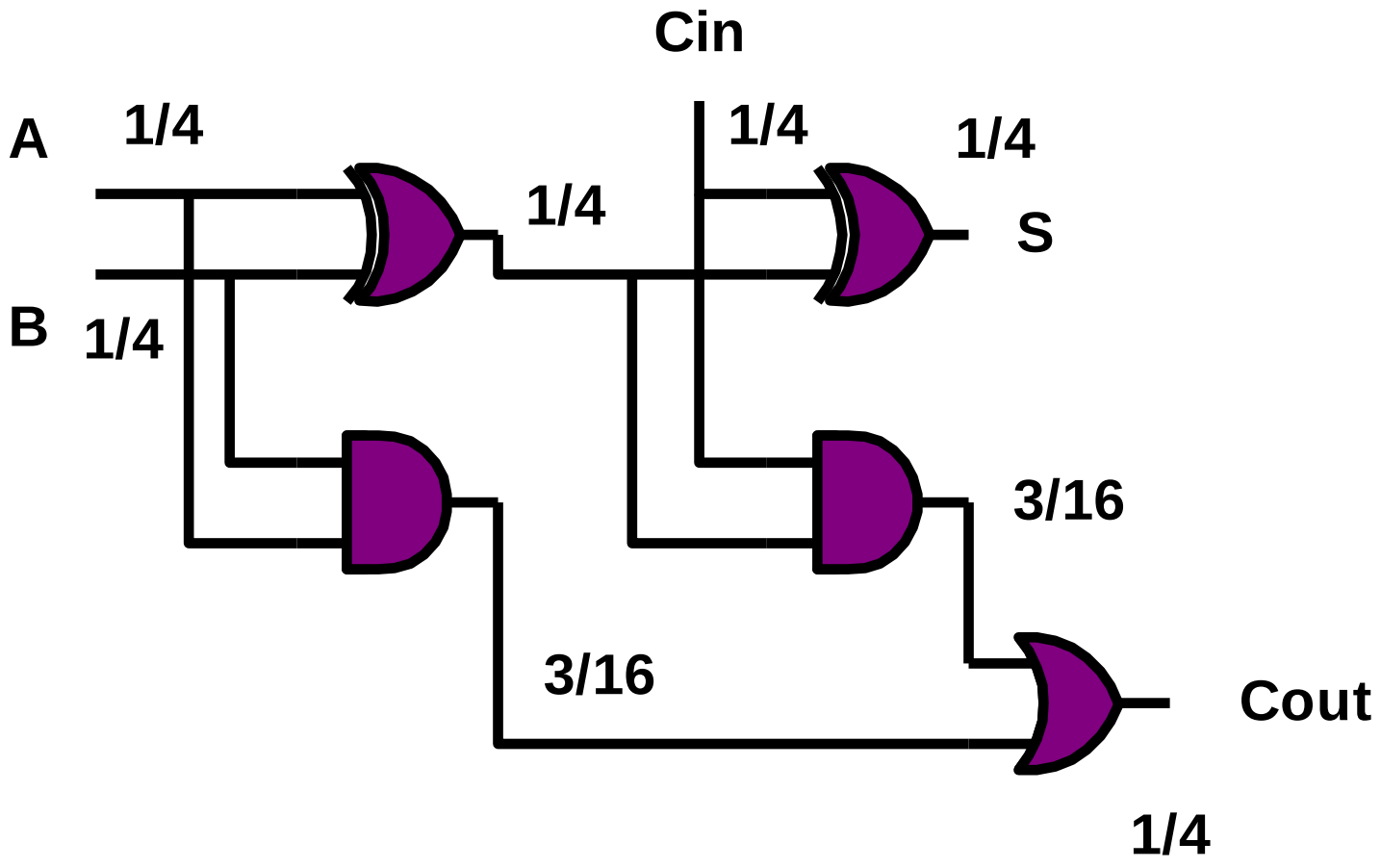
- Note:
  - This equation is independent of circuit topology (re-convergent fan-outs).
  - The above equation is valid for static CMOS style. For dynamic CMOS style we can write:

$$P(W_{0\to1}) = P(W_1)$$

Output activities for static and dynamic CMOS styles



Example: FA Unit (Static CMOS)



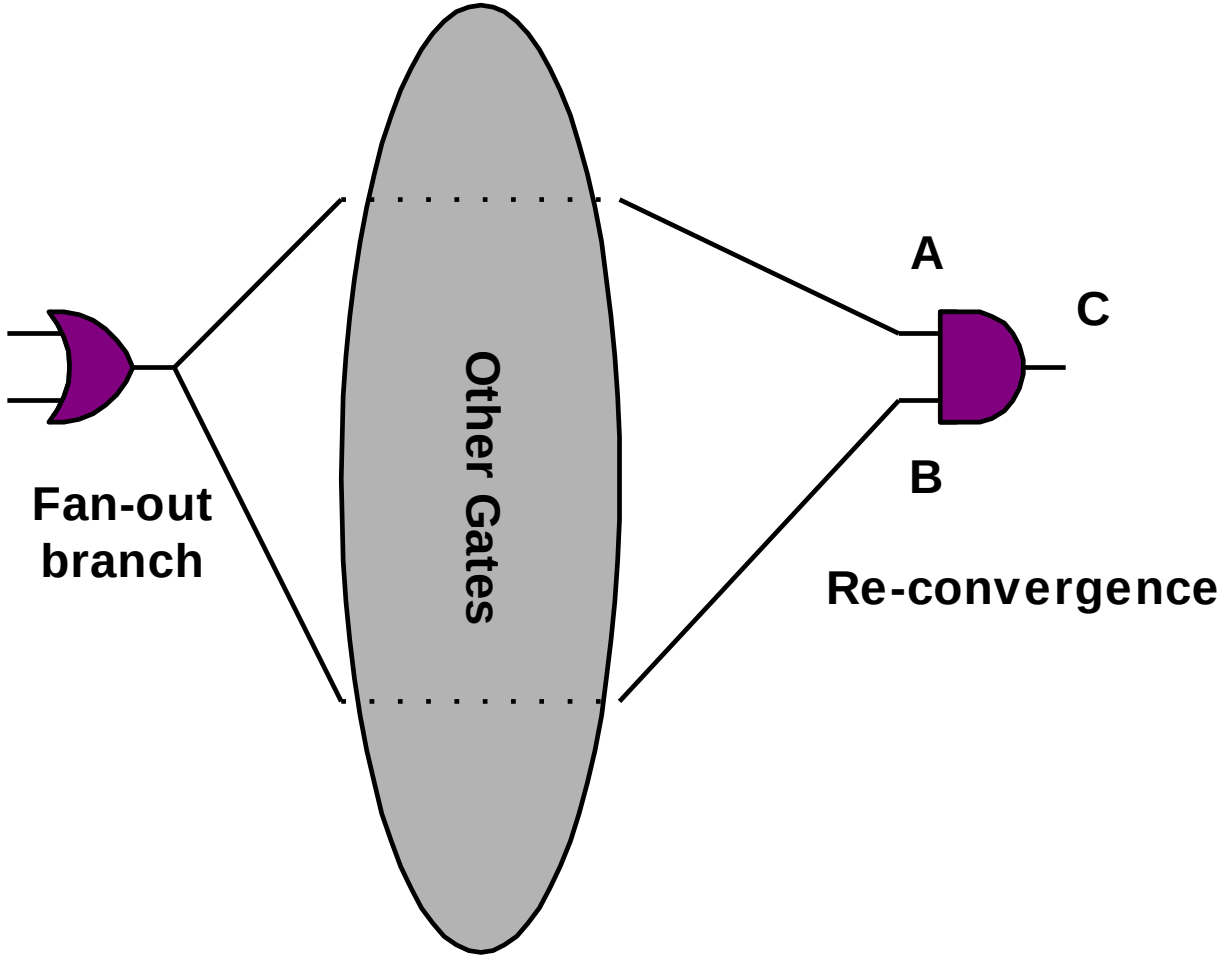
- Hint: The signal activity can be easily obtained from its truth table.

Probability Propagation

	$P_{0\rightarrow 1}$
AND	$(1-P_A P_B)P_A P_B$
OR	$(1-P_A)(1-P_B)(1-(1-P_A)(1-P_B))$
EXOR	$(1 - (P_A + P_B - 2P_A P_B))(P_A + P_B - 2P_A P_B)$

- Assumption: Independence of input probabilities.
- Main Problem: Re-convergent Fan-outs cause cross-correlation between the inputs of a gate.

Re-convergent Fan-out



$P(C=1)=P(A=1).P(B=1|A=1)=P(B=1).P(A=1|B=1)$

Note: The truth table technique is still applicable