Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2009-2010

Midterm Examination

CLOSED BOOK

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Date: November 9, 2009
Place: Room 1164 Mechanical Engineering (In Class)
Time: 7:15 - 8:30 PM
Duration: 75 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	General Questions	14	
2	Test Economics	14	
3	Modeling	12	
4	Fault Simulation	14	
5	SCOAP Computation	18	
6	Test Generation	12	
7	Checking Seq	16	
TOTAL		100	

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam.

Last Name (Please print): _____
First Name: _____
ID Number: _____

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1. (**14 points**) **General Questions**

   Answer the following in brief and to the point. You must not use more than two to three lines of explanation where an an explanation is needed.

   (a) (**1.5 points**) Memory usage by a concurrent fault simulator is smaller than the memory usage by a deductive fault simulator. Answer True of False.

   (b) (**1.5 points**) Memory usage by a serial fault simulator is smaller that the memory usage by a deductive fault simulator. Answer True or False.

   (c) (**3 point**) A gate level fanout-free realization of a circuit has 20 inputs and 2 outputs. What is the maximum number of tests we will need to test this circuit. Hint: think checkpoints.

   (d) (**2 points**) If a fault f_1 dominates fault f_2, and the fault f_2 dominates a fault f_3. which of these faults can be deleted to reduce the fault list for fault detection. Give reason.

   (e) (**1.5 points**) Method of Boolean Difference can be used to determine if a fault in a combinational circuit is redundant. Answer True or False.

   (f) (**1.5 points**) Simulation based test generation can be used to identify if a fault in a sequential circuit is redundant. Answer True or False.

   (g) (**1.5 points**) Genetic algorithms for sequential circuit test generation use PODEM to generate tests for a fault in the sequential circuit. Answer True or False.

   (h) (**1.5 points**) Easy/Hard heuristic is used in PODEM during backtrace and it can not be used during D-drive. Answer True or False.

2. (**14 points**) **Test Economics**

   A manufacturer produces one million ICs of a design of which only 790,000 are truly good devices. However, due to flaws in testing and for reason of less than 100% fault coverage during testing 820,000 ICs pass the test. On further study of the failed devices it is discovered that the test rejected 1550 "good" ICs.

   Answer the following:

   (a) (**2 points**) What is the True Yield of this process.

   (b) (**2 points**) What is the Yield of this process seen after the test.

   (c) (**5 points**) What is the the true defect level in the batch of devices that passed the test.

   (d) (**2 points**) What percentage of bad devices passed the test.

   (e) (**3 points**) Assuming that the process is mature and only random defects are the cause of failure of the ICs manufactured. What is the fault coverage of the test. Note that you need to choose the correct yield model for this analysis.

3. (**12 points**) **Modeling**

A library cell of a design library realizes a function $f(A, B, C) = A\ B\ +\ C$. A designer makes a mistake in the design while connecting this cell to other parts and uses it to realize the function $A\ C\ +\ B$. Answer the following:

(a) (**4 points**) Write the primitive cubes of f.

(b) (**4 points**) Write two propagation D-cubes of f such that one of the propagation cube must have at least a D as an input and the other must have at least on $\overline{D}$ as an input.

(c) (**4 points**) Write two primitive cubes of failure for the fault specified in the problem description.

4. (**14 points**) **Fault Simulation - Deductive**

The circuit of Fig 1 is to be simulated using the pattern given below:

```
pattern  =   A B C D E F  = 0 0 1 1 1 0
```

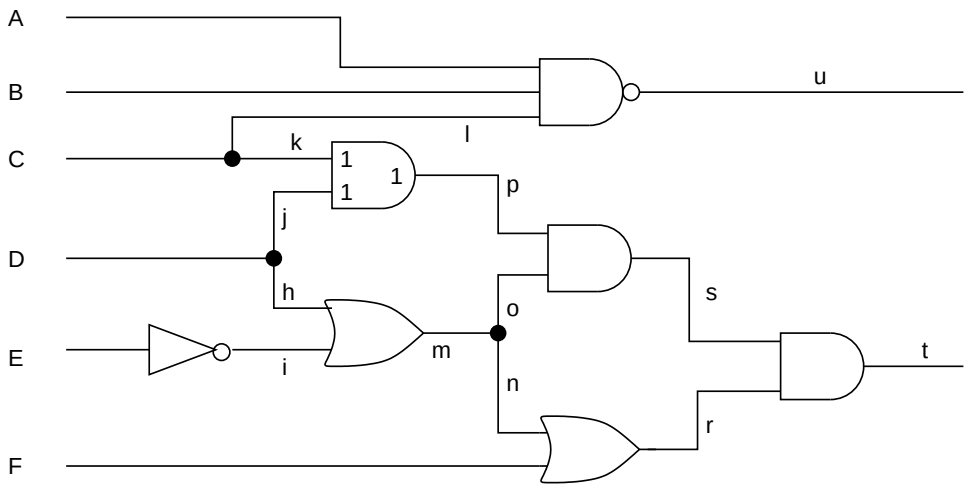

Figure 1: Circuit for deductive fault simulation

The fault list that needs to be simulated for this pattern is given below:

```
A/1  B/1  D/0  E/0  F/1  h/0  i/0  k/0 s/0
```

Note during fault simulation list associated with any line or gate should not contain a fault that is not in the above list.

(a) (**2 points**) Indicate the true signal values in every gate of the circuit. For your convenience, I have already provided values in one of the gates.

(b) (**10 points**) In the table below provide the deductive fault list associated with every line in the circuit. Again to get you started, I have already completed the entries associated with all primary input lines.

Line Name	fault list	Line Name	fault list
A	A/1	i	
B	B/1	m	
C	–	n	
D	D/0	o	
E	E/0	p	
F	F/1	s	
l		r	
k		u	
j		t	
h			

(c) (**2 points**) Now, indicate which of the faults will be detected and at which output.

Faults detected at output u:

Faults detected at output t:

5. (**18 points**) **SCOAP Computation**

Consider the two circuits shown in Figure 2 and Figure 3 for SCOAP computations.

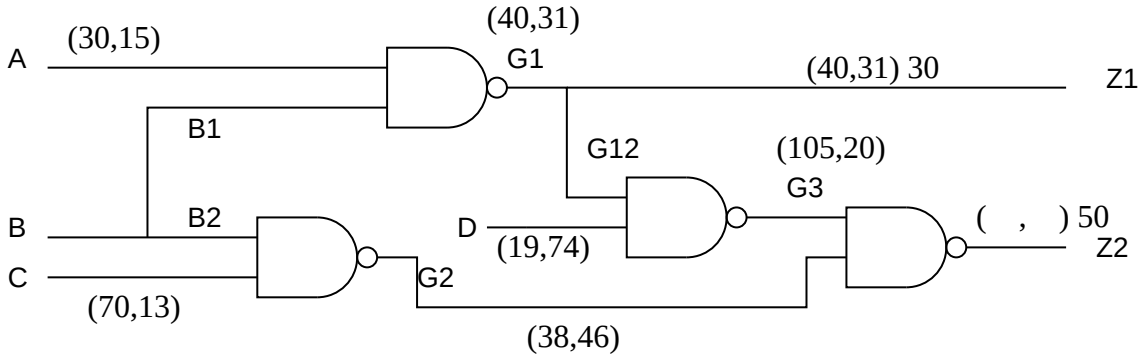

Figure 2: Combinational Circuit for SCOAP Computations

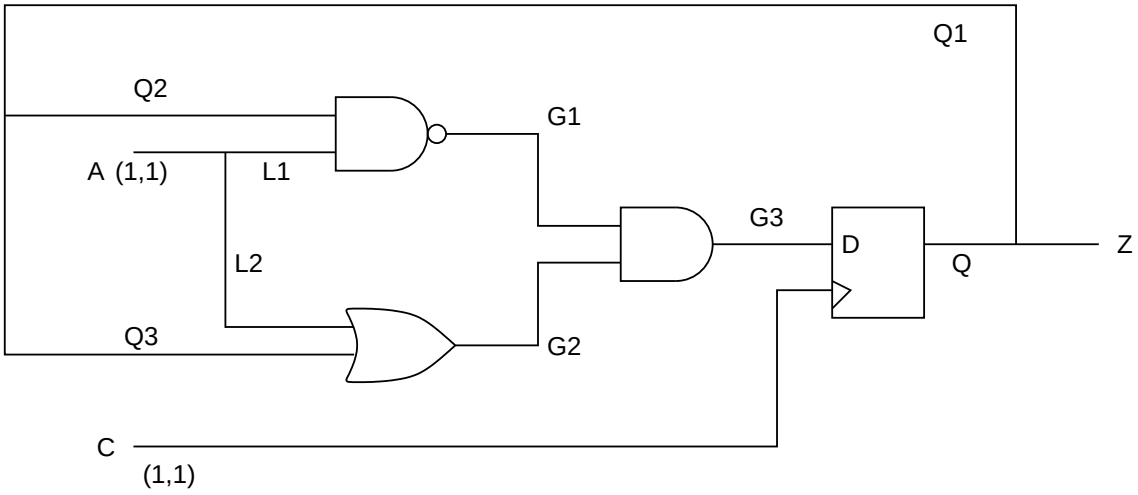

Figure 3: Sequential Circuit for SCOAP Computations

(a) (**8 points**) In the combinational circuit shown in Figure 2 many of the CC0 and CC1 values and some of the observability values are already assigned. The notation used is (CC),CC1)CO. You are to compute all the remaining values, i.e. CC0, CC1 and CO values which are not shown in the figure.

(b) (**10 points**) For the sequential circuit shown in Figure 3 you are to compute the combinational CC0 and CC1 values. Note that it may take more than one iteration. I have completed the initial iteration. Complete the subsequent iteration and stop when no change takes place in the CC0 and CC1 values.

Initial					
A (CC0,CC1) 1,1	C (CC0,CC1) 1,1	L1 (CC0,CC1) ∞,∞	L2 (CC0,CC1) ∞,∞	G1 (CC0,CC1) ∞,∞	G2 (CC0,CC1) ∞,∞
G3 ∞,∞	Q ∞,∞	Q1 ∞,∞	Q2 ∞,∞	Q3 ∞,∞	Z ∞,∞
Iteration 1					
A	C	L1	L2	G1	G2
G3	Q	Q1	Q2	Q3	Z
Iteration 2					
A	C	L1	L2	G1	G2
G3	Q	Q1	Q2	Q3	Z
Iteration 3					
A	C	L1	L2	G1	G2
G3	Q	Q1	Q2	Q3	Z
Iteration 4					
A	C	L1	L2	G1	G2
G3	Q	Q1	Q2	Q3	Z

6. (**12 points**) **Combinational Test Generation - PODEM**

A PODEM like test generator is used to generate a test of for the line 20 s-a-1 in the circuit of Figure 4.

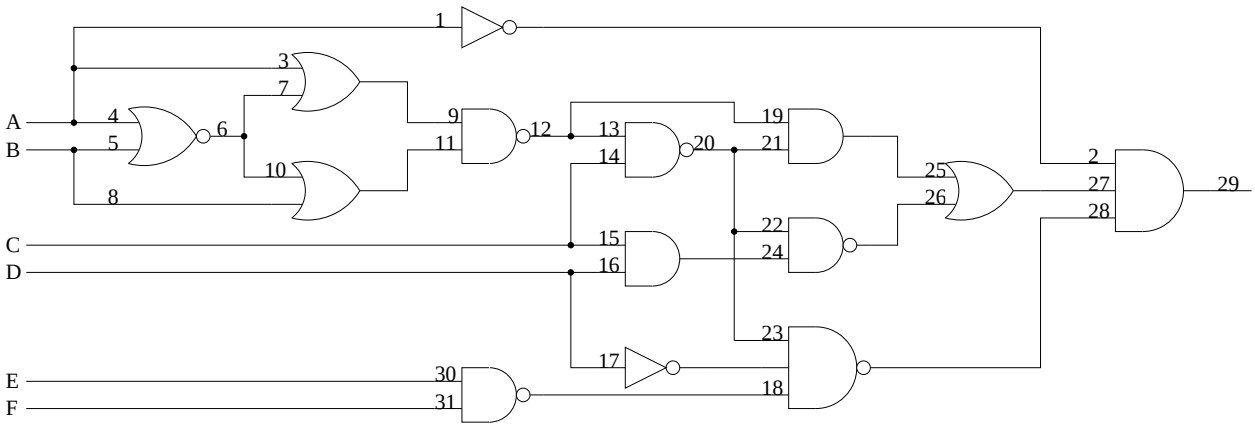

Figure 4: Circuit for test generation

It is still in the process of test generation and has made the assignments at some of the primary inputs as follows and in the order shown:

```
C = 1
B = 1
A = 1
A = 0
D = 0
```

(a) (**3 points**) Construct the decision tree for the completed work this far.

(b) (**7 points**) In the table below indicate all the implications of the above assignments. I have already filled in a few values at the signal lines.

Assignments	Implications
C=1, B=1, A=0, D=0	Lines 14, 15 are 1; Lines 5, 8 are 1; Lines 4, 3, 1 are 0; Lines 16, 17 are 0

(c) (**2 points**) Will this assignment cause a back track or lead to next new assignment?

7. (**16 points**) **Checking Experiment**

State table of a finite state machine with five states, A, B, C, D, and E; an input alphabet consisting of a, b; and with output alphabet consisting of 0, 1; is given below.

Table 1: State Machine for Problem xx

	Input	
	a	b
A	A/0	C/1
B	A/1	C/0
C	B/0	D/1
D	B/1	E/0
E	C/1	A/0

Answer the following:

(a) (**2 point**) Is this machine strongly connected?

(b) (**5 points**) Find a shortest synchronizing sequence for this circuit if one exists. You **must show your work otherwise no points** will be awarded.

(c) (**3 points**) Find a shortest synchronizing sequence for this circuit that synchronizes this circuit to state E. Thus the final state of the machine should be E irrespective of the start state of the machine. Again, you must show your work for full credit.

(d) (**3 points**) Find a shortest distinguishing sequence for this machine that begins with the input "b". You must show your work for full credit.

(e) (**3 points**) Is the sequence "b a a b" a homing sequence for this machine. You must show your work. and give a brief explanation for your answer.