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Low Power Digital System Design

On-chip Interconnects

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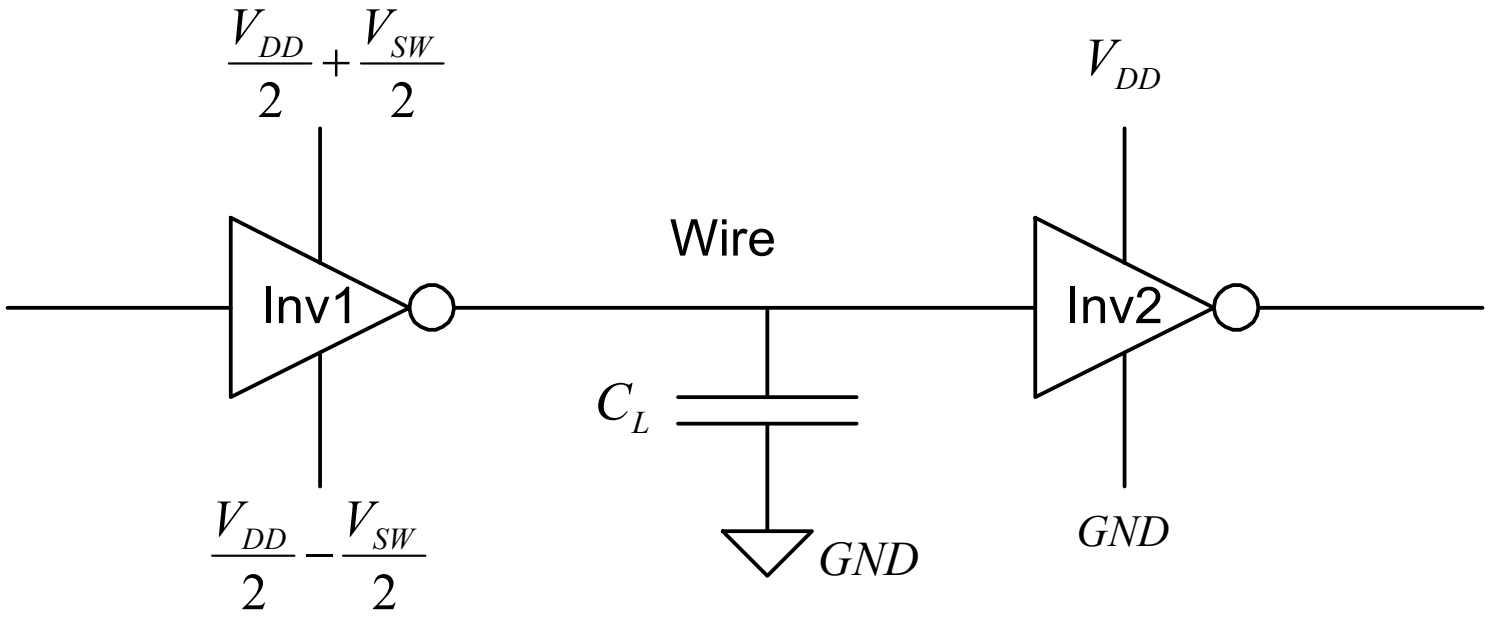
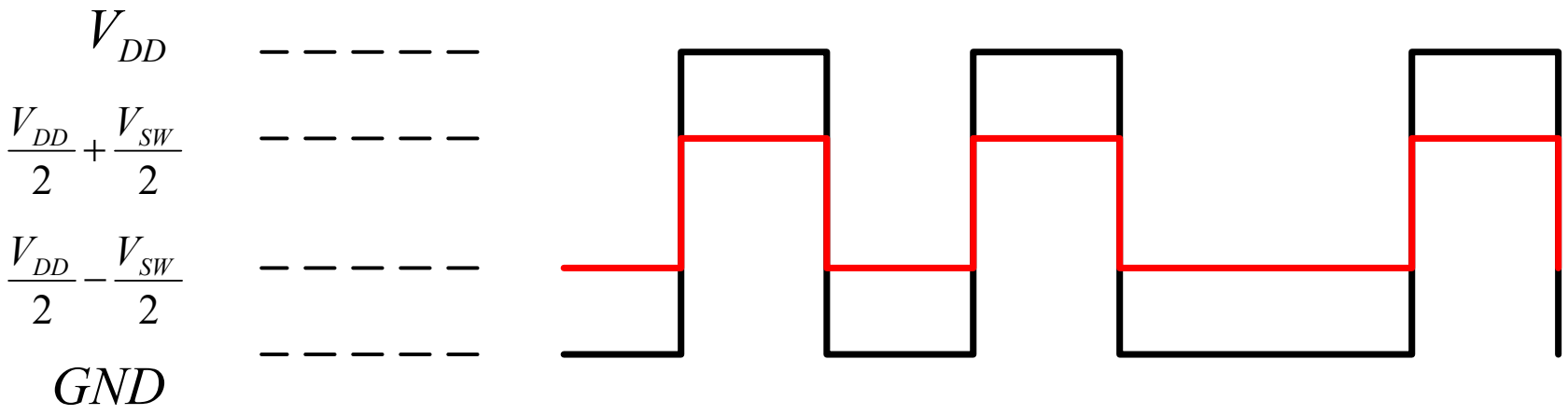
On-chip Interconnects

- Account for a significant fraction (up to 50%) of the total on-chip energy (SoC).
- One possible solution:
  - reduced voltage swing



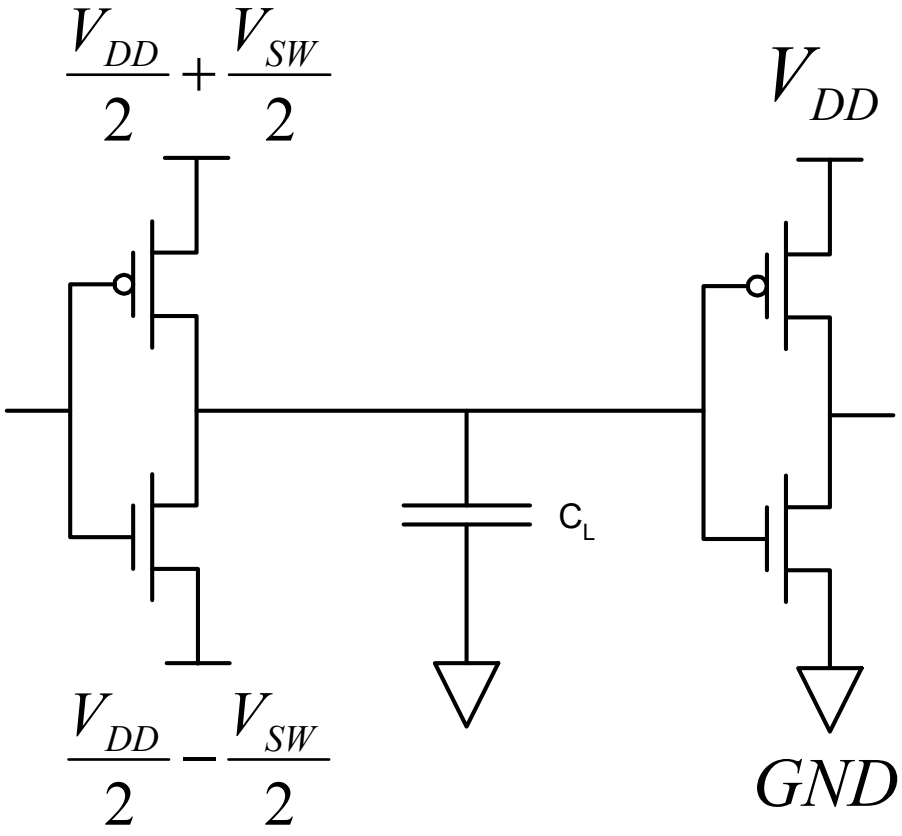
Reduced Voltage Swing



$$Power \propto Amplitude^2$$

Level Shifters

- Inverters used as Level Shifters



Switching Power

- Mainly consumed by driver inverter
  - Driver supply voltage is externally generated.
  - Voltage Source (efficient dc-dc converters).

$$P_{SW} = \alpha \cdot f \cdot C_L \cdot V_{SW}^2$$

  - Driver supply voltage is internally generated.
  - Series regulators.

$$P_{SW} = \alpha \cdot f \cdot C_L \cdot V_{SW} \cdot V_{DD}$$

Static Power

- Mainly consumed by receiver inverter
- Transistors of receiver INV may never be in sub-threshold region.

$$I_{REC-Static}(V_{SW}) = \begin{cases} 0 & \frac{V_{DD}}{2} - \frac{V_{SW}}{2} \le V_{th} \\ \frac{\beta}{2}\left(\frac{V_{DD}}{2} - \frac{V_{SW}}{2} - V_{th}\right)^2 & \frac{V_{DD}}{2} - \frac{V_{SW}}{2} > V_{th} \end{cases}$$

Optimum Voltage Swing

$$V_{SW} \downarrow \Rightarrow P_{SW} \downarrow$$

$$V_{SW} \downarrow \Rightarrow P_{Static} \uparrow$$

- Optimum voltage swing minimizes the total power.
- It is a function of activity:

$$\alpha \downarrow \Rightarrow V_{SW} \uparrow$$

Compromising Other Objectives

- Performance (Operational Frequency):

$$f(V_{SW}) = \frac{\beta}{2C_L} \cdot \frac{(V_{SW} - V_{th})^2}{V_{SW}}$$

- Reliability (Bit Error Rate):
  - Gaussian Noise Assumption

$$BER(V_{SW}) = Q\left(\frac{V_{SW}}{2\sigma_N}\right)$$

where

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{\frac{-u^2}{2}} du$$

Assignment

- Analyze the power of a case-study interconnect
  - Technology: 90nm PTM
  - C_L=0.5pf (Wire length=almost 2mm)
  - Aspect ratio (W/L): N:3, P:6
  - V_{DD}=1.1V
  - V_{SW}=0.2V, 0.4V, 0.8V, 1V
  - Power consumption=?
  - Cut-off frequency=?

References

Christer Svensson, "**Optimum Voltage Swing on On-Chip and Off-Chip Interconnect**", *IEEE Journal of Solid-State Circuits*, 2001.

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