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Low Power Digital System Design

Circuit-Level LPD Techniques

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Circuit-Level LPD Techniques

- Example of circuit-level LPD techniques:
  - Multi-V_t circuits
  - Multi-V_{DD} circuits
  - Minimizing device count and internal swing (Proper CMOS logic style).
    - Pseudo NMOS, CPL
  - Custom circuit design

Dual Threshold Circuits

- Dual threshold technique can be used to deal with the leakage problem.
- Why has leakage problem become an important concern in LPD?
  - V_{DD} reduction =>
    - Switching Power decreases quadratically
    - Sub-threshold Leakage Power deceases linearly
  - V_{th} reduction =>
    - Increases Sub-threshold Leakage Power exponentially

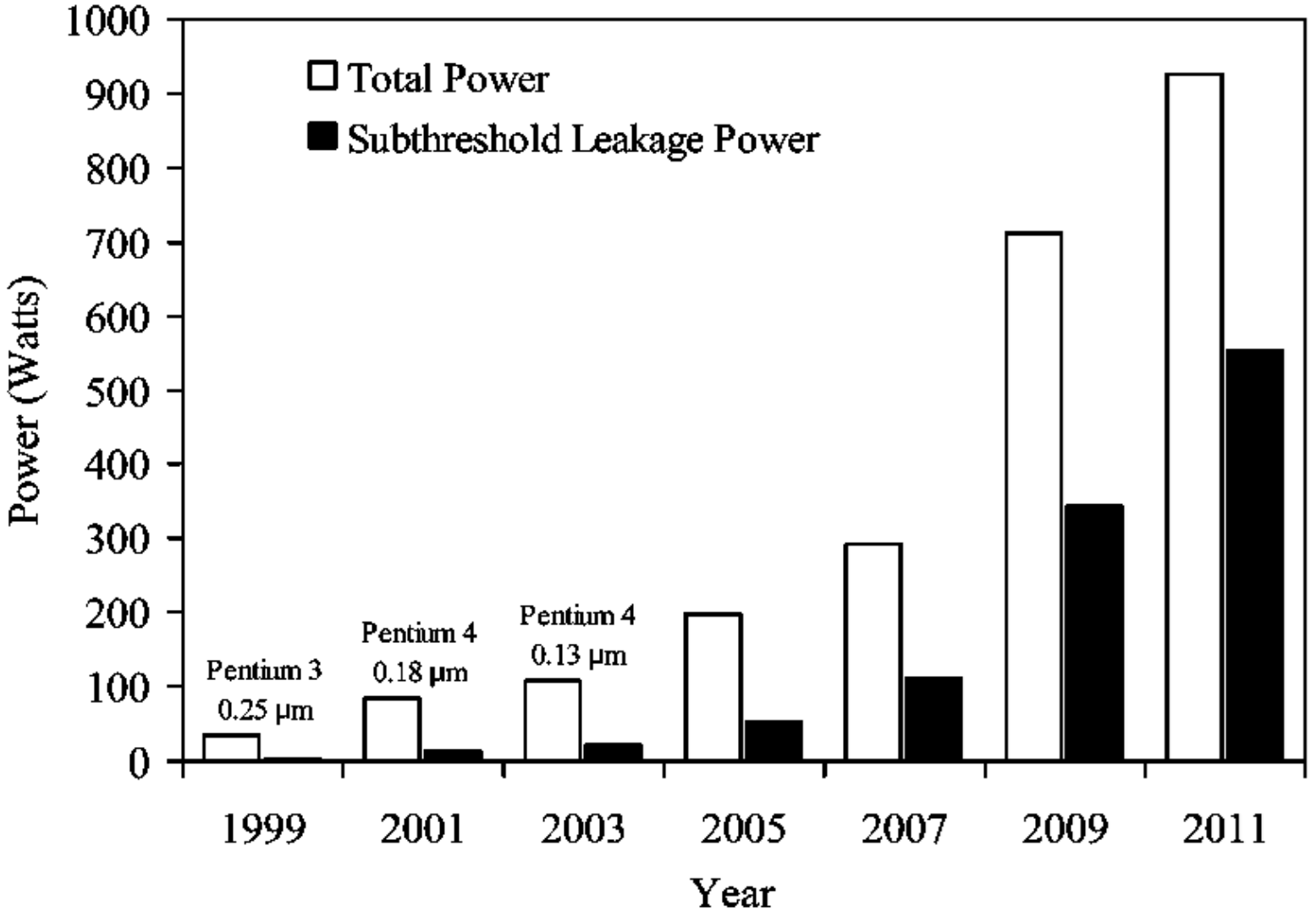
Impact of Scaling on Sub-threshold Leakage Power

$$P_{SUB} = V_{DD} \cdot \beta(1-\eta)V_T^2 \underbrace{\exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right)}_{T1} \underbrace{\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right]}_{T2}$$

where $V_T = \frac{KT}{q}$

- Assume: $V_{GS} \cong 0$, $V_{DS} \cong V_{DD}$ (Realistic assumption)
- In constant field scaling, the relative variations of term *T1* is much greater than the relative variations of term *T2*.

Power Trends of Microprocessors



Impact of Threshold Voltage on Circuit Performance

$$V_{th} \uparrow \Rightarrow P_{Sub} \downarrow$$

$$V_{th} \uparrow \Rightarrow Delay \uparrow$$

$$Delay \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_{th})^{\alpha}}$$

Dual Threshold Circuits

- Main Idea: Assigning a high-threshold voltage to some transistors in non-critical paths, and using low-threshold transistors in critical path(s).

- Not all the transistors in non-critical paths can be assigned a high-threshold voltage, otherwise, the critical path may change, thereby increasing the critical delay.

Dual Threshold Circuits

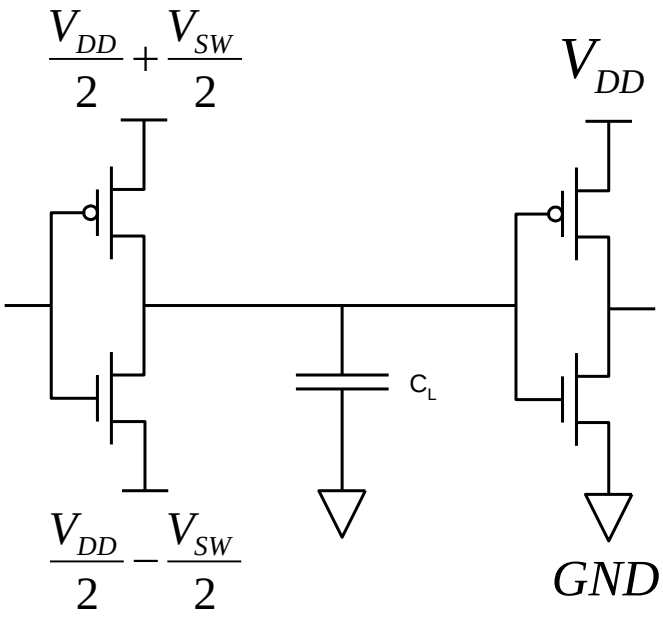
- Dual-threshold voltages can be achieved by:
  - Body Biasing

$$V_t = V_{t0} + \gamma[\sqrt{2\Phi_b + |V_{sb}|} - \sqrt{2\Phi_b}]$$

$$V_{sb} \uparrow \Rightarrow V_{th} \uparrow$$

  - Dual-V_{th} MOSFET Process
    - Channel Doping

Dual Threshold Circuits: Application in Level Shifters



Driver Inverter

Receiver Inverter

$$P_{SW} = \alpha \cdot f \cdot C_L \cdot V_{SW} \cdot V_{DD}$$

$$I_{REC-Static}(V_{SW}) = \begin{cases} 0 & \frac{V_{DD}}{2} - \frac{V_{SW}}{2} \le V_{th} \\ \frac{\beta}{2}\left(\frac{V_{DD}}{2} - \frac{V_{SW}}{2} - V_{th}\right)^2 & \frac{V_{DD}}{2} - \frac{V_{SW}}{2} > V_{th} \end{cases}$$

- Assigning a high-threshold voltage to the transistors of the receiver LS, and using low-threshold transistors in the driver LS.