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Low Power Digital System Design

Gate-Level and Circuit-Level Techniques (Cont.)

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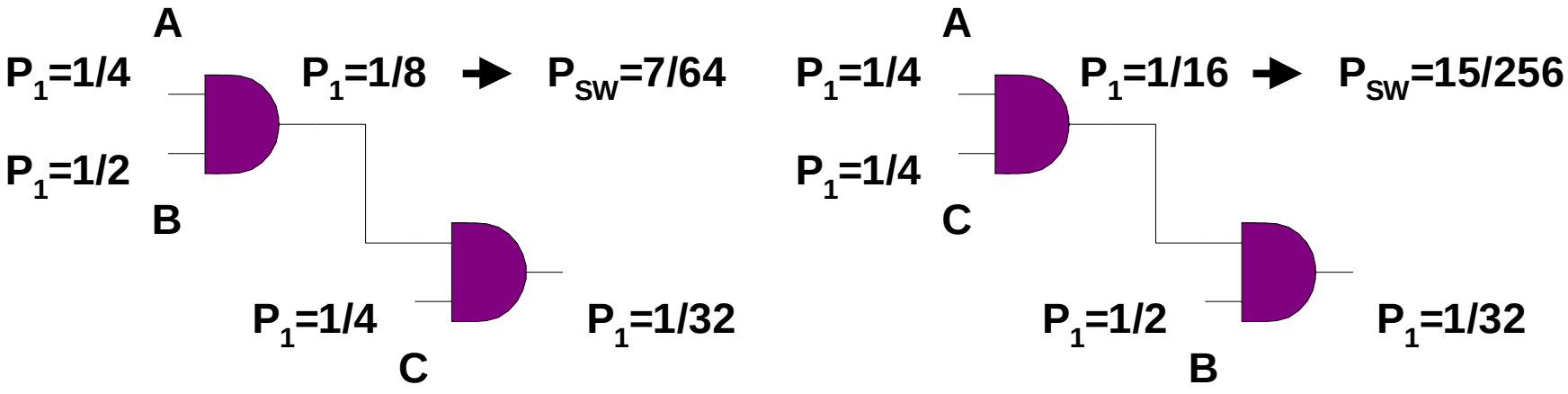
Input Reordering

- Input Reordering: Changing the spatial order in which the inputs are entered to a Boolean network without changing the network logic.
  - Input reordering at the gate level of abstraction
    - Activity Postponement
  - Input reordering at the circuit level of abstraction
    - Sometimes requires transistor reordering

Activity Postponement

- The basic concept is to postpone introduction of high activity signals as long as possible. In this way, the fewest gates are affected by the rapidly switching signals.
  - Objective: Reducing activity α
- Example:



Activity Postponement: Example 2

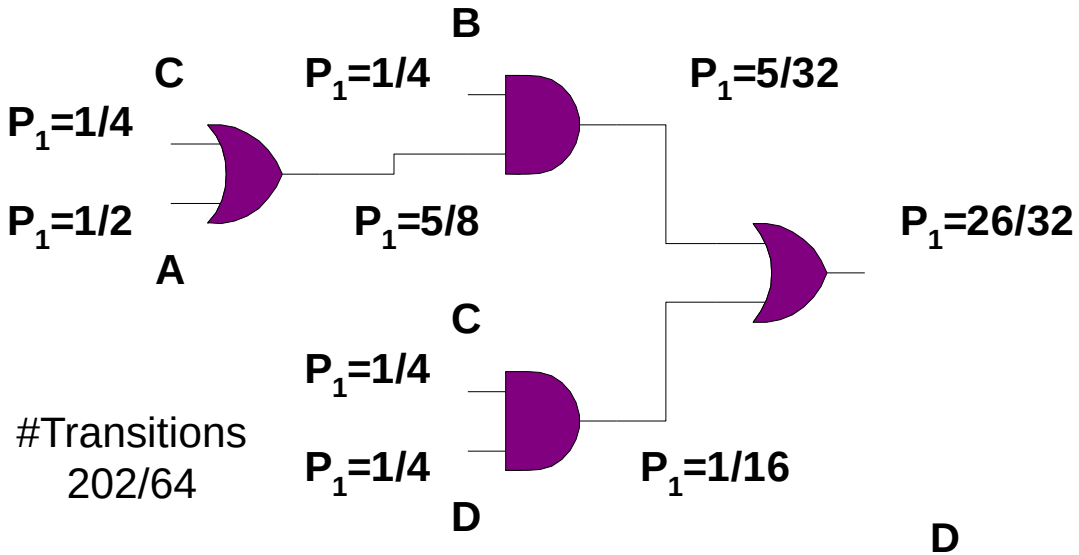
$$F(A,B,C,D) = AB + BC + CD =$$
$$F_1(A,B,C,D) = B(A+C) + CD =$$
$$F_2(A,B,C,D) = AB + C(B+D) =$$

- Assuming that:
  - A:P1=1/2
  - B:P1=1/4
  - C:P1=1/4
  - D:P1=1/4

- When A is a rapidly switching signal F_2 dissipates less switching power than F_1.

Example 2 (Cont.)

$$F(A,B,C,D) = AB + BC + CD = B(A+C) + CD = AB + C(B+D)$$



#Transitions
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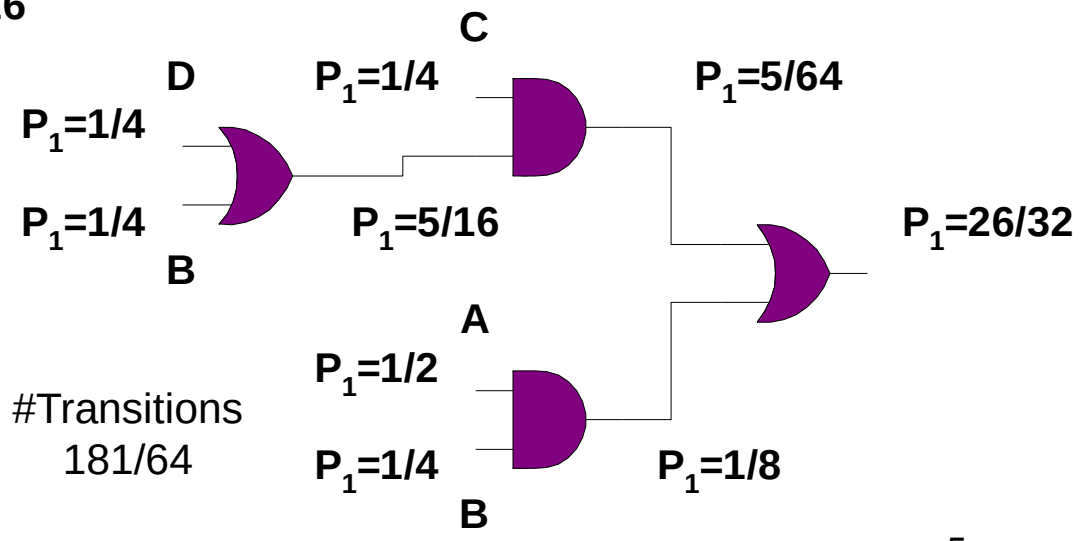

#Transitions
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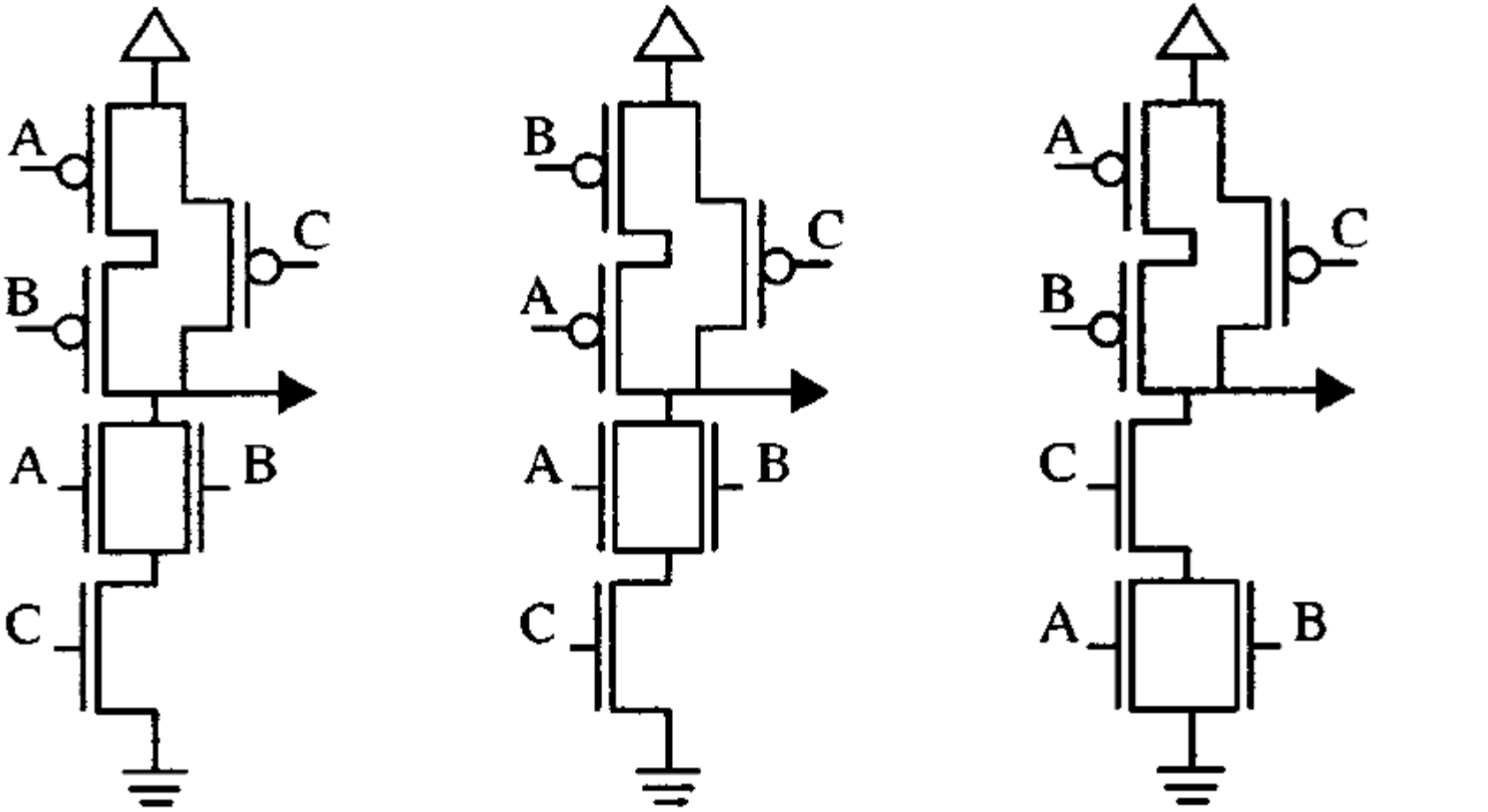
Input reordering at the circuit level

- The main objective is to reduce the switching power of low capacitance internal nodes.
  - Diffusion capacitance ≅ 20% of the gate capacitance

- Rules for input ordering (transistor ordering):
  - Signals with a high probability of switching are placed nearest the output.
  - Signals with a high probability of being off are placed nearest the output .
  - Signals with high probability of being on are placed nearest the supply node.

Input and Transistor Reordering

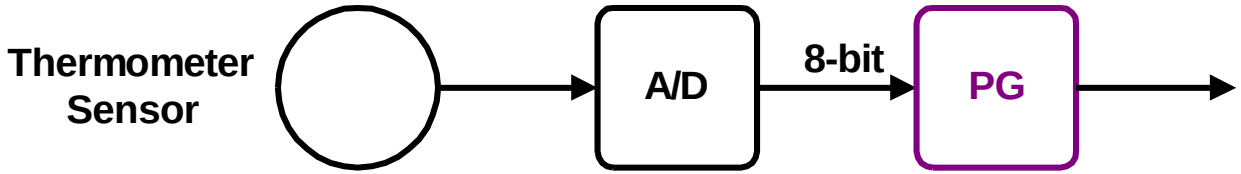


Input Reordering

Transistor Reordering

Assignment

- Design a parity generator circuit with minimum PDP (Power Delay Product)
  - 8-bit Parity Generator



  - Probability distribution:

$$P(B_i = 1) = \frac{1}{2^{i+1}}$$

    - LSB: i=0, MSB: i=7
    - The probabilities are independent
  - Gate level estimation:
    - Power = Transition * Fan-out
    - Delay = Number of circuit levels (Only 2-input XOR gates are allowed)

References

C.-Y. Tsui, et. al., "Power Efficient Technology Decomposition and Mapping Under an Extended Power Consumption Model", IEEE Transactions on CAD, 1994.

B. Moyer, "Low-Power Design for Embedded Processors", Proceedings of the IEEE, 2001.