Department of Electrical and Computer Engineering
University of Wisconsin–Madison

ECE 553: Testing and Testable Design of Digital Systems
Fall 2008-2009

Final Examination

CLOSED BOOK

Kewal K. Saluja

Date: December 18, 2008
Place: Room 2535 Engineering Hall
Time: 12:25 - 2:25 PM
Duration: 120 minutes

PROBLEM	TOPIC	POINTS	SCORE
1	General/PreMidterm	12	
2	TEST GEN	10	
3	CHECK-SEQ	10	
4	MEMORY	11	
5	PSEUDO-EXH	16	
6	TEST TIME	17	
7	BIST	14	
8	BOUNDARY SCAN	10	
TOTAL		100	

Name: (Please Print in Capitals)

Last Name: _____

First Name: _____

Show your work carefully for both full and partial credit.
You will be given credit only for what appears on your exam. **Use facing page when ever you need more space to write**

1. (**12 points**) **General and Pre-Midterm**

   Answer the following. Use only the space provided and be brief.

   (a) (**2 points**) In a two input NAND gate with inputs **a** and **b** and output **z** Which of the following fault(s) can be removed due to dominance fault collapsing and why?

   `a s-a-0,  a s-a-1,  b s-a-1,  z s-a-0`

   (b) (**1 points**) True or False. The D-algorithm will always find a test if one exists.

   (c) (**2 points**) Besides Test Pattern Generation, name two other usages of Linear Feedback Shift Registers.

   (d) (**4 points**) Consider the circuit given in Figure 1(a) below.

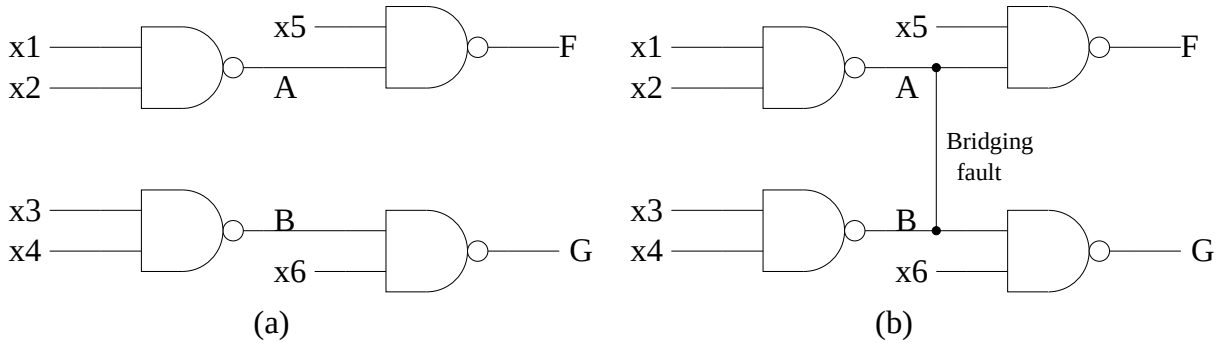

Figure 1: Circuit for Problem 1 - Original and with Bridging Fault

Tests shown in the table below are applied to this circuit. Indicate in the table if the single fault A stuck-at 0, fault B stuck-at 0 will be detected or not by these tests.

Test #	X1	X2	X3	X4	X5	X6	A s-a 0	B s-a 0	OR-Bridge
1	0	1	1	1	0	1			
2	1	1	0	1	1	0			
3	0	1	0	1	1	1			
4	0	1	1	1	1	0			

(e) (**3 points**) Now consider the circuit of (a) with a bridging fault as shown in (b). Let this be an OR type bridging fault between lines A and B. Note that an OR type bridge means that if the lines A and B are bridged and if any of the lines A or B is logic 1 than both A and B will take logic 1 values. Show in the above table which tests will detect the OR types bridging fault in the circuit.

2. (**10 points**) **Sequential Test Generation**

Consider the sequential circuit described below using two edge trigger D-type flip-flops. Derive a test sequence for the fault 2/0/1 (output of gate 2 s-a-1) in this circuit. Assume the initial states of both the flip-flops (FF1 and FF2) are set to 0. Show your work indicating the

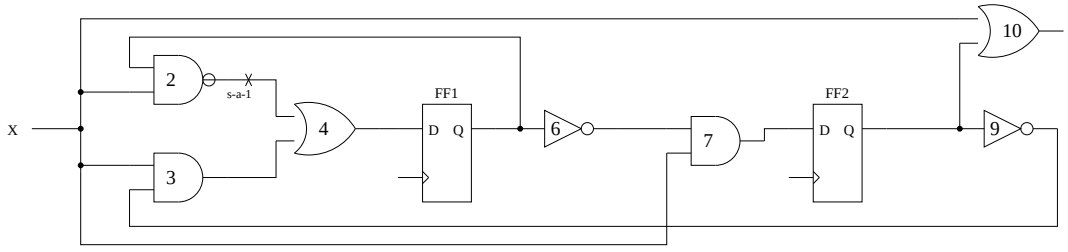

Figure 2: Circuit for Test Generation

test generation process. You can use any method you like. But provide your answer in the following format. In the "comments" column provide information about need for your action, such as "fault excited", "sensitize fault", etc.

Time (t)	Present State FF1 FF2	Input (X)	Next State FF1 FF2	Comments
0	0 0			
1				
2				
3				
4				
5				
6				
7				
8				

3. (**10 points**) **Checking Sequence**

Consider a finite state machine (FSM) with six states given below.

Present State	Next State/Output	
	x = 0	x = 1
A	B/0	A/0
B	C/1	B/1
C	D/0	C/0
D	E/1	D/0
E	F/0	E/0
F	A/1	A/1

Now answer the following.

(a) (**4 points**) Consider two sequences of length four for this FSM and these are 1 0 1 0 and 1 0 1 1. What will be the output sequences for these sequences if the initial state is either A or B?

(b) (**6 points**) You are told that on start-up this FSM can NOT be in states A or F. Thus the initial ambiguity of the FSM is {B C D E}. Find a shortest sequence that can differentiate between all these states. You must show your work to get any credit for this question.

4. (**11 points**) **Memory testing**

Consider the following March algorithm:

$$\{\Uparrow (W0); \quad \Uparrow (R0, W1); \quad \Downarrow (R1, W0)\}$$

This algorithm is used to test a large two dimensional memory array consisting of a total of n cells.

(a) (**1 points**) What is the length of the above test.

(b) (**2 points**) Consider a memory fault in which when ever the contents of cell 250 are changed, the cell 200 will also change state (inversion coupling fault). The above algorithm can only potentially detect this fault and can not detect this fault definitively. Explain in the space provided. Long explanation will be penalized.

(c) (**2 points**) Consider a memory fault in which when ever the contents of cell 1250 are changed, the cell 5000 will also change state (inversion coupling fault). Can the above algorithm definitely detect this fault? If yes, when will be fault be excited and when will it be detected?

(d) (**3 points**) If the direction of initialization on the above algorithm is changed (i.e. the first march element is changed to $\Downarrow (W0)$) which of the two faults will be detectable by such a modified algorithm? Give a brief explanation.

(e) (**1 points**) Will the original algorithm detect cell stuck-at 0 and 1 faults in the memory array?

(f) (**1 points**) Will the original algorithm detect transition faults in the memory array?

(g) (**1 point**) How many march elements does the original test have?

5. (**16 points**) **Pseudo-exhaustive testing**

Consider the circuit below in Figure 3. This circuit is to be tested using pseudoexhaustive testing with sensitized partitioning. The partitions are shown in the figure. Note that each gate forms a partition and it must be tested exhaustively using all 4 tests. Also remember when a partition is tested its output must be sensitized to the primary output. Derive

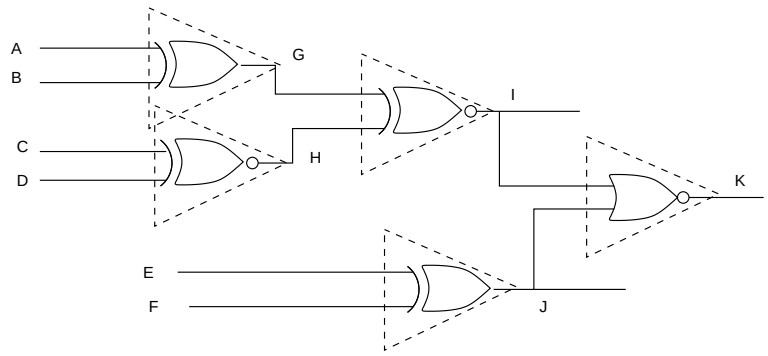

Figure 3: Figure for Pseudoexhaustive Test Generation

a smallest test set (using fewest test vectors) to test this circuit so that each partition is applied all possible required tests. You can derive tests using any method you like but list your tests in the table below which requires you to list and check the inputs and outputs of each partition for each test. Note that you may not need as many vectors as the space provided in the table. Also, some of the column headings repeat to make the checking easier, but these columns must have identical entries to be consistent.

Test #	A B	G	C D	H	G	I	E F	J	I	K

This page is left intentially blank so that you can use it as scratch sheet.

6. (**17 points**) **Test application time**

Consider a design with four scan chains as shown in Figure 4. All the necessary data for the

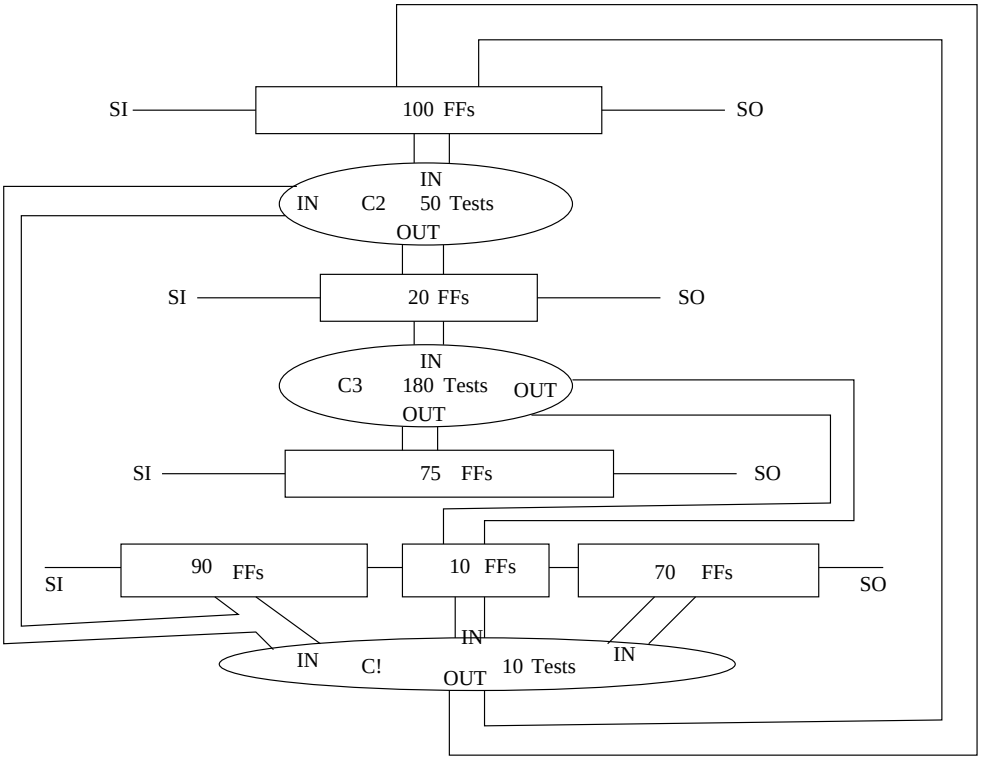

Figure 4: Multiple serial scan chains

circuit, such as number of inputs, number of outputs, number of tests for each combinational block, length of scan chains (some of the lengths can be easily computed from the number of FFs), are provided in the figure.

While answering the following questions you can assume that the *scan-chains are fault-free, thus ignore the application time required to test the scan-chains.*

(a) (**1 points**) What is the number of inputs to the combinational block C1?

(b) (**1 points**) What is the number of inputs to the combinational block C2?

(c) (**1 points**) What is the number of output from the combinational block C3?

(d) (**3 points**) What is the minimum test application time to test only the block C1?

(e) (**3 points**) What is the minimum test application time to test only the block C2?

(f) (**3 points**) What is the minimum test application time to test only the block C3?

(g) (**5 points**) What is the minimum test application time to test all three combinational blocks. calculate the total number of test cycles.

7. (**14 points**) **BIST**

Answer the following and you must show your work for full credit.

(a) (**4 points**) Realization of a 4-bit mixed mode (internal/external EOR Linear Feedback Shift Register (LFSR) is given in the Figure 5 below along with the notation to be used to label the flip-flops.

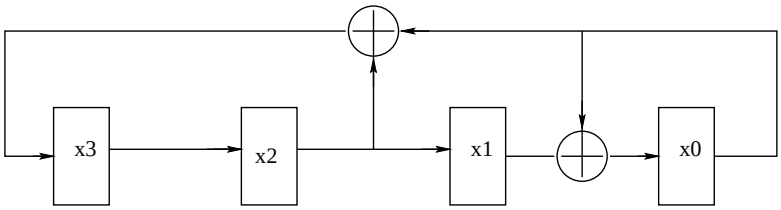

Figure 5: A mixed mode linear feedback shift register

Write the companion matrix T_s for the above LFSR by completing the flowing matrix equation.

$$\begin{bmatrix} x0(t+1) \\ x1(t+1) \\ x2(t+1) \\ x3(t+1) \end{bmatrix} = \begin{bmatrix} \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \end{bmatrix} \begin{bmatrix} x0(t) \\ x1(t) \\ x2(t) \\ x3(t) \end{bmatrix}$$

(b) (**4 points**) Companion matrix T_s of a mixed mode LFSR is given below:

$$T_s = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 \end{bmatrix}$$

Write the characteristic polynomial of this LFSR.

(c) (**3 points**) For each of the following polynomials indicate if it can be factored or not. And if it can be factored, give its smallest degree factor.

i. $x^4 + x^3 + x^2 + x$

ii. $x^{50} + 1$

iii. $x^{49} + x^{47} + x^2 + 1$

(d) (**3 points**) Give an external exclusive-OR (standard) LFSR realization of the polynomial $x^4 + x^3 + x^2 + x$.

8. (**10 points**) **Boundary scan and general problems**

A board contains five ICs all of which have boundary scan. The information relevant to this problem about these ICs is given in the table below:

Device information	IC-1	IC-2	IC-3	IC-4	IC-5
Number of input pins	121	150	98	75	50
Number of output pins	51	75	129	175	250
Bits in Instruction reg	4	3	5	3	7
Bits in Device ID reg	45	45	52	50	45

Answer the following:

(a) (**1 points**) All five ICs form a single boundary scan chain on the board. How many extra pins the board will have to make use of the boundary scan feature of the ICs.

(b) (**2 points**) Assuming that the TAP controller on each ICs is in Shift-IR state, how many test clocks (TCK) are required to load the instruction registers of all ICs?

(c) (**3 points**) Assuming that the TAP controller on each ICs is in Shift-DR state, how many test clocks (TCK) are required to load all boundary registers of all ICs?

(d) (**2 points**) Assume that IC-3 and IC-4 are in bypass modes and the TAP controller on each ICs is in Shift-DR state, how many test clocks (TCK) are required to load all boundary registers of IC-1, IC-2, and IC-5? you can assume that the ICs are connected in sequential order.

(e) (**2 points**) If all five ICs had some pins that were bidirectional, which of the results in the above three cases be different.