Sharif University of Technology
Department of Computer Engineering

Low Power Digital System Design

Concurrency and redundancy at RT-level

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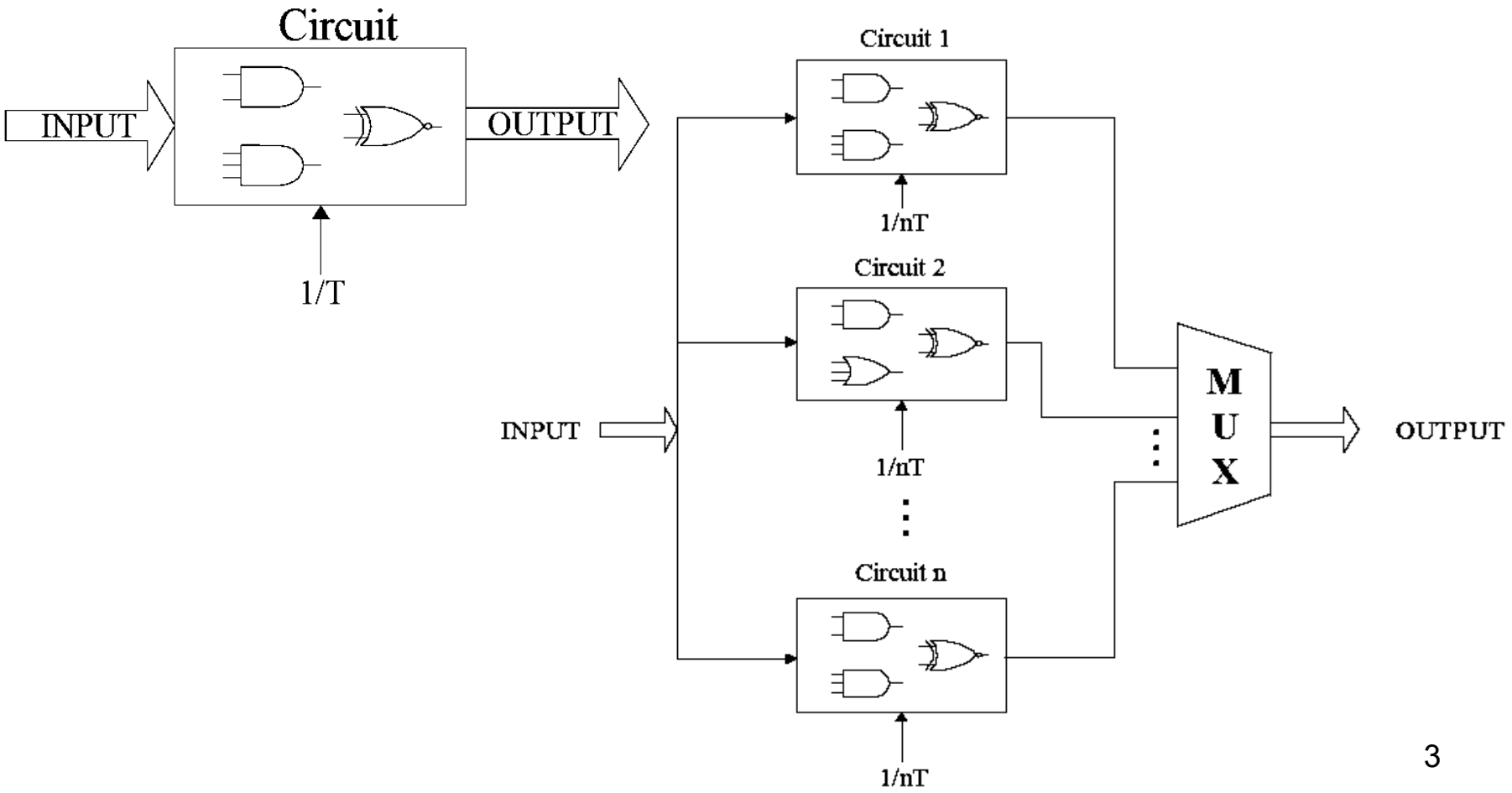
Assignment

- Develop the gate level models of:
  - Ripple carry adder
  - CLA adder
  - Hint: Develop behavioral models and use synthesis tools to generate gate-level models.
- Estimate the C_{eff} redundancy
  - Hint: Use Modelsim and use transition*fan-out as a gate-level measure for C_{eff}, or use Synopsys power compiler.
- Estimate the speed-up of the CLA adder over the ripple carry adder.
- Estimate the power reduction factor.
  - Hint: Recall

$$P'_{SW} = (R \times C_{eff}) \cdot (\frac{V_{DD}}{S})^2 \frac{f}{S}] = \frac{R}{S^3} P_{SW}$$

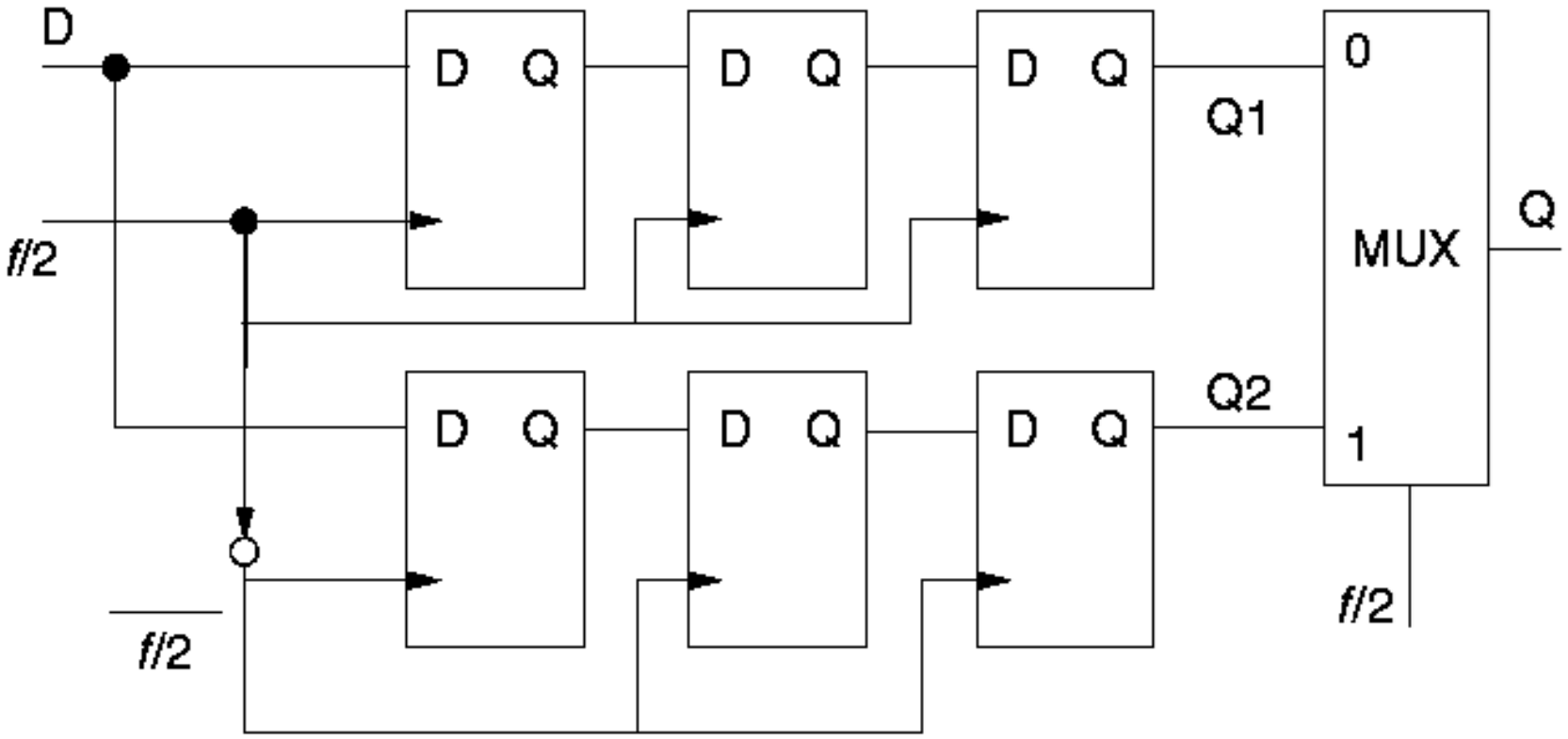
Voltage Reduction Using Parallelism

- Redundancy and concurrency



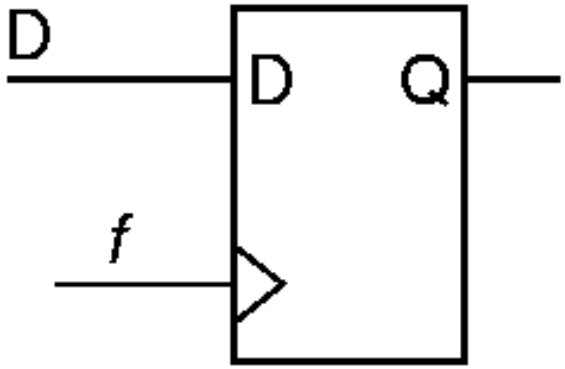
Parallel Shift Register

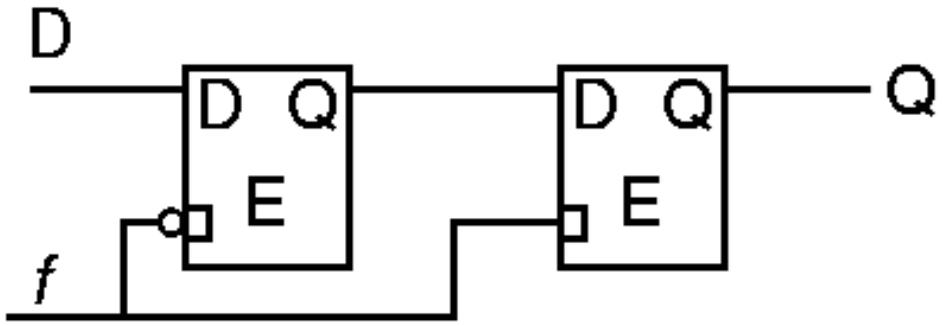
- Redundancy and concurrency

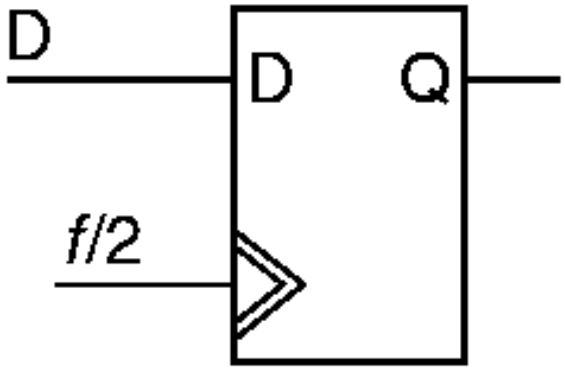


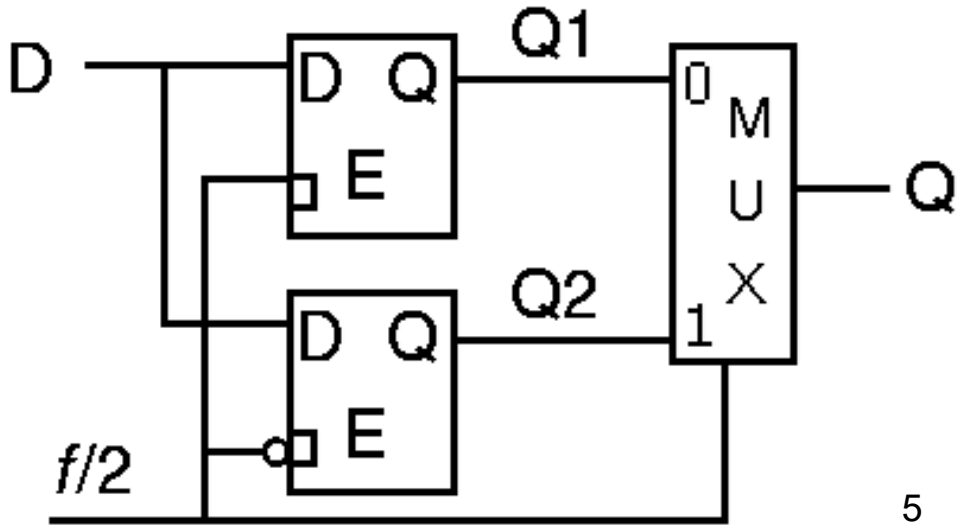
DFF Parallelization

- Redundancy and concurrency









References

H. Mizas, et.al., "Structure of the Low-Power Design Flow", *LPGD/WP1/DUTH/ D1.2R1*, 1998.

R. Hossain, et. al.,"Low Power Design Using Double Edge Wggered Flip-Flops", *IEEE Transactoins on VLSI*, 1994.