Sharif University of Technology
Department of Computer Engineering

Low Power Digital System Design

Operand Isolation

A. Ejlali

Operand Isolation

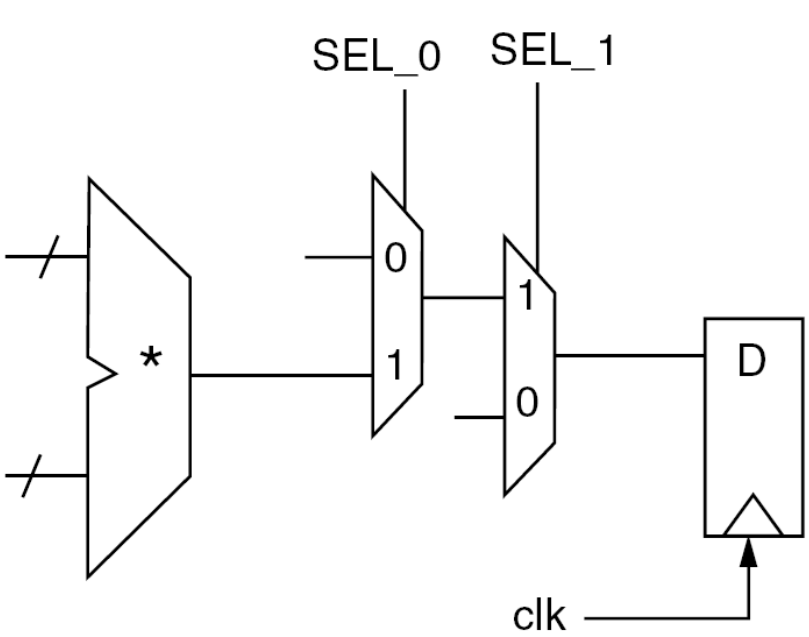
- Clock gating is mainly used to reduce the power dissipation of clock signal.
- However, it may also be used to reduce the power dissipation of FFs and combinational parts.
- At the RT level, the most popular technique for power reduction in the combinational parts is operand isolation.

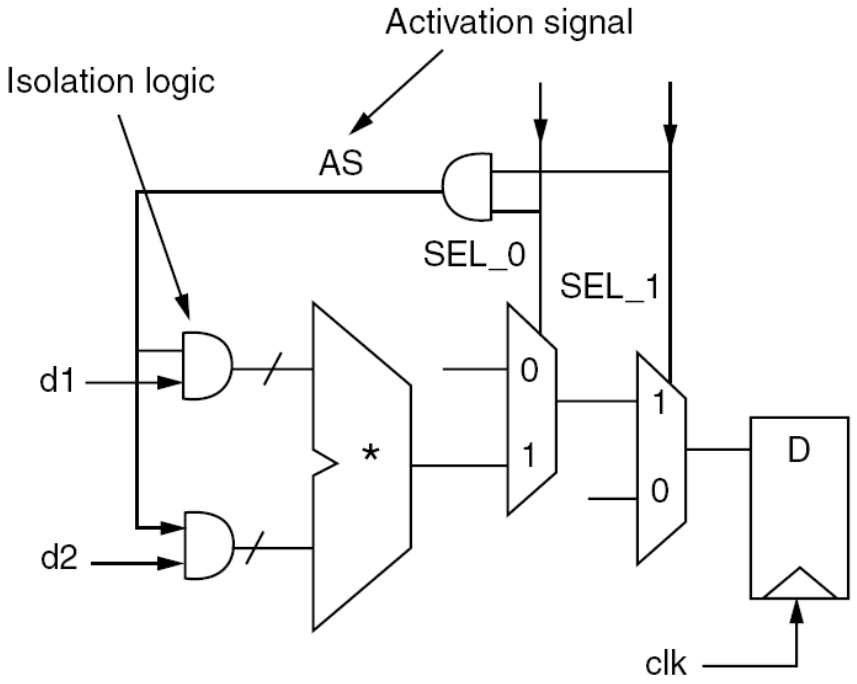
Operand Isolation (Cont.)

- The basic concept in operand isolation is to shut-off combinational logic blocks in clock cycles when they do not perform any useful computation.
  - Similar to clock gating.

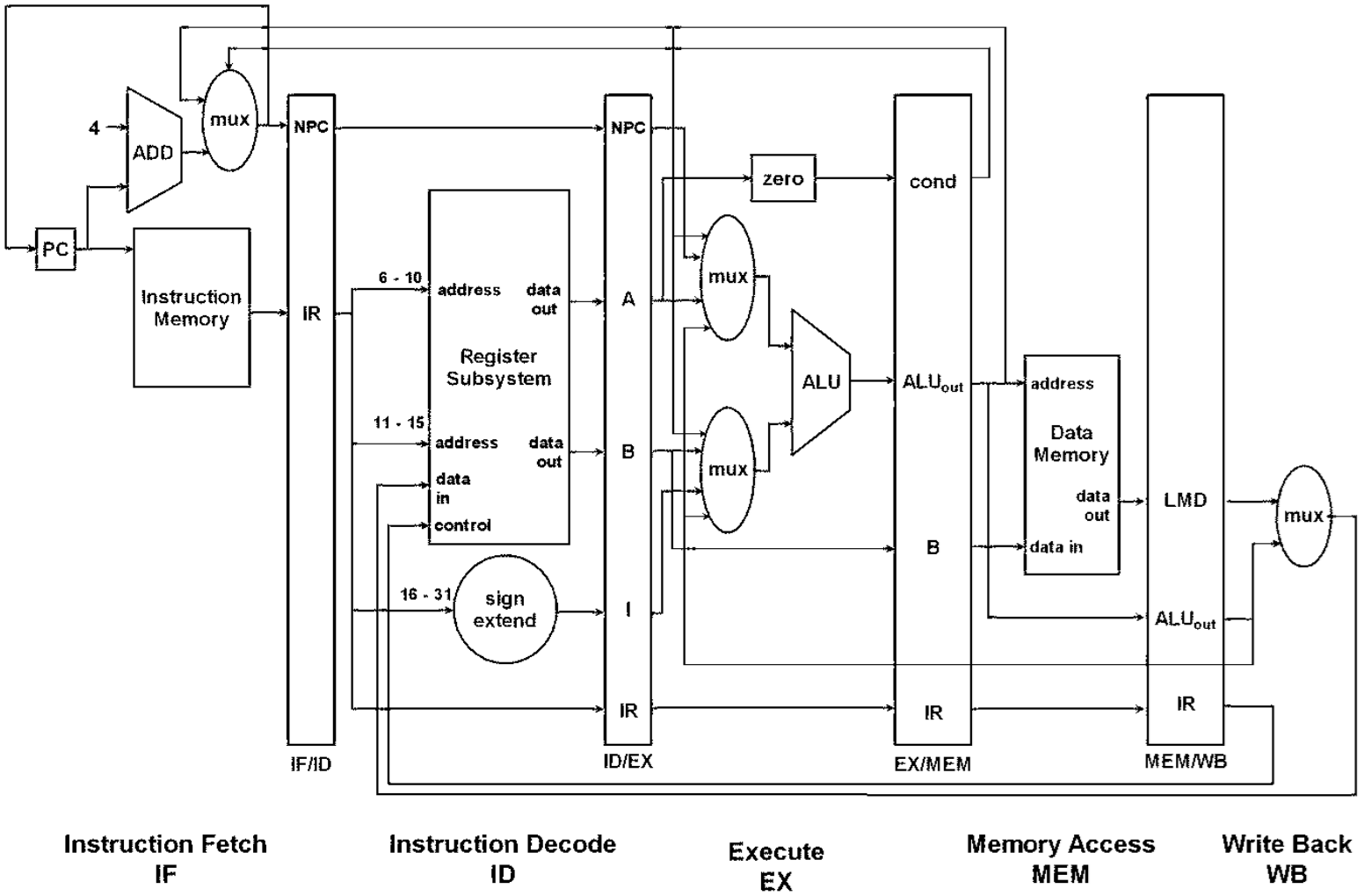
- Shutting-off a combinational block involves preventing the activity in the block by not allowing the inputs to toggle in clock cycles in which the block output is not used.

Operand Isolation: Example 1





Operand Isolation
Example 2: DLX Processor



Reference

M. Munch, et. al., "Automating RT-level operand isolation to minimize power consumption in datapaths", *DATE* 2000.

T. Lobo, et.al., "LP805X: A customizable and low power 8051 soft core for FPGA applications", *ISIE* 2013.