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Department of Computer Engineering

Low Power
Digital System Design

Precomputation

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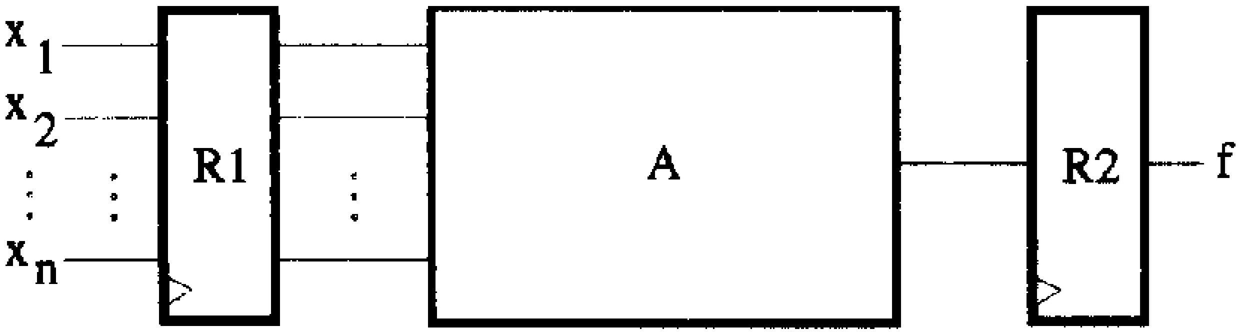
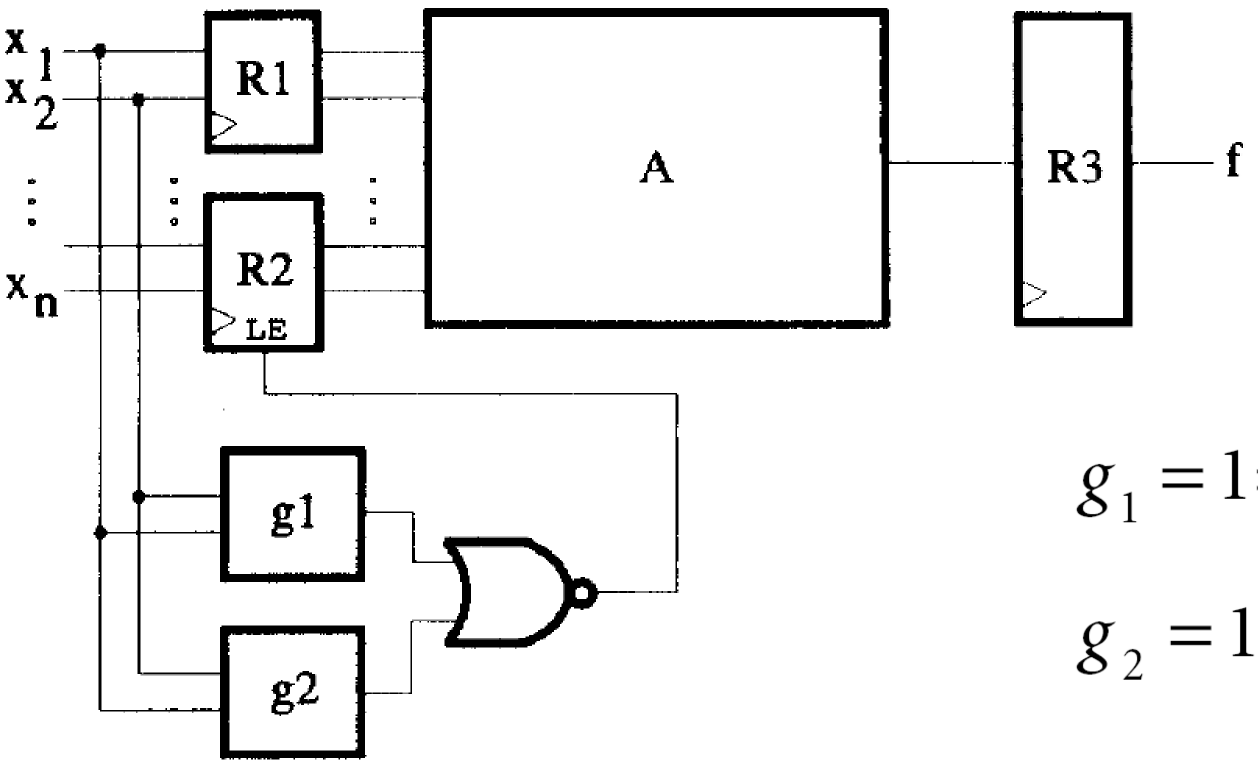
Precomputation

- Basic Ideal:
  - Selectively precomputing the output logic values of a circuit one clock cycle before they are required.
  - Use the precomputed values to reduce the internal switching activity of the combinational logic in the successive clock cycle.

Precomputation Architecture





$$g_1 = 1 \Rightarrow f = 1$$

$$g_2 = 1 \Rightarrow f = 0$$

Predictor Functions: g_1 and g_2

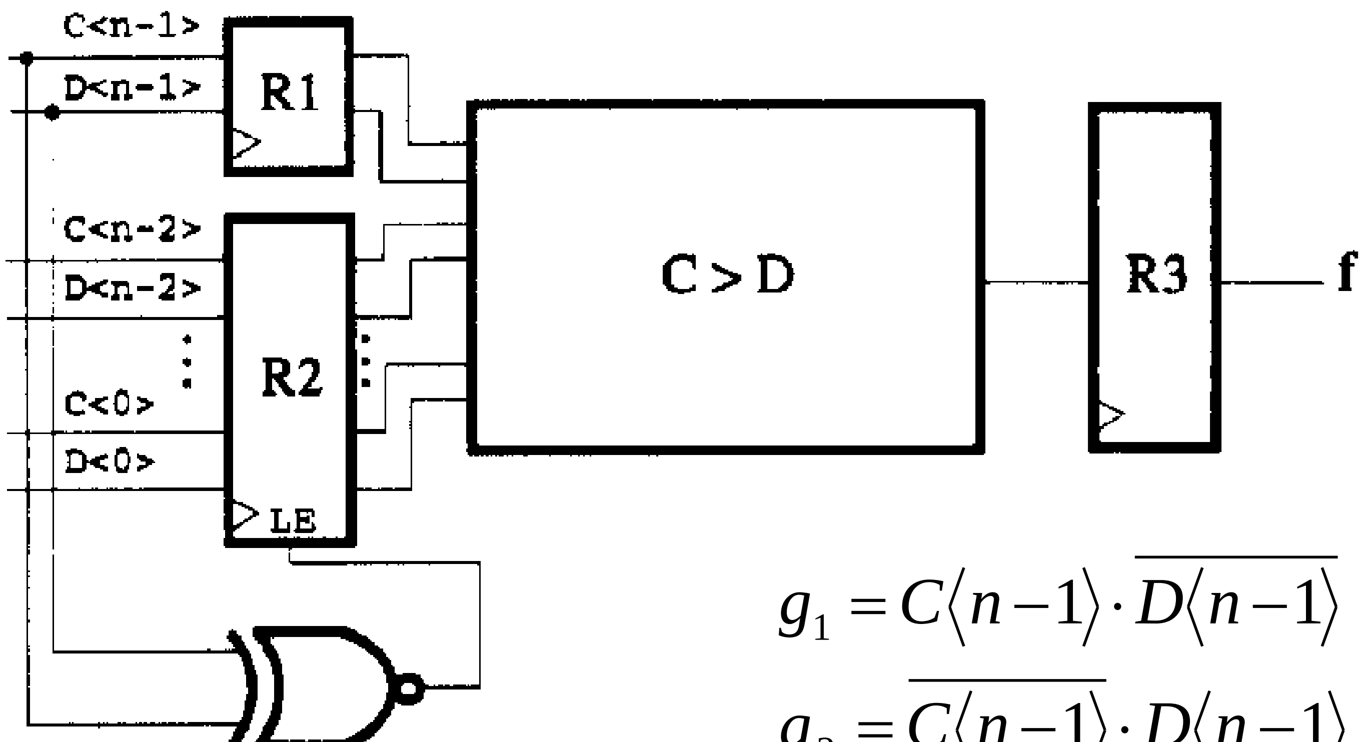
- A power reduction is obtained because for a subset of input conditions corresponding to g_1+g_2,R2 does not change implying reduced switching activity.
- The probability of g_1+g_2 being a 1 should be high.
- g_1 and g_2 have to be significantly less complex than f.
- g_1 and g_2 cannot both be 1 during the same clock cycle due to the conditions imposed by:

$$g_1 = 1 \Rightarrow f = 1$$

$$g_2 = 1 \Rightarrow f = 0$$

An Example of Precomputation

- Example: a n-bit comparator that compares two n-bit numbers C and D and computes the function C > D.



$$g_1 = C\langle n-1\rangle \cdot \overline{D\langle n-1\rangle}$$

$$g_2 = \overline{C\langle n-1\rangle} \cdot D\langle n-1\rangle$$

An Example of Precomputatioin (Cont.)

- In this example, the probability of g_1+g_2 being a 1 is 0.5.

- If we add the inputs C(n-2) and D(n-2) to g1 and g2 it is possible to achieve a power reduction close to 75%.
  - Suitable for large n

Precomputation Logic

- Observability don't care set for input *x*:

$$ODC_x = \overline{f_x \oplus f_{\bar{x}}} = f_x \cdot f_{\bar{x}} + \overline{f_x} \cdot \overline{f_{\bar{x}}}$$

- f_x and $f_{\bar{x}}$ are the cofactors of f .

- What does *ODC* mean?
  - For all the input combinations in ODC_x, we do not need the value of *x* in order to know what the value of f is.

- If we wish to disable the inputs $x_{m+1} \sim x_n$ we will have to implement the predictor function:

$$g = \prod_{i=m+1}^{n} ODC_{x_i}$$

Precomputation Logic (Cont.)

- Universal Quantification of a function:

$$U_x f = f_x \cdot f_{\bar{x}}$$

- What does $U_x f$ mean?
  - all the input combinations that result in f=1 such that the value of x, does not matter.

- Given a subset of inputs $S=\{x_1,x_2,\ldots,x_n\}$, it has been proven that the best choices for g_1 and g_2 are:

$$g_1 = \prod_{i=m+1}^{n} U_{x_i} f \qquad g_2 = \prod_{i=m+1}^{n} U_{x_i} \overline{f}$$

Precomputation Logic (Cont.)

- Problem: Selecting a subset of inputs for the precomputation logic.
  - Exhaustive check
    - Time-consuming
  - The simplest prime implicants in the simplified SOP and POS representations are suitable to be used as g_1 and g_2 functions.
    - For large combinational blocks it is very time-consuming to find simplified SOP and POS representations.

Reference

M. Alidina, "Precomputation-Based Sequential Logic Optimization for Low Power", IEEE Trans. VLSI 1994.