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Embedded System Design

System Level Design

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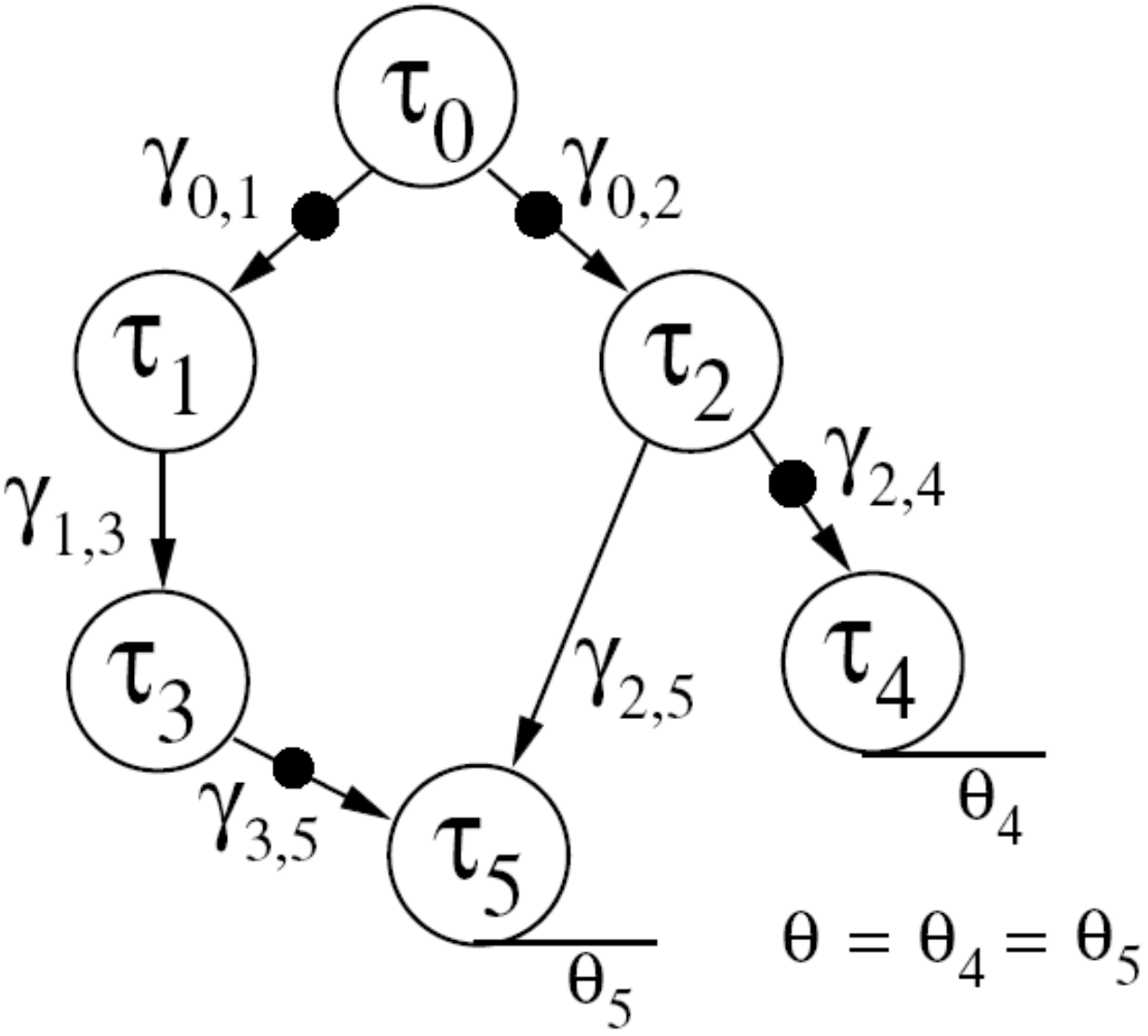
Task Graphs

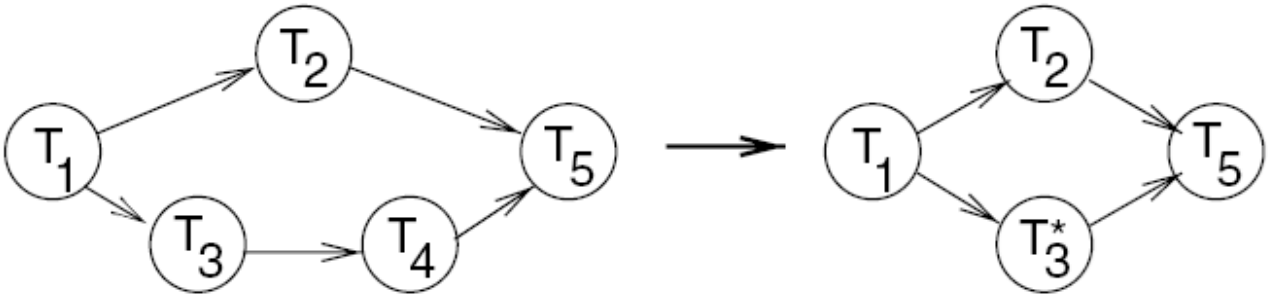
- **DAG = Directed Acyclic Graph**
- **Set of nodes $T = \{t0, t1, ..., tn\}$ denotes the set of tasks to be executed.**
- **Set of directed edges *C* refers to communications between tasks.**
  - **e.g., $(ti,tj) \in C$ indicates a communication from task ti to task t j**

Task Graph Example

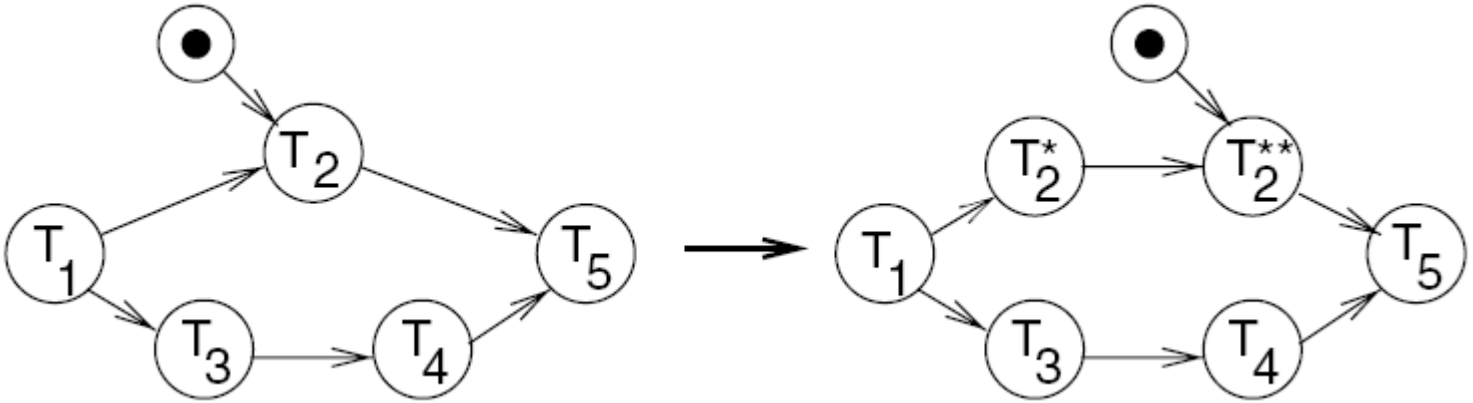


Task Graphs' Granularity

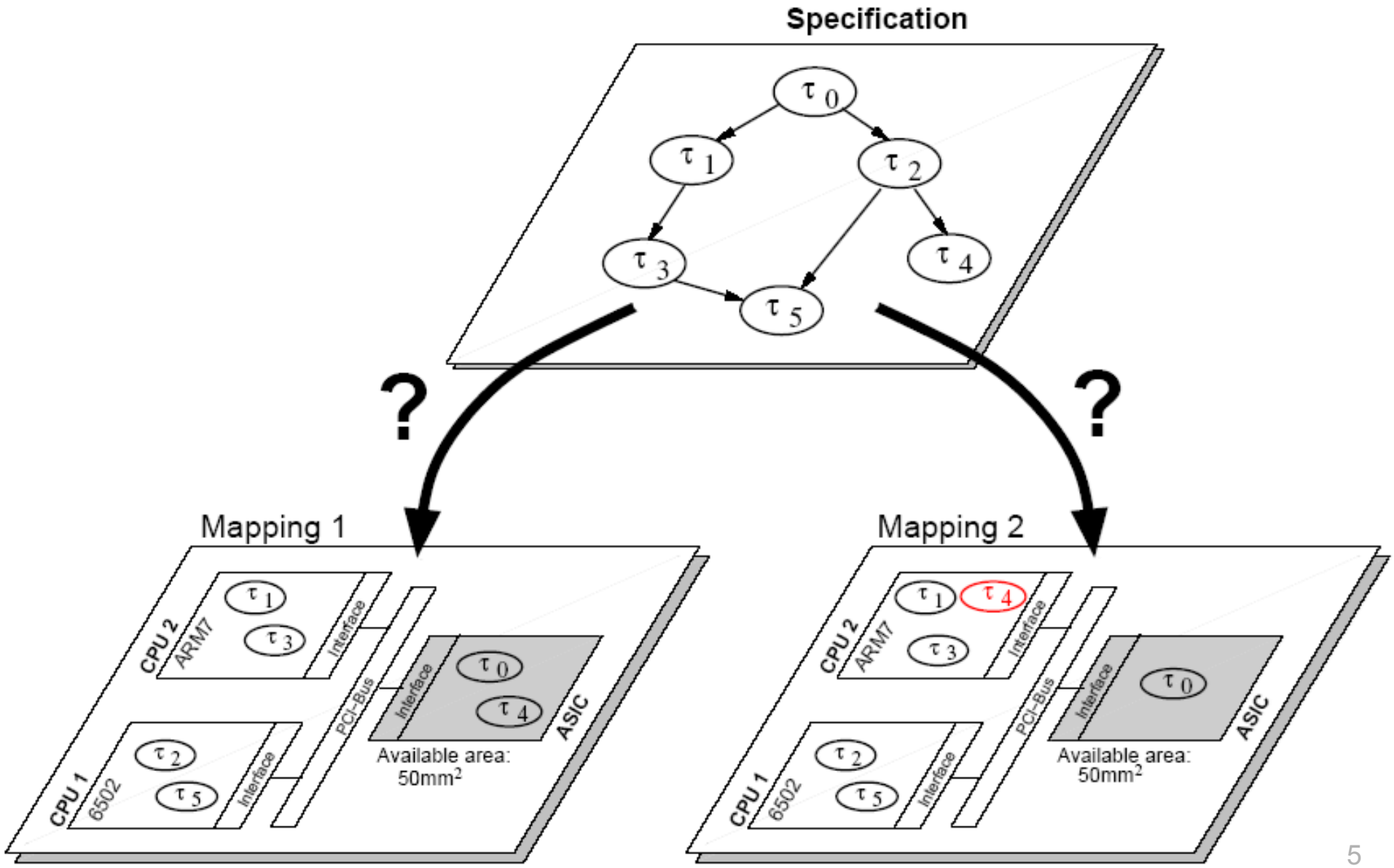
- **Task graph specification of an ES is not unique.**
  - **Example 1: Merge of tasks**



  - **Example 2: Splitting of tasks (Waiting for input)**



Hardware/Software Partitioning



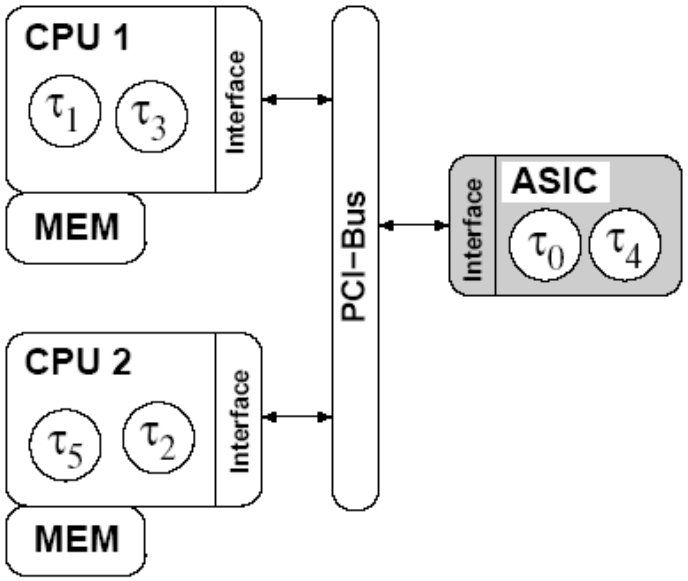
Task Execution Properties

Task	**CPU 1** (6502 @10*MHz*)		**CPU 2** (ARM7 @20*MHz*)		**ASIC** (50mm^2, Technology: 0.6μm)		
	t_{exe} (ms)	P_{dyn} (mW)	t_{exe} (ms)	P_{dyn} (mW)	t_{exe} (ms)	P_{dyn} (mW)	A (mm^2)
τ_0	89.3	3.6	12.1	23	1.8	0.13	7.76
τ_1	25.2	3.9	3.0	26	0.3	0.05	5.82
τ_2	19.7	4.4	2.8	28	0.2	0.07	9.71
τ_3	31.1	3.8	4.7	28	0.4	0.02	12.52
τ_4	172.2	3.9	22.3	27	2.7	0.12	8.05
τ_5	27.2	4.2	3.5	24	0.6	0.02	3.74

Scheduling

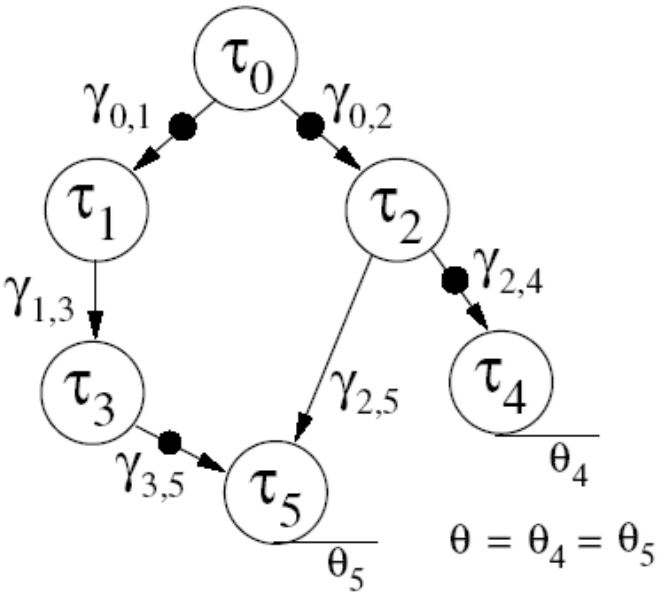
Consider the following partitioning

Architecture and Mapping



Spatial place of execution

Task Graph



Precedence constraints
(● =Communication via bus)

Scheduling (Cont.)

Two different scheduling for the same portioning.