PICO2-iCE

USBC Connector
J1 — USB_C_Receptacle_USB2.0
D5 MF-FSMF035X-2, PTC1, 1N5819WS
SHIELD

Peripheral(Default)/Host Selection
Host Mode: Solder open bridges, cut shorted bridges
Peripheral: Default

3.3V
U1 NCP115AMX330TCG
SJ6 SHORT
+3V3_FPGA

FPGA Power Note:
The FPGA is normally powered off the +3V3 supply.
If you want to conserve power and turn off the FPGA,
cut the jumper shorting the +3V3 and the +3V3_FPGA
and supply the +3V3_FPGA externally.
You may use an external load switch deriving power
from the +3V3 and controlled by the RP2350 for example.

FPGA 1.2V Core
U9 NCP115AMX120TCG
+1V2

Raspberry Pico
U3 Raspberry Pi RP2350B QFN-80 / RP2350_80QFN
Y1 ABM8-272-T3
Place R4/R5 close to RP2040
JST Debug Connector — J5 BM03B-SRSS-TB
https://datasheets.raspberrypi.com/rp2350/hardware-design-with-rp2350.pdf

Note:
Set the GPIO high to enable power to the
reference when the ADC needs to be calibrated.
Remove resistors to use the ADC on the external pins.

R12 1kx (Cathode current) > 0.5mA
Vref = 2.5V
U4 TL431DBZ

Power monitor:
Adding R29 makes it possible to connect directly
to the positive terminal of a nominally 3.6V
lithium battery. R29 is 2.2K so that a fully
charged battery at about 4V yields 3.3V on GPIO47_ADC7.
An external resistor in series with R29 allows for
higher battery voltages. R29 acts as a current
limiting resistor if ADC7 is misused,
e.g. connected directly to the positive terminal of a 12V battery

HSTX FPC Connector
J6 SFV22R-2STE1HLF
22 pin Top Contact 0.5mm FPC
ICE_35_G0 FPGA Clock
ICE_20_G3 Suggested data clock

Pico Flash
U2 W25Q32JVSSIQ
Note:
Add DNF if the Flash is
replaced with an SRAM.

SRAM
U5 APS6404L-3SQN-SN

RP2 LED
D2 MHPA1010RGBDT

PICO Button
SW1 BOOT
The button functions as a boot select
as well as GPIO.

R7 10K Hold FPGA in reset while the pico is coming up

Peripheral Headers
J2 / J3
iCE Flash
iCE PMOD
iCE Misc
iCE PMOD
BOOT|ADC
iCE Prog
iCE-Pico PMOD
LED/ADC
Pico PMOD
ADC/Power
USBC

FPGA Banks
Bank 0, Bank 2, Bank 1
U6A / U6B / U6C ICE40UP5K-SG48ITR
SJ5 SHORT
SJ3 SHORT
Bank 1 is 3.3V IO!

Note:
Bank 2 is selectable IO voltage!
To select non-3.3V, cut the shorted jumper
and supply external voltage (1.8-3.3V) on
VIO_BANK_2.

Output-only when the pll
is used for 2 output mode

FPGA Power
R11 100
U6D ICE40UP5K-SG48ITR
VCCPLL, VCC, VPP_2V5
D1 1N414BWT-7
SJ4 SHORT
Core current measurement

FPGA Flash
U8 W25Q32JVSSIQ

FPGA LED
D4 MHPA1010RGBDT
SJ2 SHORT

FPGA Button
SW2 SW_Push

FPGA Done LED
D3 LTST-C191KGKT

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Sheet: /
File: pico2-ice.kicad_sch
Title: PICO2-iCE
Size: A2   Date: 2024-09-23
KiCad E.D.A. 9.0.2
Id: 1/1
Rev: 0.2

LOGO4 OSHW ID: US002372
LOGO1 tinyVS Logo
LOGO2 WEEE Logo
LOGO3 Pb free Logo
H1-H4 MountingHole
FID1-FID6 Fiducial