Design of 8X3 Priority Encoder

Group Number : 21

Guided By :
Dr. Anuj Grover
TAs: Ali & Aditya

Group Members :
Amisha (MT25160)
Dushyant (MT25115)
Aditya (2023044)
Ronak (2023447)

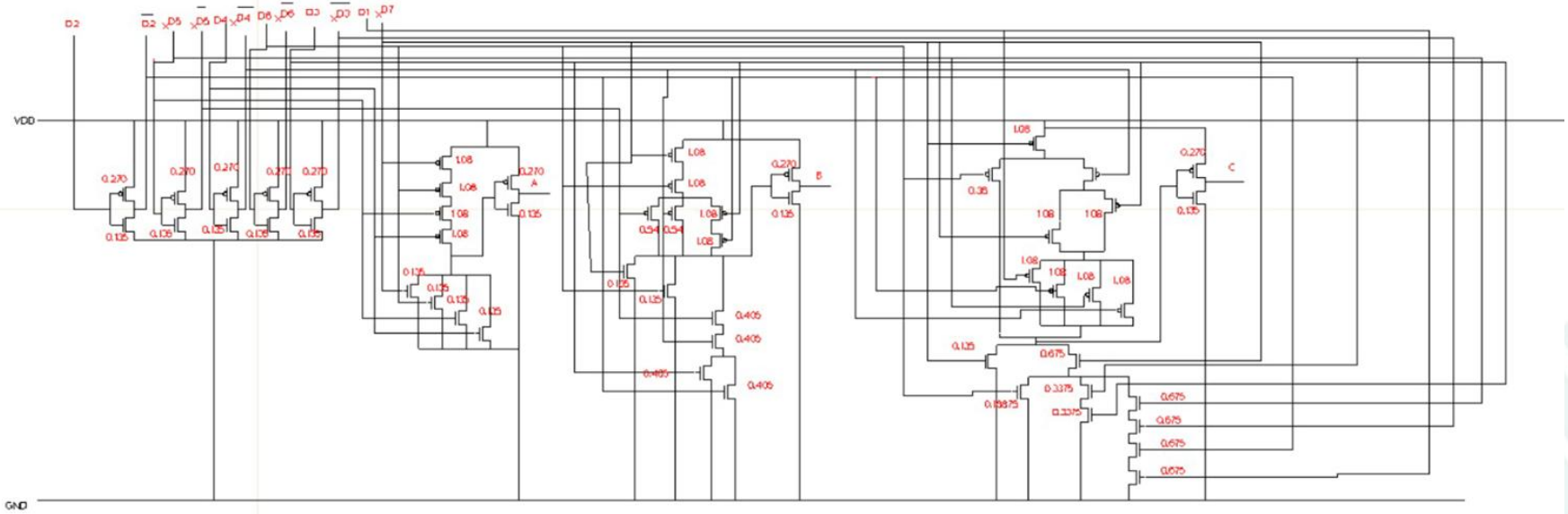
INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY **DELHI**

Schematic

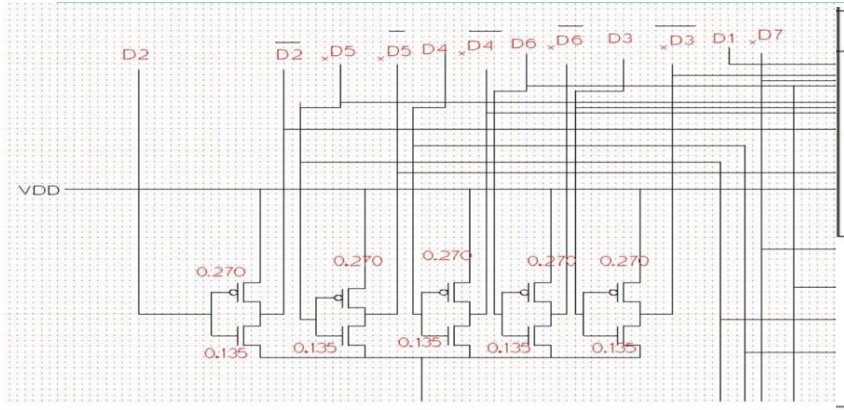
A = D7 + D6 + D5 + D4

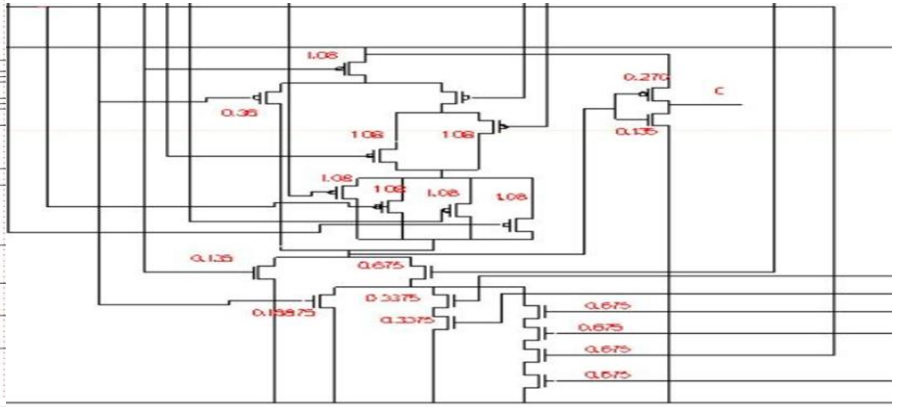
B = D7 + D6 + D5’ D4’ (D3 + D2)

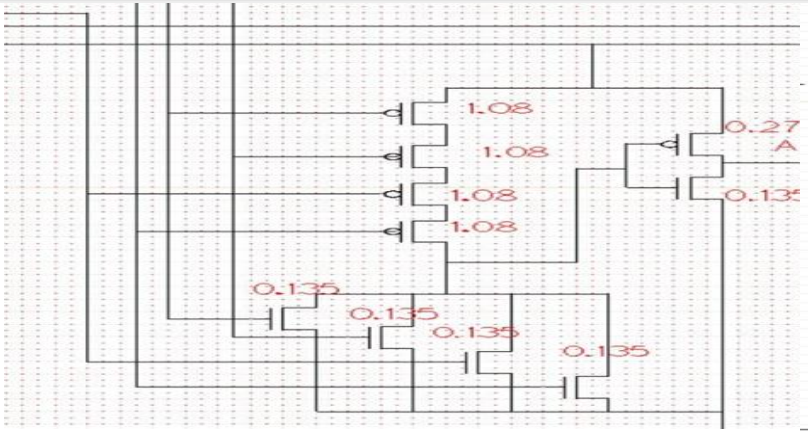
C = D7 + D6’ (D5 + D4’ D3 + D4’ D3’ D2’ D1)

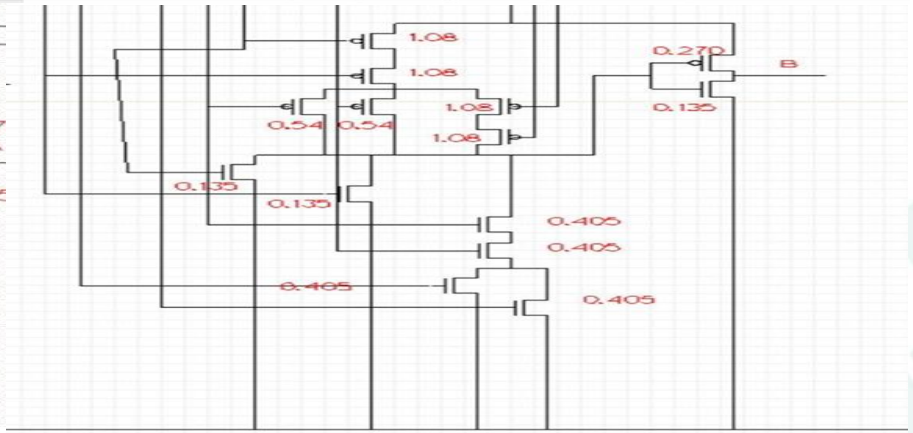


Sizing

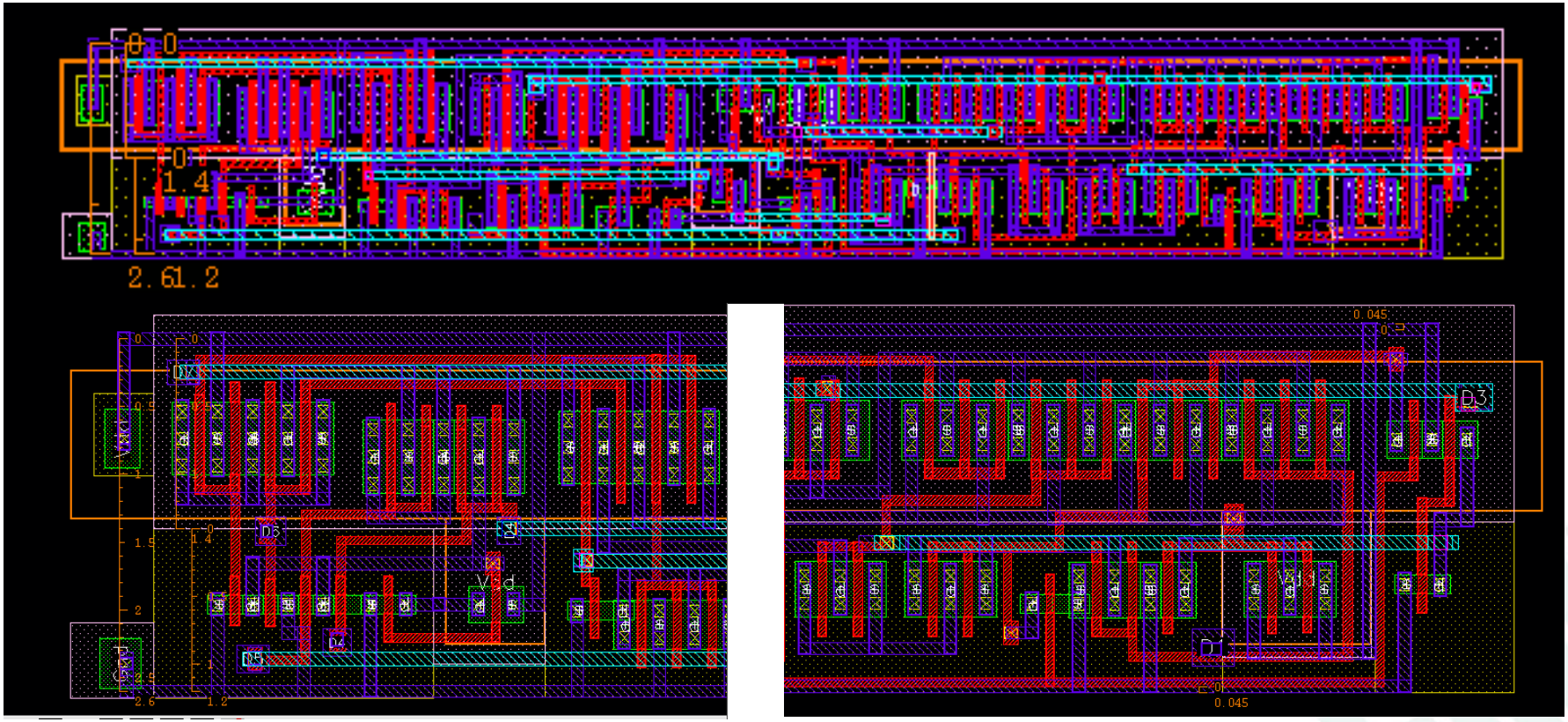

D2
D2
D5
D5
D4
D4
D6
D6
D3
D3
D1
D7
VDD
0.270
0.270
0.270
0.270
0.270
0.135
0.135
0.135
0.135
0.135


1.08
0.270
C
0.135
0.675


1.08
1.08
1.08
1.08
0.27
A
0.135
0.135
0.135
0.135
0.135

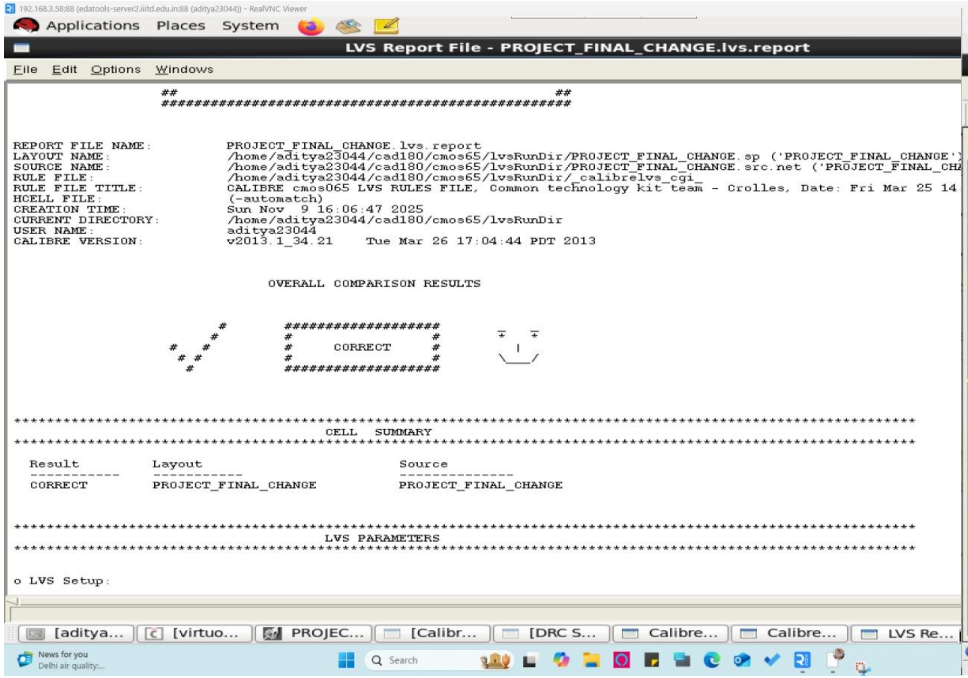

1.08
1.08
0.270
B
0.135
0.54
0.54
1.08
0.135
0.135
0.405
0.405
0.405
0.405

Layouts

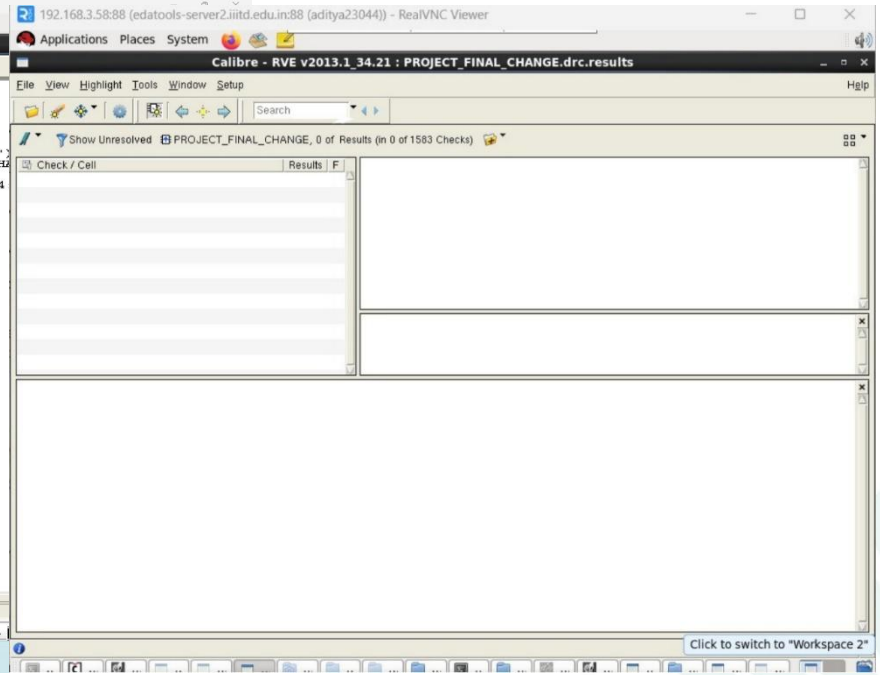


DRC/LVS Reports

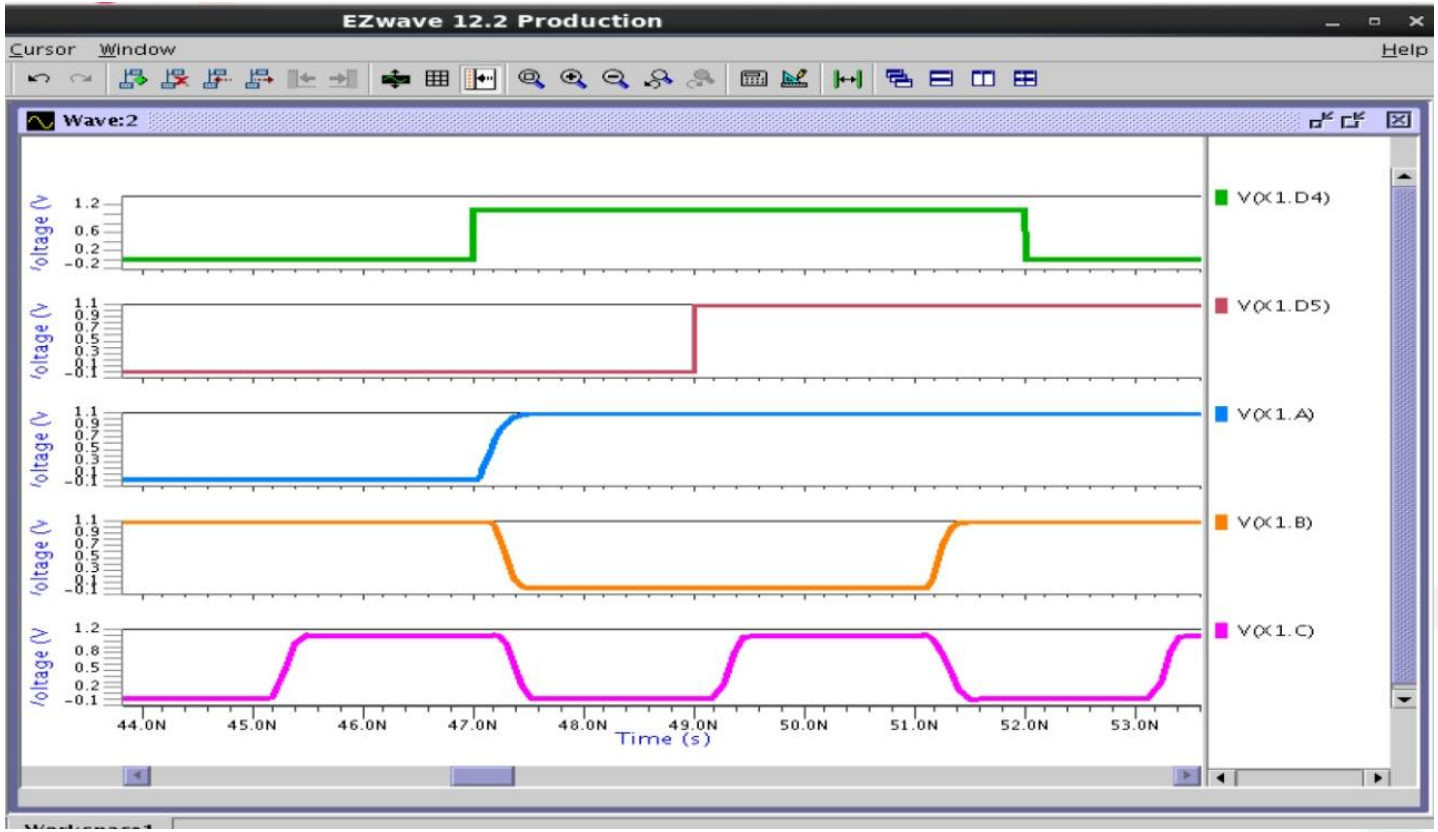
LVS Report



DRC Report



Layout Functionality Verification



Pre/Post Layout Stimulus

SS (Slow - Slow)

```
.include /modelfile_65nm/minNminP.cir
*.include /modelfile_65nm/typNtypP.cir

.include PROJECT_FINAL.src.net

*from netlist
X1 A B C D1 D2 D3 D4 D5 D6 D7 Gnd Vdd PROJECT_FINAL_CHANGE

.param SUPPLY = 1.08
.Param tend = 150n

.TEMP = 125

c1 A Gnd 10f    *Load capacitance
c2 B Gnd 10f
c3 C Gnd 10f

vd Vdd 0 SUPPLY
vg Gnd 0 0


*v0 D0 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v1 D1 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v2 D2 Gnd PULSE(0 SUPPLY 3n 10p 10p 5n 20n)
v3 D3 Gnd PULSE(0 SUPPLY 5n 10p 10p 5n 20n)
v4 D4 Gnd PULSE(0 SUPPLY 7n 10p 10p 5n 20n)
v5 D5 Gnd PULSE(0 SUPPLY 9n 10p 10p 5n 20n)
v6 D6 Gnd PULSE(0 SUPPLY 11n 10p 10p 5n 20n)
v7 D7 Gnd PULSE(0 SUPPLY 13n 10p 10p 5n 20n)
```

TT (Typical – Typical)

```
*.include /modelfile_65nm/minNminP.cir
.include /modelfile_65nm/typNtypP.cir

.include PROJECT_FINAL.src.net

*from netlist
X1 A B C D1 D2 D3 D4 D5 D6 D7 Gnd Vdd PROJECT_FINAL_CHANGE

.param SUPPLY = 1.2
.Param tend = 150n

.TEMP = 25

c1 A Gnd 10f    *Load capacitance
c2 B Gnd 10f
c3 C Gnd 10f

vd Vdd 0 SUPPLY
vg Gnd 0 0


*v0 D0 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v1 D1 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v2 D2 Gnd PULSE(0 SUPPLY 3n 10p 10p 5n 20n)
v3 D3 Gnd PULSE(0 SUPPLY 5n 10p 10p 5n 20n)
v4 D4 Gnd PULSE(0 SUPPLY 7n 10p 10p 5n 20n)
v5 D5 Gnd PULSE(0 SUPPLY 9n 10p 10p 5n 20n)
v6 D6 Gnd PULSE(0 SUPPLY 11n 10p 10p 5n 20n)
v7 D7 Gnd PULSE(0 SUPPLY 13n 10p 10p 5n 20n)
```

Pre/Post Layout Simulation Results

SS (Slow-Slow) Corner

Pre - Simulation

```
***>Current simulation completed

 TPLH_A =  1.6596E-10
 TPLH_B =  2.0451E-10
 TPLH_C =  2.5682E-10
 TPHL_A =  2.2331E-10
 TPHL_B =  2.8261E-10
 TPHL_C =  3.0842E-10
 LEAKAGE_CURRENT =  1.8737E-08
 DYNAMIC_POWER =  8.4793E-06

SIMULATION INFORMATION
memory size allocated in Mbytes  260.5
Latency: 0.000000%
average number of newton iterations: 3.004304
nb of components: 66
nb of nodes: 90
nb of MOS or BIP calls: 112192
Number of steps computed: 2091
```

Post - Simulation

```
***>Current simulation completed

 TPLH_A =  1.6775E-10
 TPLH_B =  2.0837E-10
 TPLH_C =  2.5979E-10
 TPHL_A =  2.2564E-10
 TPHL_B =  2.8686E-10
 TPHL_C =  3.1358E-10
 LEAKAGE_CURRENT =  1.8737E-08
 DYNAMIC_POWER =  8.6422E-06

SIMULATION INFORMATION
memory size allocated in Mbytes  306.8
Latency: 0.000000%
average number of newton iterations: 3.003335
nb of components: 4997
nb of nodes: 1219
nb of MOS or BIP calls: 116477
Number of steps computed: 2099
```

Pre/Post Layout Simulation Result

TT (Typical-Typical) Corner

Pre - Simulation

```
TPLH_A =  1.0758E-10
TPLH_B =  1.1509E-10
TPLH_C =  1.3819E-10
TPHL_A =  1.3501E-10
TPHL_B =  1.6846E-10
TPHL_C =  1.7185E-10
LEAKAGE_CURRENT =  1.8591E-09
DYNAMIC_POWER =  1.0016E-05


SIMULATION INFORMATION
memory size allocated in Mbytes  260.5
Latency: 0.000000%
average number of newton iterations: 3.011273
nb of components: 66
nb of nodes: 90
nb of MOS or BIP calls: 115294
Number of steps computed: 2129
```

Post - Simulation

```
TPLH_A =  1.0883E-10
TPLH_B =  1.1764E-10
TPLH_C =  1.3995E-10
TPHL_A =  1.3649E-10
TPHL_B =  1.7106E-10
TPHL_C =  1.7472E-10
LEAKAGE_CURRENT =  1.8465E-09
DYNAMIC_POWER =  1.0212E-05


SIMULATION INFORMATION
memory size allocated in Mbytes  306.7
Latency: 0.000000%
average number of newton iterations: 3.011273
nb of components: 4997
nb of nodes: 1219
nb of MOS or BIP calls: 119868
Number of steps computed: 2129
```

Work Distribution

AMISHA	DUSHYANT	ADITYA	RONAK
Layout, Pex, simulation, Power calculation	Layout, Pex, simulation, Power calculation	PPT, Sizing, Verification	PPT, Sizing, Verification