# Design of 8X3 Priority Encoder

Group Number: 21

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Ali & Aditya

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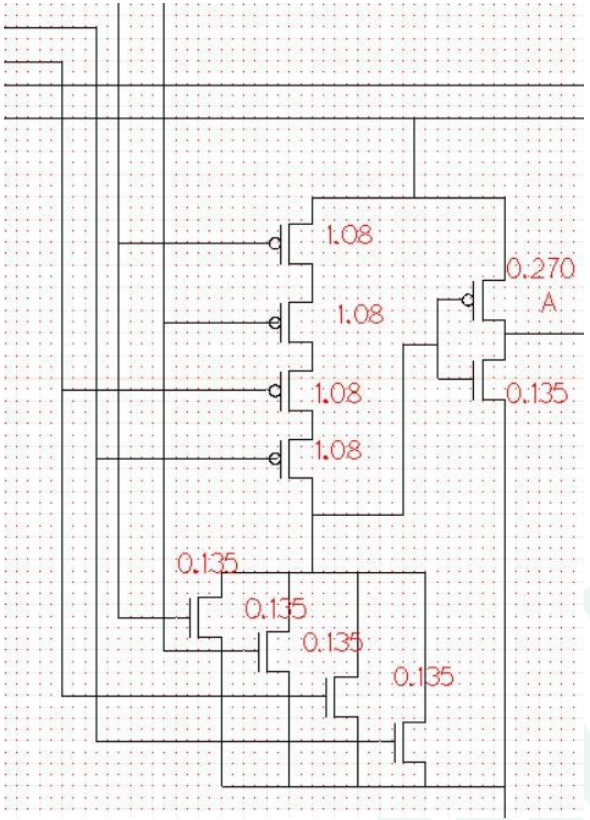
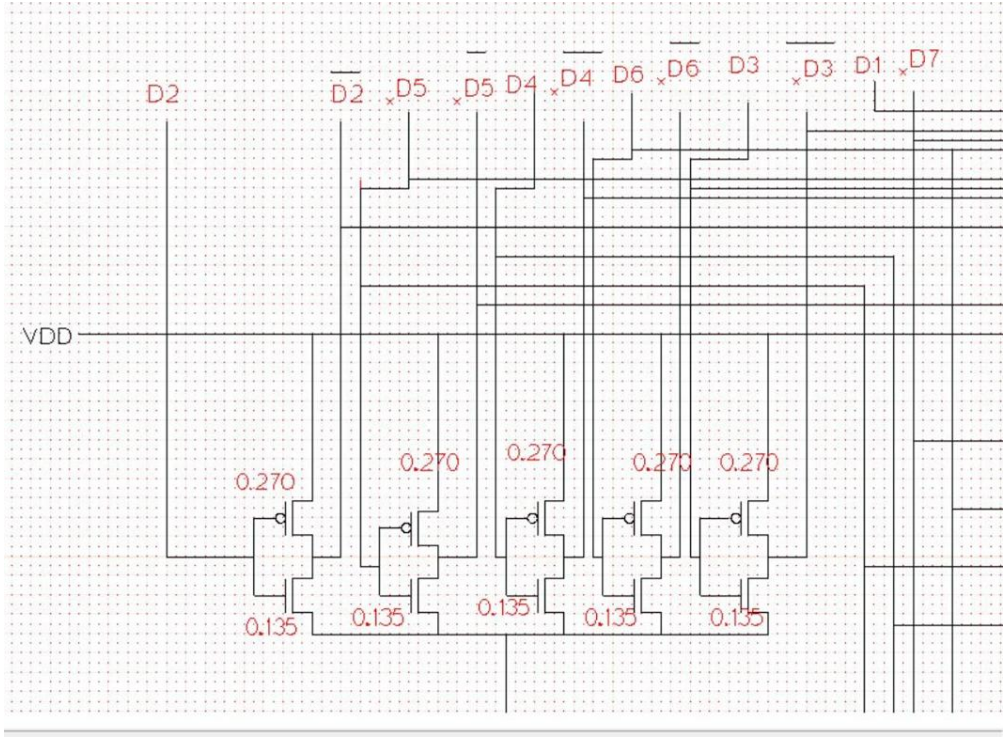
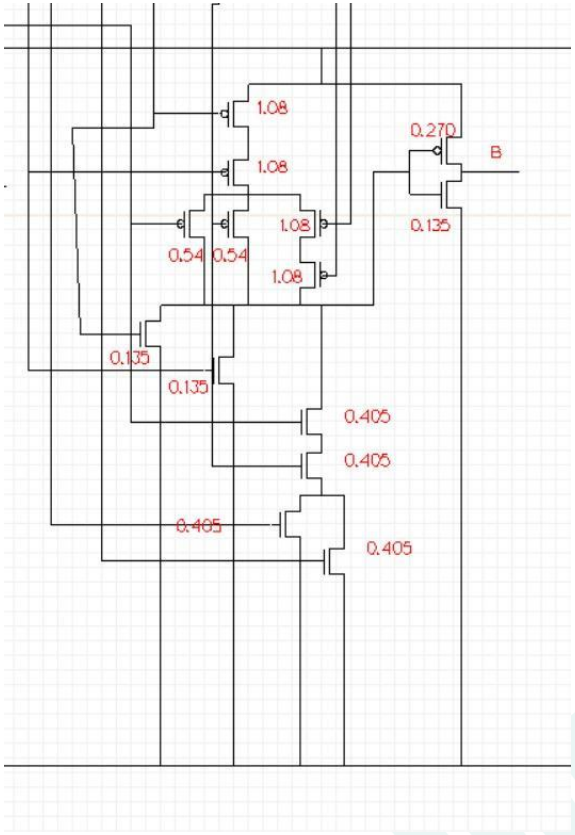
# Schematic + Sizing

A = D7 + D6 + D5 + D4
B = D7 + D6 + D5’ D4’ (D3 + D2)
C = D7 + D6’ (D5 + D4’ D3 + D4’ D3’ D2’ D1)

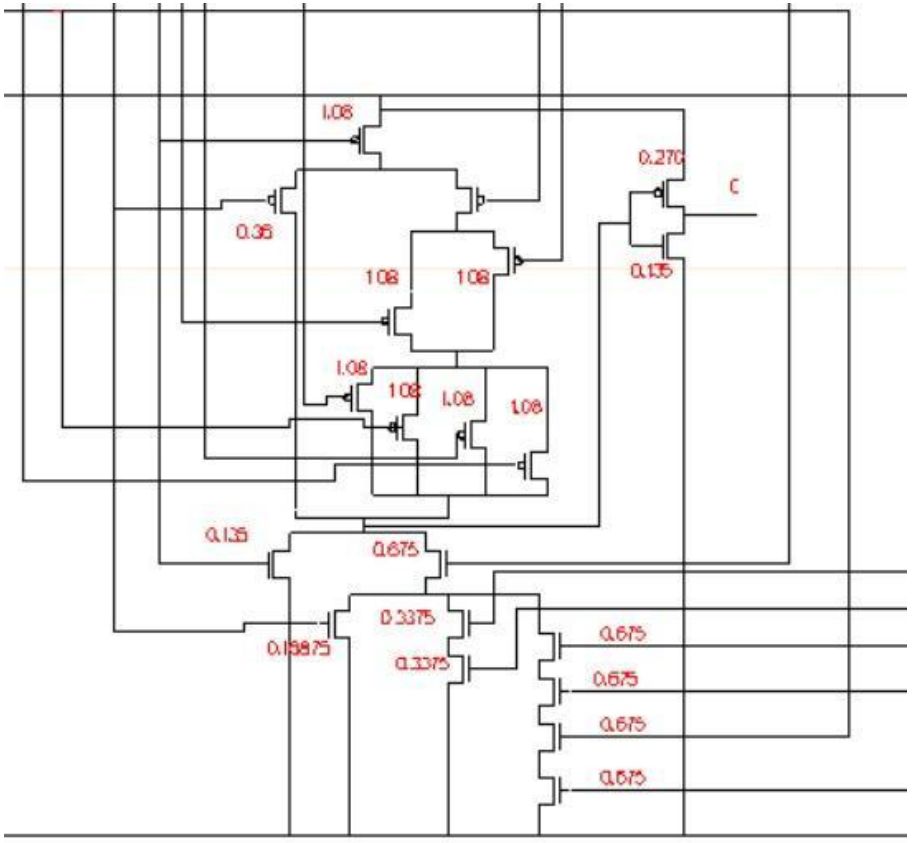


# Schematic + Sizing



# Schematic + Sizing



# Stimuli For Verification & Verification Plan

```
.include /modelfile_65nm/minNminP.cir
*.include /modelfile_65nm/typNtypP.cir

.include PROJECT2.src.net

*from netlist
X1 A B C D1 D2 D3 D4 D5 D6 D7 Gnd Vdd PROJECT

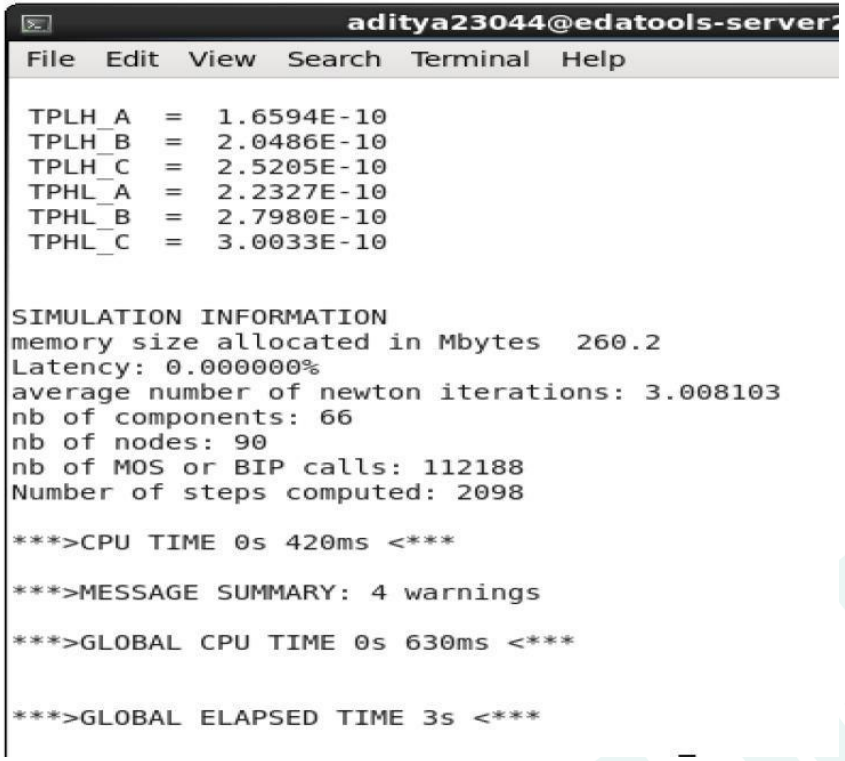
.param SUPPLY = 1.08
.Param tend = 150n

.TEMP = 125

c1 A Gnd 10f    *Load capacitance
c2 B Gnd 10f
c3 C Gnd 10f

vd Vdd 0 SUPPLY
vg Gnd 0 0


*v0 D0 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v1 D1 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v2 D2 Gnd PULSE(0 SUPPLY 3n 10p 10p 5n 20n)
v3 D3 Gnd PULSE(0 SUPPLY 5n 10p 10p 5n 20n)
v4 D4 Gnd PULSE(0 SUPPLY 7n 10p 10p 5n 20n)
v5 D5 Gnd PULSE(0 SUPPLY 9n 10p 10p 5n 20n)
v6 D6 Gnd PULSE(0 SUPPLY 11n 10p 10p 5n 20n)
v7 D7 Gnd PULSE(0 SUPPLY 13n 10p 10p 5n 20n)
```



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X1 A B C D1 D2 D3 D4 D5 D6 D7 Gnd Vdd PROJECT

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.Param tend = 150n

.TEMP = 125

c1 A Gnd 10f    *Load capacitance
c2 B Gnd 10f
c3 C Gnd 10f

vd Vdd 0 SUPPLY
vg Gnd 0 0


*v0 D0 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v1 D1 Gnd PULSE(0 SUPPLY 1n 10p 10p 5n 20n)
v2 D2 Gnd PULSE(0 SUPPLY 3n 10p 10p 5n 20n)
v3 D3 Gnd PULSE(0 SUPPLY 5n 10p 10p 5n 20n)
v4 D4 Gnd PULSE(0 SUPPLY 7n 10p 10p 5n 20n)
v5 D5 Gnd PULSE(0 SUPPLY 9n 10p 10p 5n 20n)
v6 D6 Gnd PULSE(0 SUPPLY 11n 10p 10p 5n 20n)
v7 D7 Gnd PULSE(0 SUPPLY 13n 10p 10p 5n 20n)
```

```
File  Edit  View  Search  Terminal  Help

 TPLH_A   =   1.3530E-10
 TPLH_B   =   1.5730E-10
 TPLH_C   =   1.8986E-10
 TPHL_A   =   1.7883E-10
 TPHL_B   =   2.1911E-10
 TPHL_C   =   2.3079E-10


SIMULATION INFORMATION
memory size allocated in Mbytes  260.2
Latency: 0.000000%
average number of newton iterations: 3.024964
nb of components: 66
nb of nodes: 90
nb of MOS or BIP calls: 111223
Number of steps computed: 2083

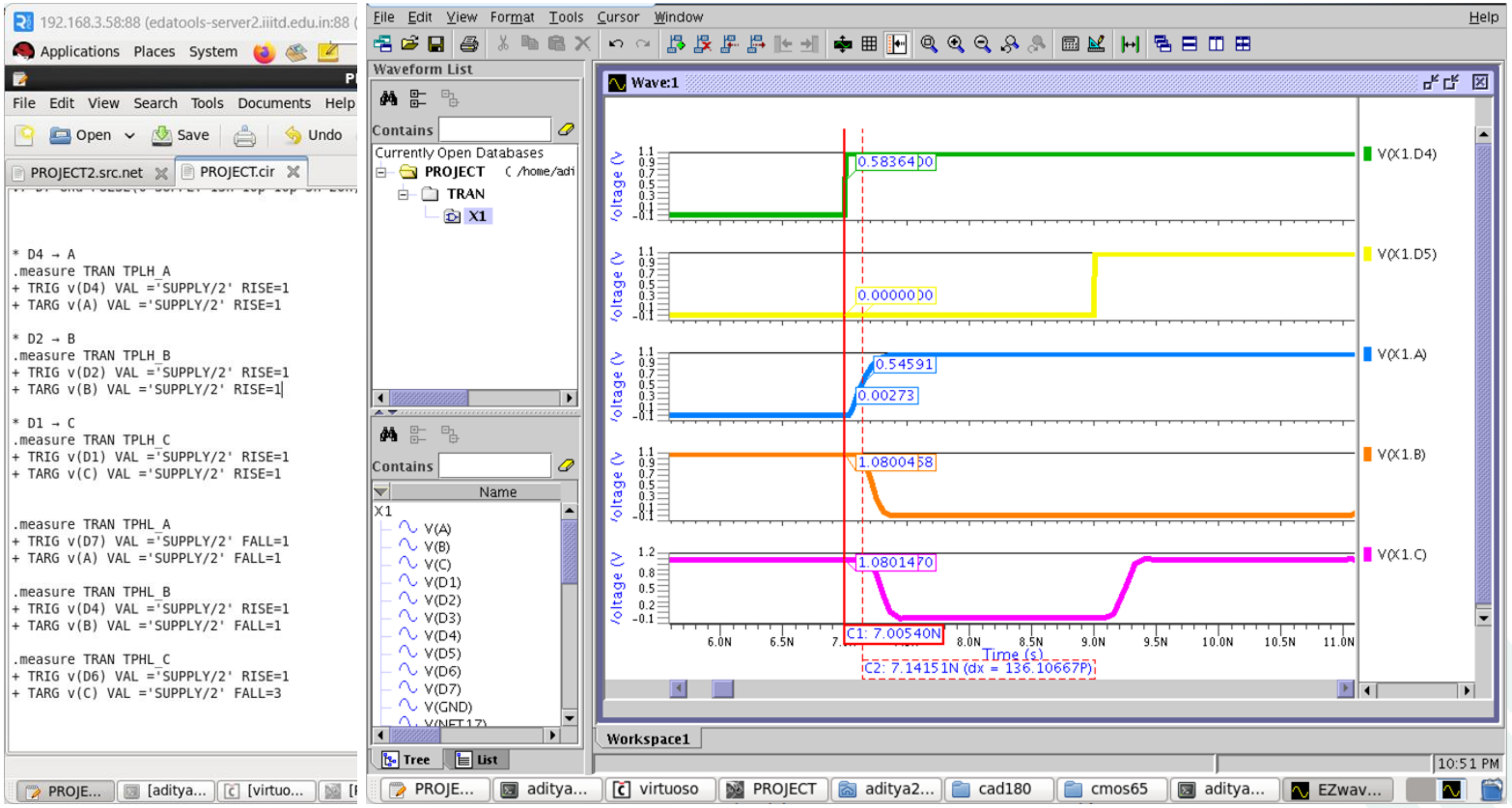
***>CPU TIME 0s 460ms <***

***>MESSAGE SUMMARY: 4 warnings

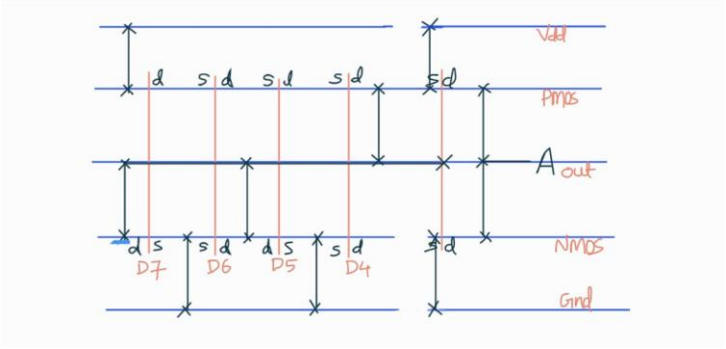
***>GLOBAL CPU TIME 0s 670ms <***

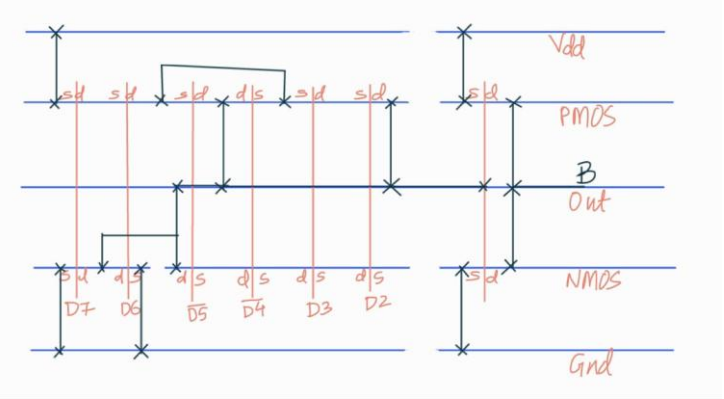

***>GLOBAL ELAPSED TIME 3s <***
```

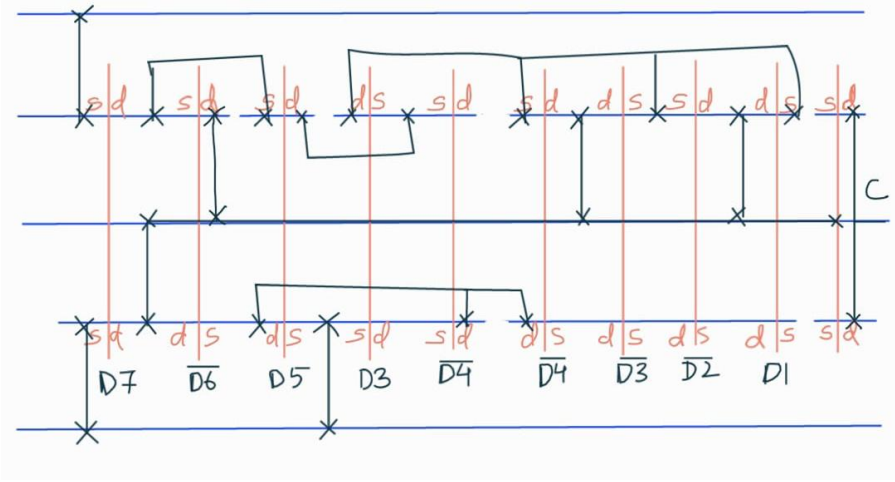
# Stimuli For Verification & Verification Plan



# Stick diagram



# Future Work + Work Distribution

| | |
|---|---|
| Amisha | Virtuoso Schematic, debugging & stick diagram |
| Dushyant | Functional verification & delay calculation |
| Aditya | Schematic & functional verification |
| Ronak | XCircuit schematic & sizing |

**Future Work Plans:**

1. Power calculation
2. Stick diagram optimization & Layout
3. Post layout simulations