A SYNCHRONOUS FREQUENCY DIVIDER WITH RING OSCILLATOR AS CLOCK CIRCUIT.

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ABSTRACT:

In this design, a 3-bit synchronous counter is implemented using Verilog code and Ring oscillator is implemented using CMOS logic. The clock frequency of a digital system may not be suitable for operation. Hence, we may need to change it. Module performing this is called frequency divider. Counters can be used for this purpose. The clock pulses for this counter are produced by a Ring Oscillator. A closed-loop cascade connection of any odd number of inverters will display astable behavior; such circuit are called ring oscillator.

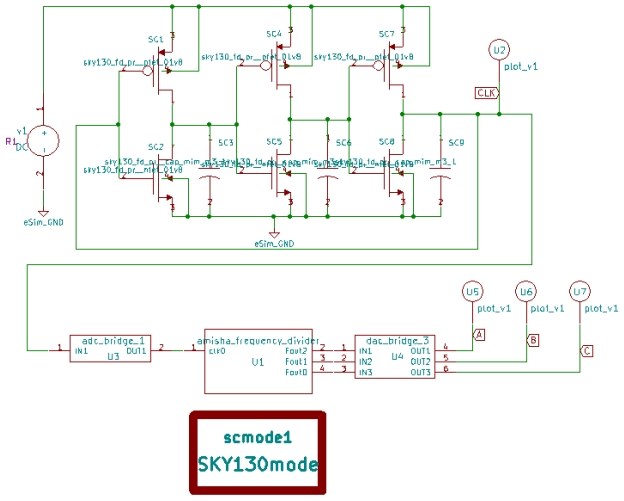
CIRCUIT DETAILS:

The T flip flops are useful when we need to reduce the frequency of the clock signal. If we use the original clock as flip flop clock and keep the T input at logic high then the output changes state once per clock period. This is with the assumption that the flip flop is not sensitive to both clock edges. This makes the output clock frequency as half of the frequency of the input clock. So the T flip flop works as a "Frequency Divider Circuit".

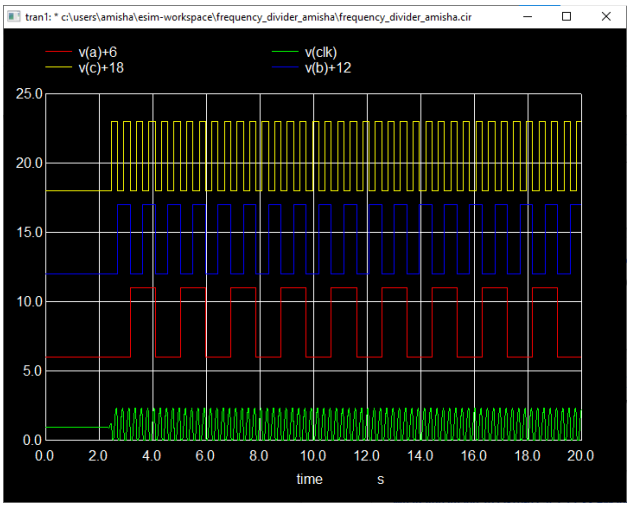
If we connect three T-type flip-flops, the initial input frequency will be "divided-by-two" by the first flip-flop ($f \div 2$) and then "divided-by-two" again by the second flip-flop ($f \div 2$) $\div 2$, and then "divided by two" again by the third flip-flop (($f \div 2$) $\div 2$) $\div 2$ giving an output frequency which has effectively been divided eight times, then its output frequency becomes one quarter value (12.5%) of the original clock frequency, ($f \div 8$).

The designing of the ring oscillator can be done using three inverters. If the oscillator is employed with a single-stage, then the oscillations & gain are not sufficient. If the oscillator has two inverters, then the oscillation and gain of the system are a little bit more than the single-stage ring oscillator. So this three-stage oscillator has three inverters that are connected in the form of series with a positive feedback system. So the oscillations & the gain of the system are sufficient. This is the reason to choose the three-stage oscillator. Ring oscillator uses an odd number of inverters to achieve more gain than a single inverting amplifier. The inverter gives a delay to the input signal and if the numbers of inverters are increases then oscillator frequency will be decreased. So the desired oscillator frequency depends on the number of inverter stages of the oscillator. The s frequency of oscillation formula for this oscillator is f=1/ (2nT).

IMPLEMENTED CIRCUIT DESIGN:



IMPLEMENTED CIRCUIT WAVEFORM:



REFERENCES:

(1) https://dcaclab.com/blog/t-flip-flop-explained-in-detail/