INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Electronics and Communication Engineering Department

3rd Year

CMOS

Project Title :– 1 : 2 Demultiplexer

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ACKNOWLEDGEMENT

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ABSTRACTION

The project "1:2 demultiplexer" is a digital circuit design implemented using Complementary Metal-Oxide-Semiconductor (CMOS) technology. The demultiplexer is a combinational circuit that accepts a single input and directs it to one of two possible outputs based on the value of the select input. The project aims to design and implement a 1:2 demultiplexer using CMOS technology.

The design of the demultiplexer is based on the principles of Boolean algebra and logic gates.

The project involves designing the circuit, simulating it using software tools, and then implementing it using CMOS technology. The design process involves selecting the appropriate components, sizing them, and connecting them in the correct configuration. The simulation process involves verifying the functionality of the circuit and identifying any errors or issues that need to be addressed before implementation.

The implementation process involves fabricating the circuit using CMOS technology, which involves depositing and patterning multiple layers of materials on a silicon substrate. The fabricated circuit is then tested to verify its functionality and performance.

The project aims to develop a better understanding of CMOS technology and digital circuit design principles. It also serves as a practical application of the theory learned in the classroom, allowing students to gain hands-on experience in designing, simulating, and implementing digital circuits.

INTRODUCTION

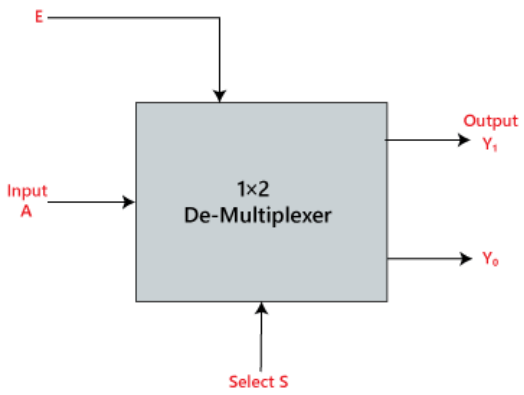
A De-multiplexer is a combinational circuit that has only 1 input line and 2^N output lines. Simply, the multiplexer is a single-input and multi-output combinational circuit. The information is received from the single input lines and directed to the output line. On the basis of the values of the selection lines, the input will be connected to one of these outputs. De-multiplexer is opposite to the multiplexer.

Unlike encoder and decoder, there are n selection lines and 2^n outputs. So, there is a total of 2^n possible combinations of inputs. De-multiplexer is also treated as **De-mux**.

1×2 De-multiplexer:

In the 1 to 2 De-multiplexer, there are only two outputs, i.e., Y_0, and Y_1, 1 selection lines, i.e., S_0, and single input, i.e., A. On the basis of the selection value, the input will be connected to one of the outputs. The block diagram and the truth table of the 1×2 multiplexer are given below.

Block Diagram



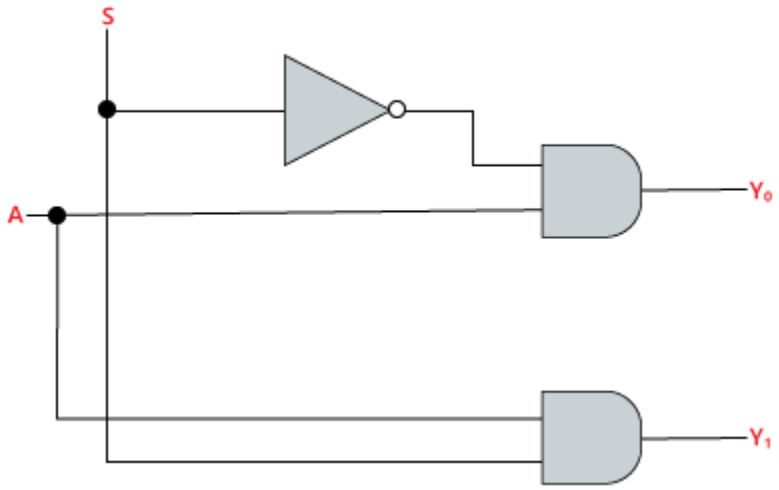
Truth Table:

INPUTS	Output	
S_0	Y_1	Y_0
0	0	A
1	A	0

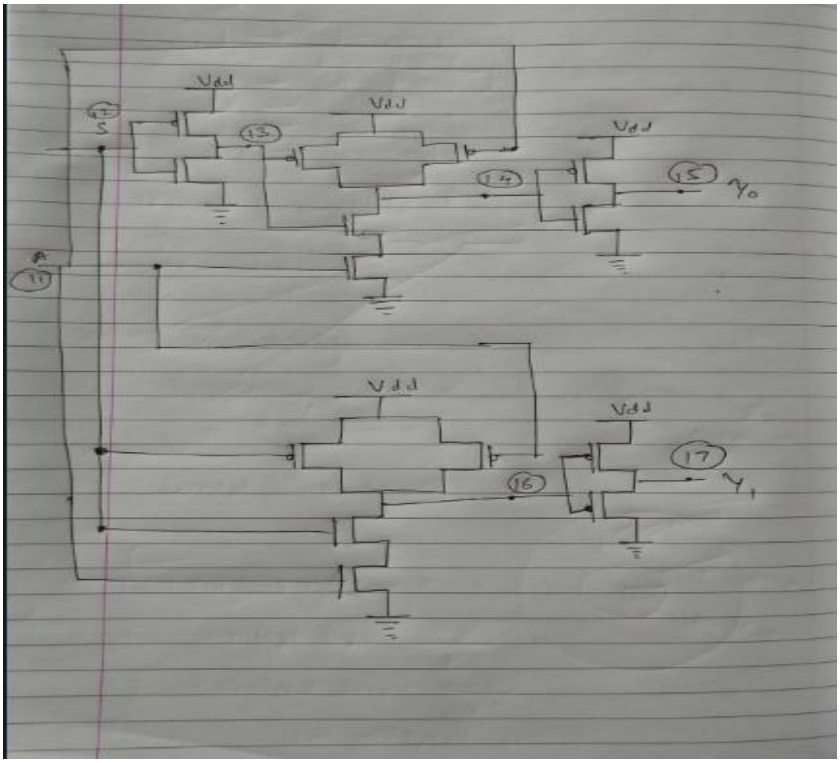
The logical expression of the term Y is as follows:

$$Y_0 = S_0'.A$$
$$Y_1 = S_0.A$$

Logical circuit of the above expressions is given below:



Circuit Diagram of CMOS Implementation of 1 : 2 Demultiplexer



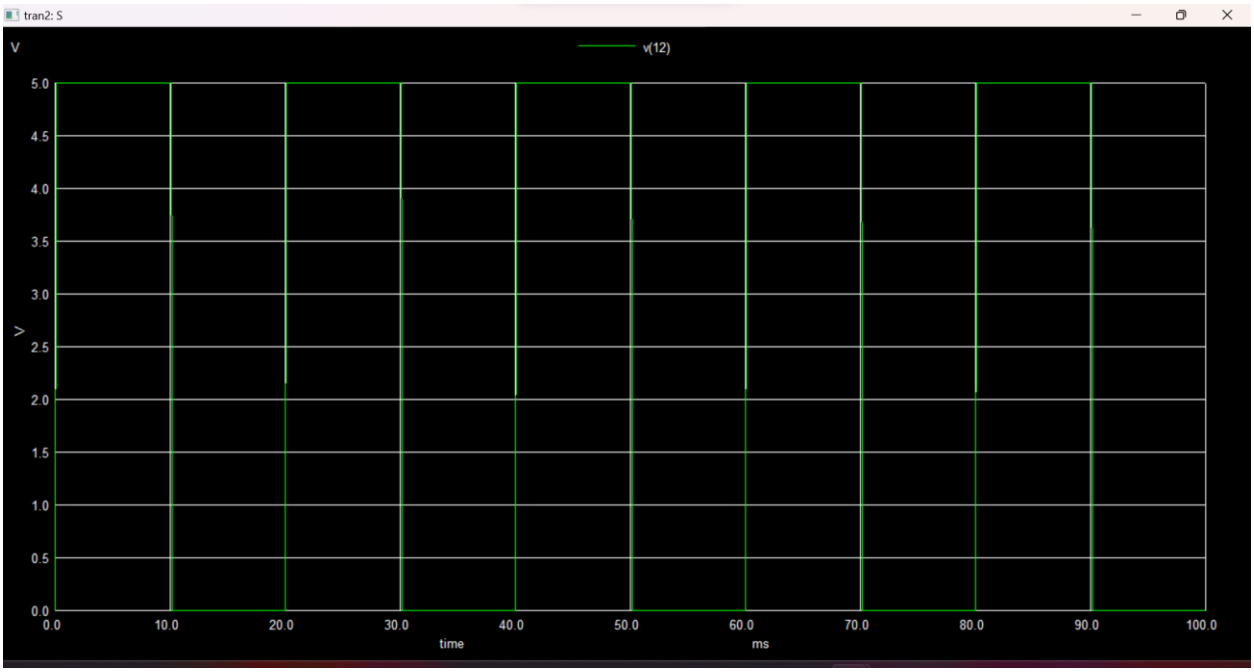
NETLIST

```
.subckt invertor_ckt 1 3 2

.model nmod nmos level=54 version=4.7

.model pmod pmos level=54 version=4.7

M1 2 1 0 0 nmod w=100u l=10u

M2 2 1 3 3 pmod w=100u l=10u

.ends


.subckt NAND_CKT 1 2 3 4

.model nmod nmos level=54 version=4.7

.model pmod pmos level=54 version=4.7

M1 5 1 0 0 nmod w=100u l=10u

M2 4 2 5 5 nmod w=100u l=10u

M3 4 2 3 3 pmod w=100u l=10u

M4 4 1 3 3 pmod w=100u l=10u

.ends


Va 11 0 pulse(0 5 0 0 0 20m 40m)

Vb 12 0 pulse(0 5 0 0 0 10m 20m)

Vdd 3 0 dc 5v
```

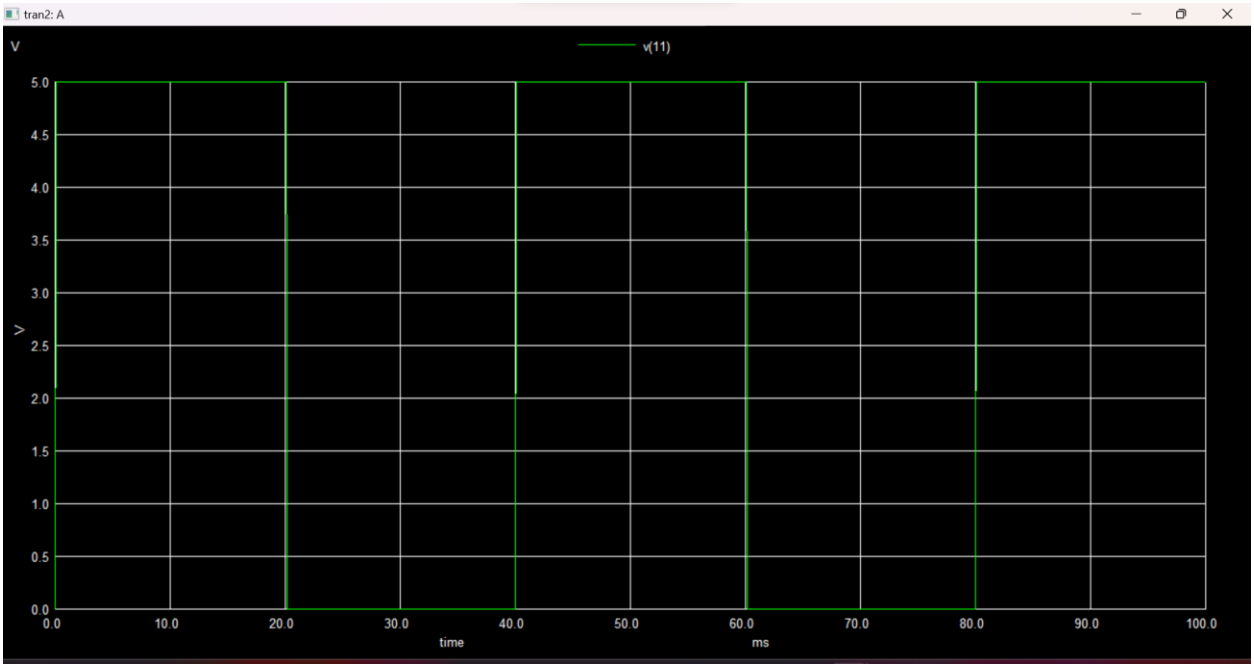
```
Xinvert 12 3 13 invertor_ckt

Xnand_1 11 13 3 14 NAND_CKT

Xinvert_1 14 3 15 invertor_ckt

Xnand_2 11 12 3 16 NAND_CKT

Xinvert_2 16 3 17 invertor_ckt


.tran 0.1m 100m

.control

run

plot V(11) xlabel 'time' ylabel 'V' title 'A'

plot V(12) xlabel 'time' ylabel 'V' title 'S'

plot V(15) xlabel 'time' ylabel 'V' title 'Y0'

plot V(17) xlabel 'time' ylabel 'V' title 'Y1'

.endc

.end
```

NETLIST Graphs

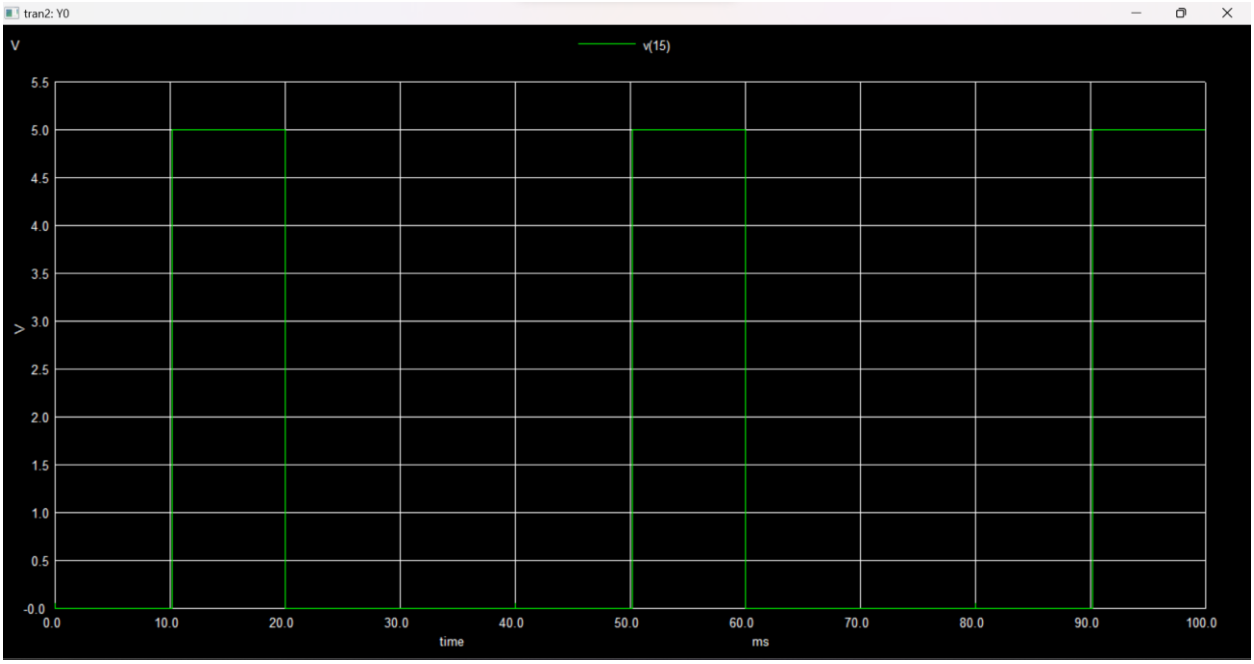
S signal waveform



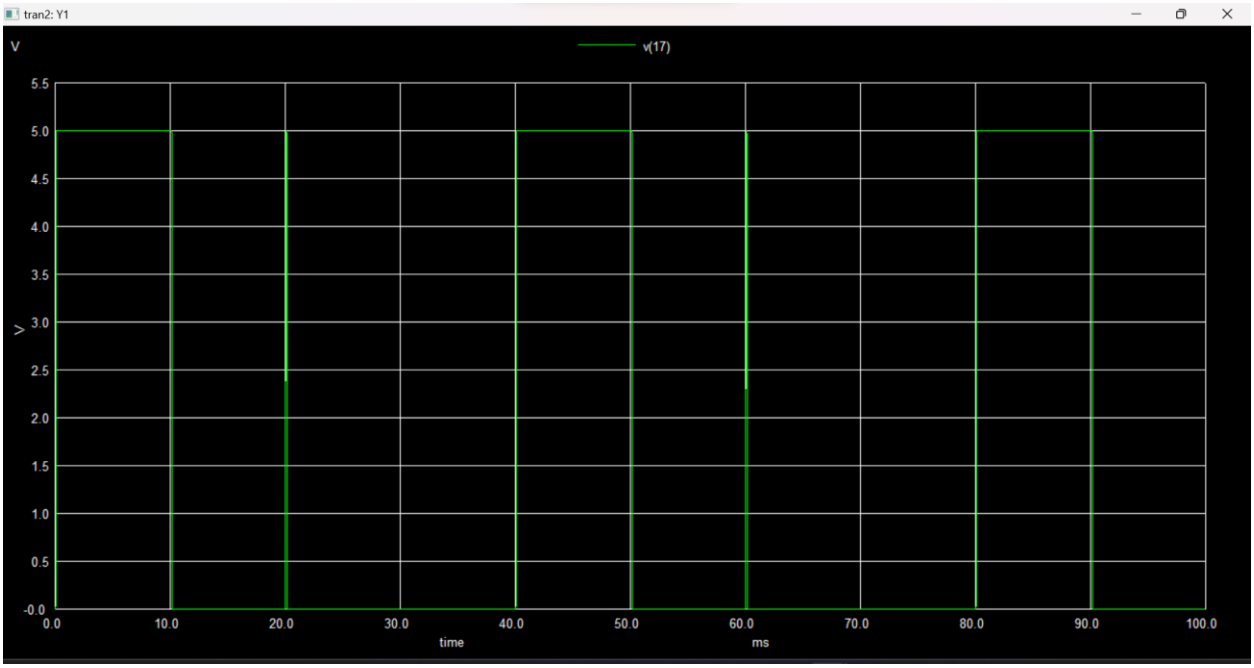
A signal waveform



Y0 Output waveform

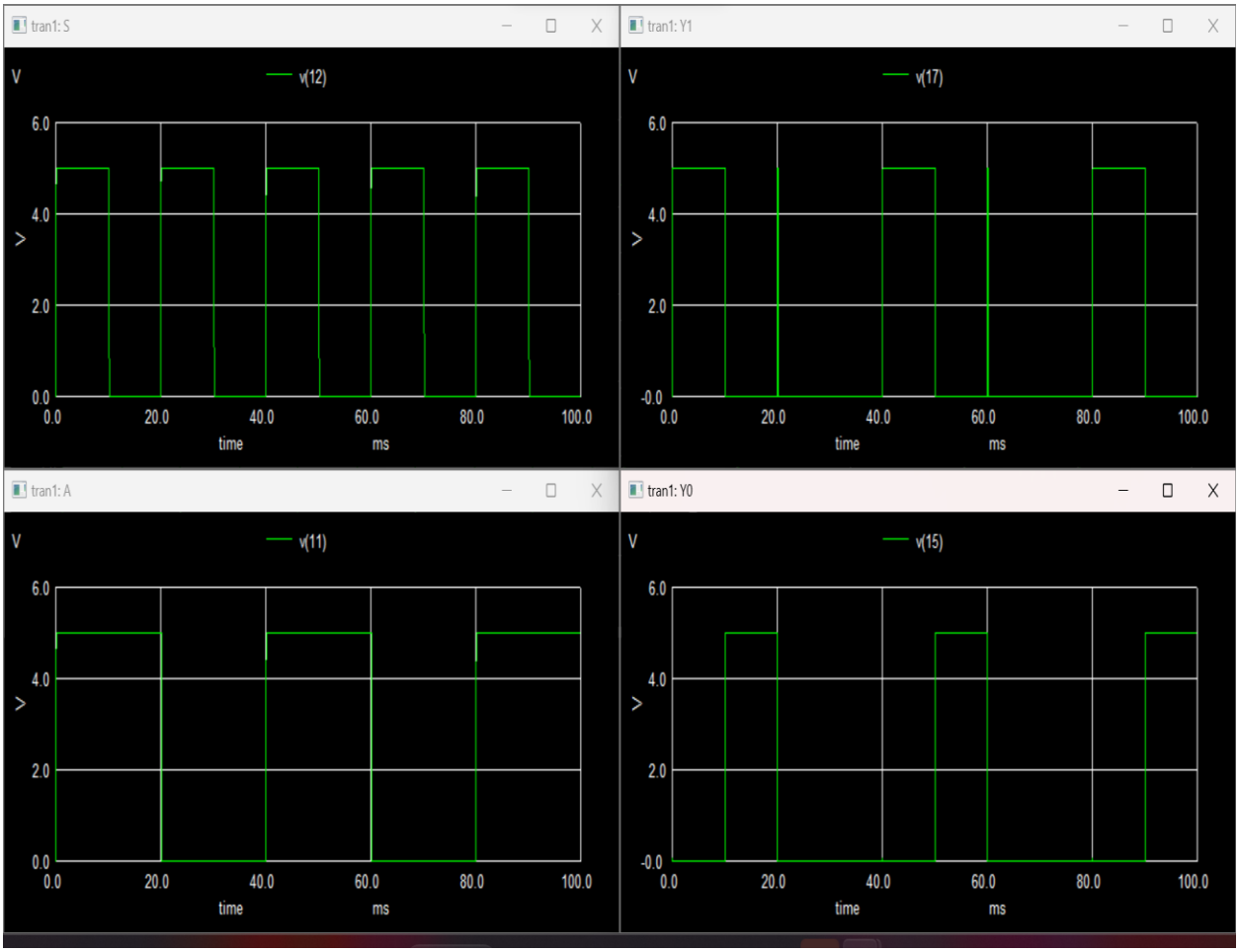


Y1 Output waveform

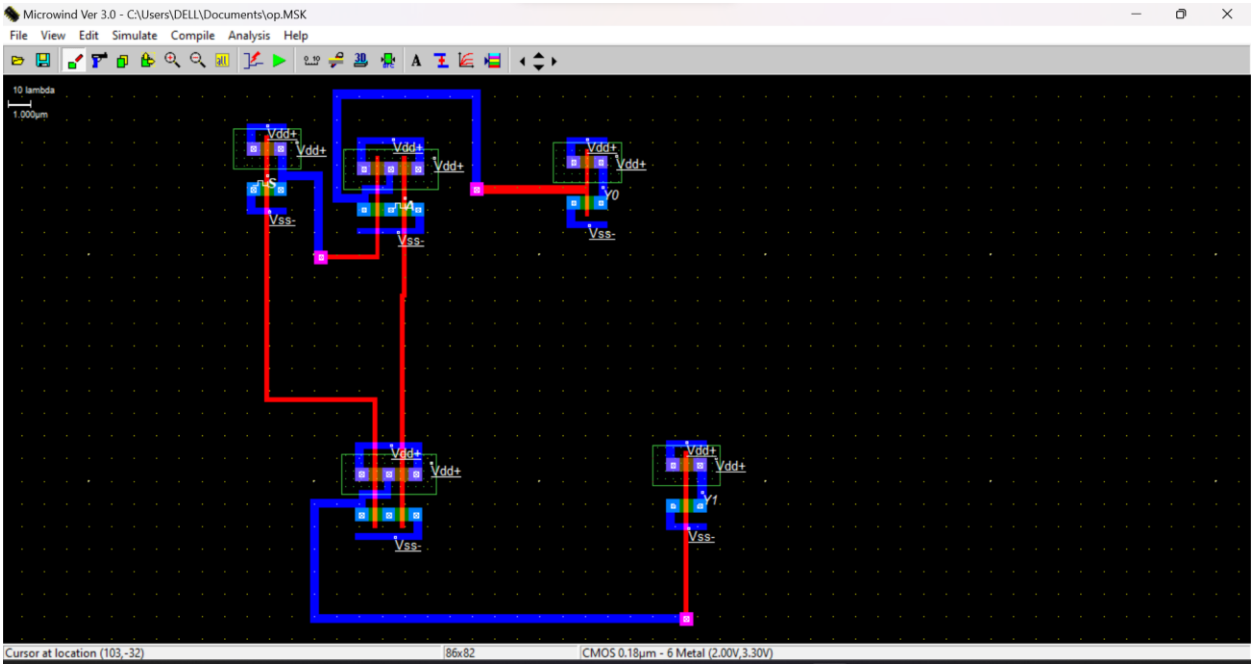


Netlist Graph

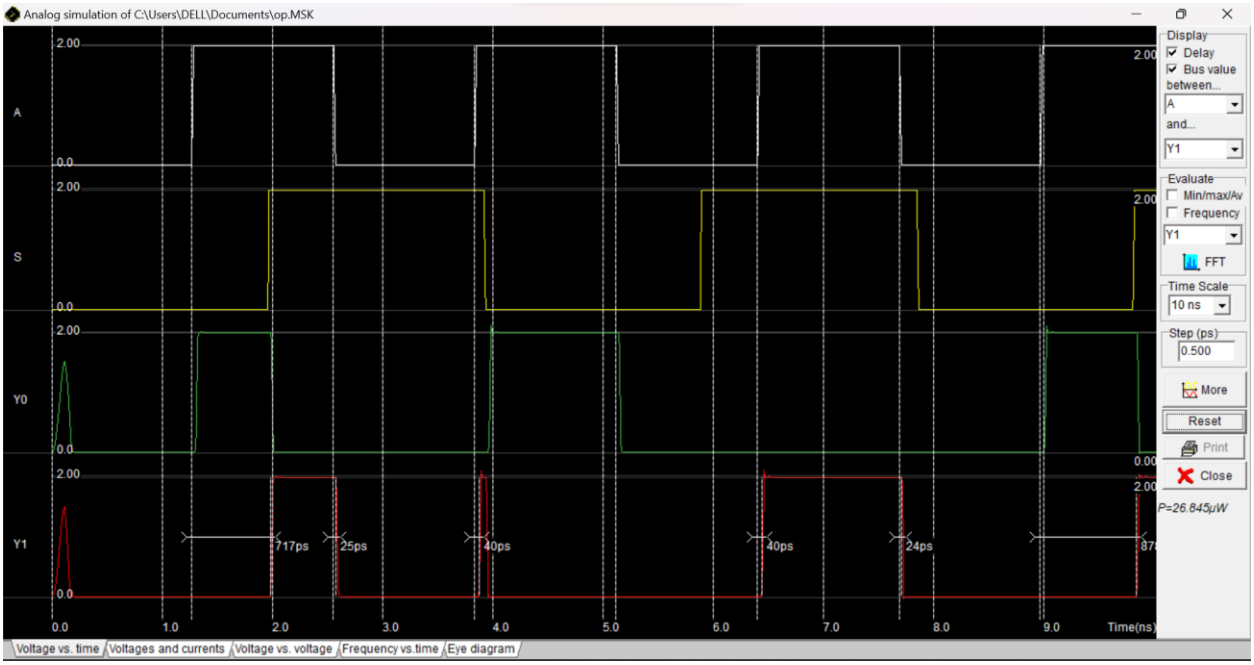
Compact View

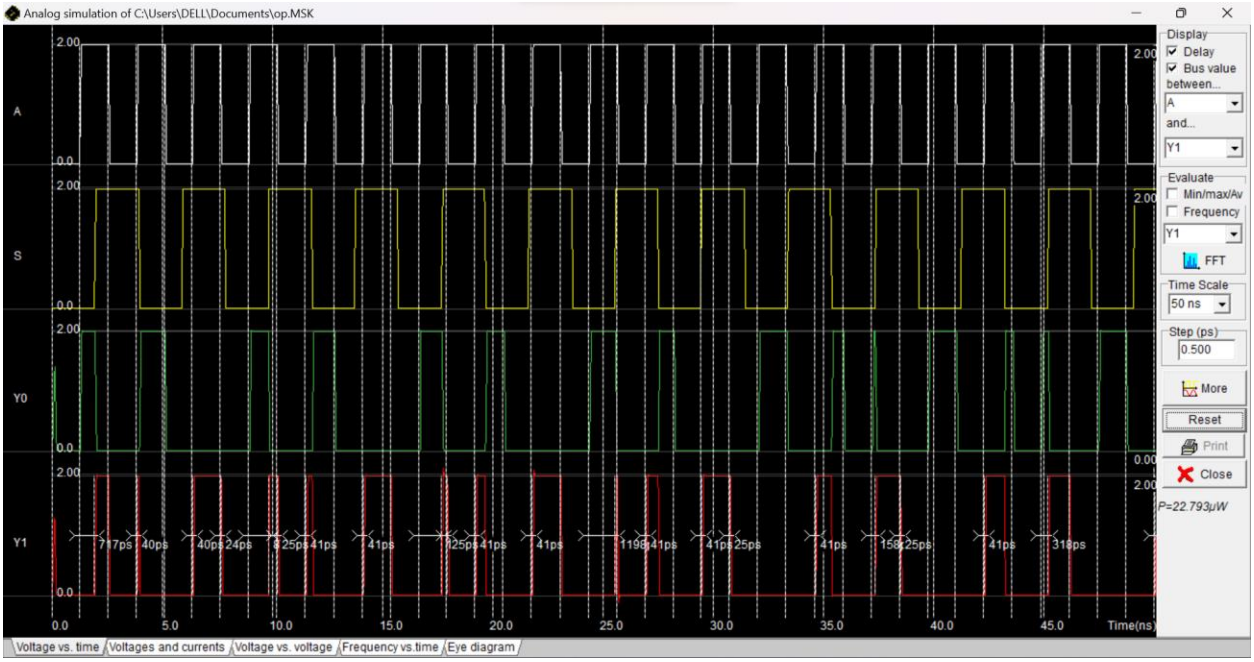


Microwind Layout



Graph




Analog simulation of C:\Users\DELL\Documents\op.MSK
A
S
Y0
Y1
2.00
0.0
717ps
40ps
40ps
24ps
25ps
41ps
41ps
25ps
41ps
41ps
1198ps
41ps
41ps
25ps
41ps
158ps
25ps
41ps
318ps
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
Time(ns)
Display
Delay
Bus value
between...
A
and...
Y1
Evaluate
Min/max/Av
Frequency
Y1
FFT
Time Scale
50 ns
Step (ps)
0.500
More
Reset
Print
Close
P=22.793μW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

RESULT

The graphs generated from the simulation of the netlist code written in the **ngspice** matches with the graphs generated from the layout designed in the **Microwind.**

Thus, we have successfully designed the 1 : 2 demultiplexer both on ***ngspice*** and ***Microwind***.