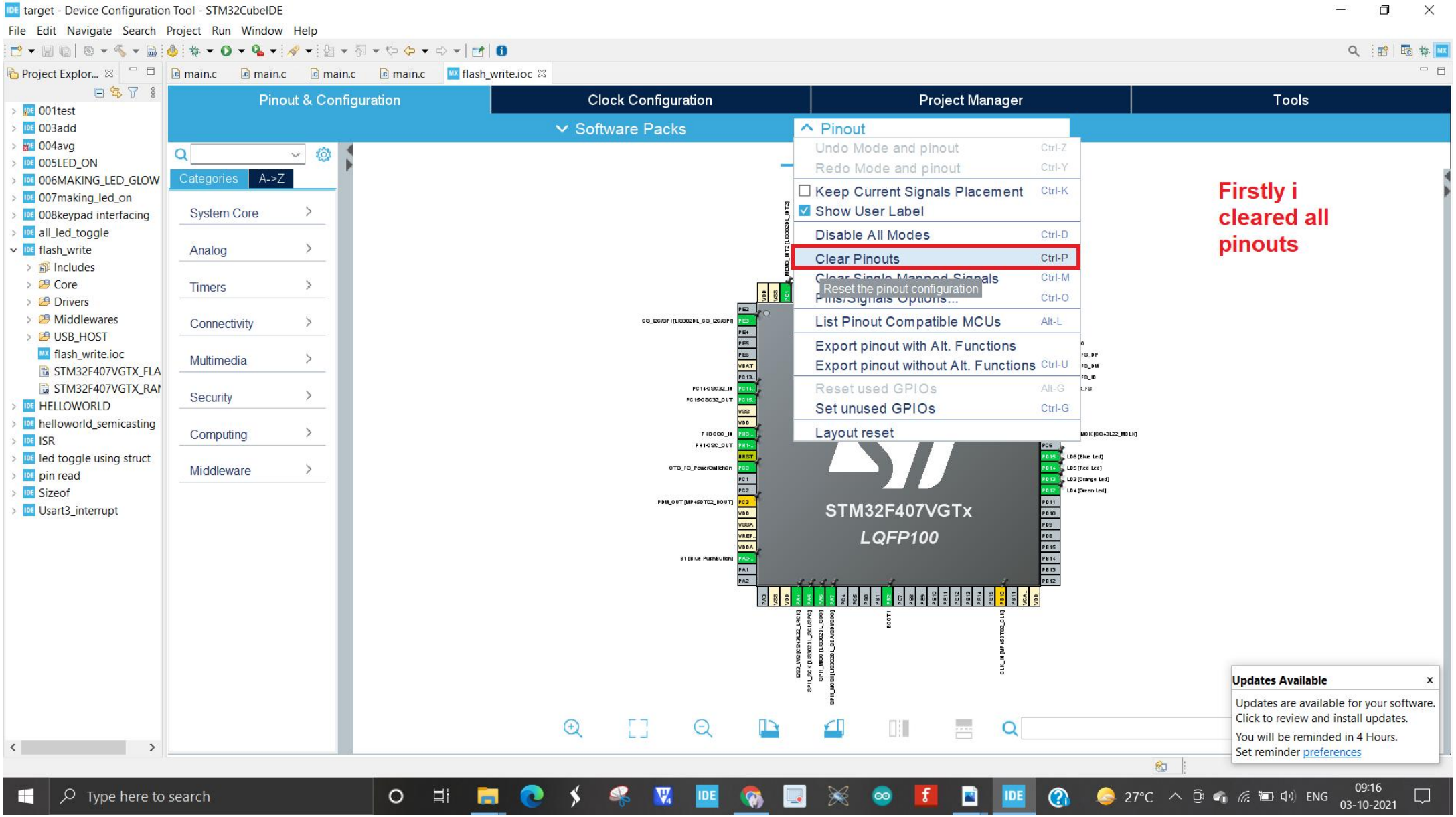
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006MAKING_LED_GLOW
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Pinout
Undo Mode and pinout Ctrl-Z
Redo Mode and pinout Ctrl-Y
Keep Current Signals Placement Ctrl-K
Show User Label
Disable All Modes Ctrl-D
Clear Pinouts Ctrl-P
Clear Single Mapped Signals Ctrl-M
Pins/Signals Options... Ctrl-O
Reset the pinout configuration
List Pinout Compatible MCUs Alt-L
Export pinout with Alt. Functions
Export pinout without Alt. Functions Ctrl-U
Reset used GPIOs Alt-G
Set unused GPIOs Ctrl-G
Layout reset
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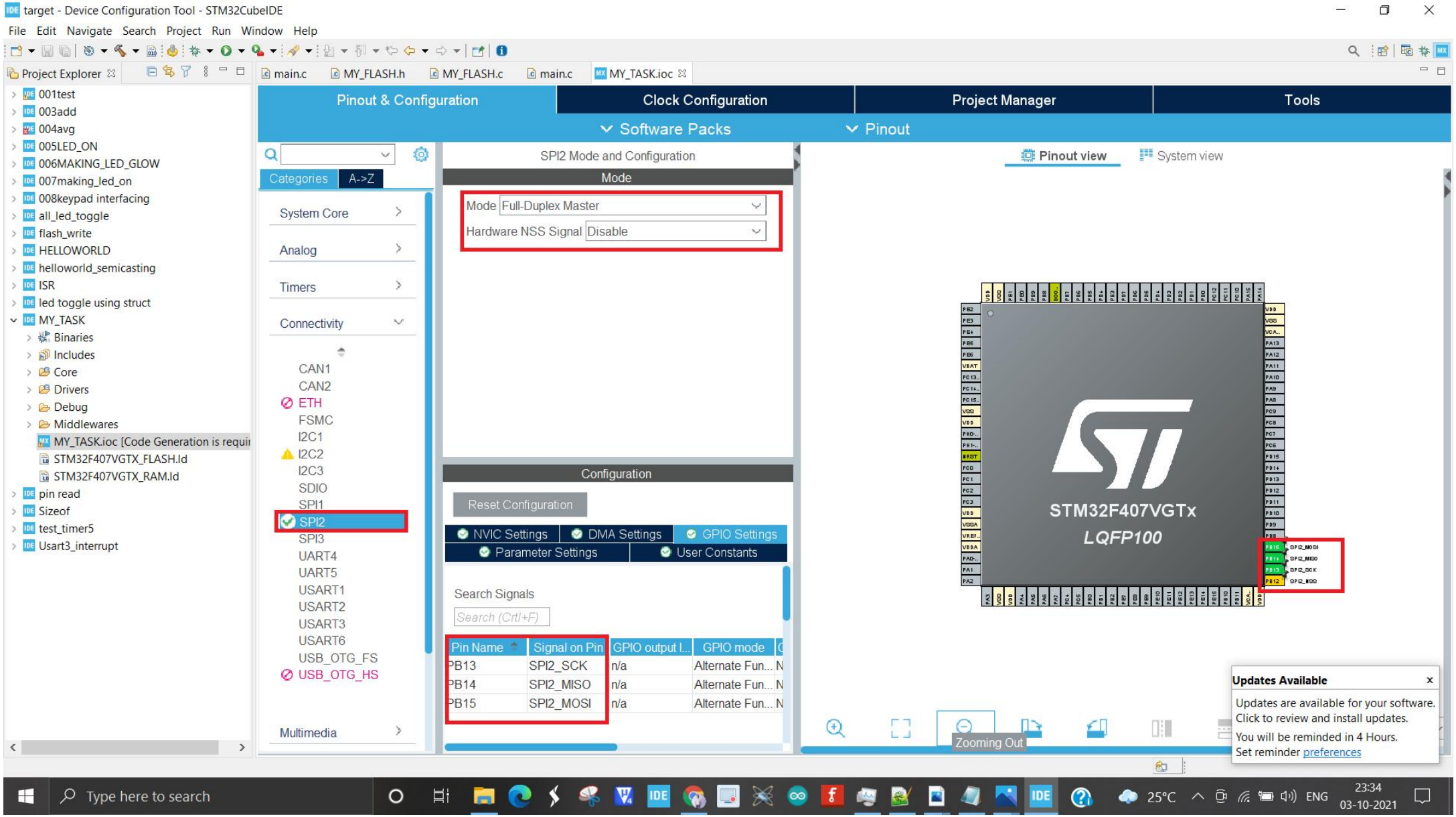
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Mode
Mode Full-Duplex Master
Hardware NSS Signal Disable
Configuration
Reset Configuration
NVIC Settings
DMA Settings
GPIO Settings
Parameter Settings
User Constants
Search Signals
Search (Crtl+F)
Pin Name
Signal on Pin
GPIO output l...
GPIO mode
PB13 SPI2_SCK n/a Alternate Fun...
PB14 SPI2_MISO n/a Alternate Fun...
PB15 SPI2_MOSI n/a Alternate Fun...
Pinout view
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STM32F407VGTx
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SPI2_MOSI
SPI2_MISO
SPI2_SCK
SPI2_NSS
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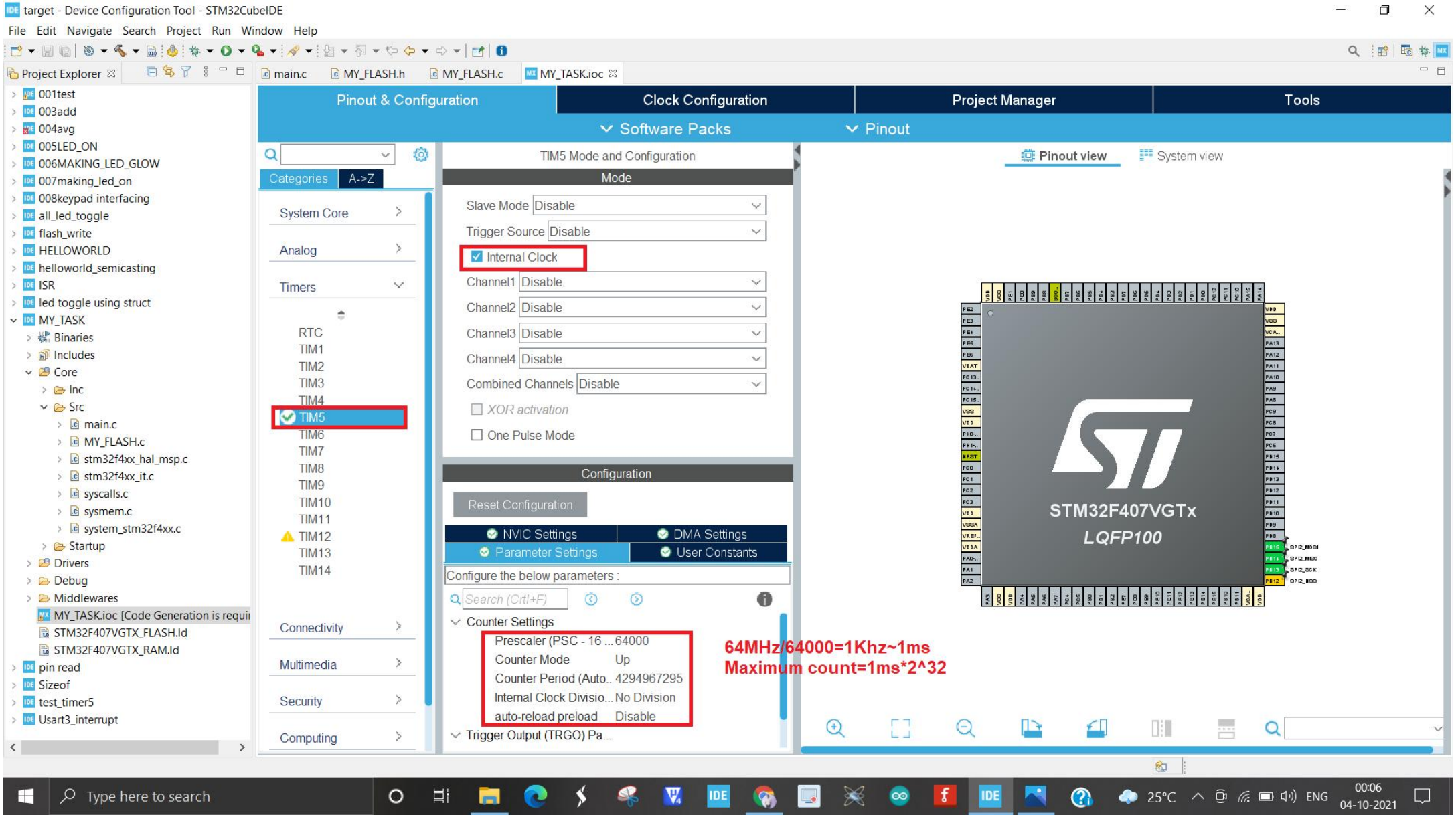
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TIM11
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TIM5 Mode and Configuration
Mode
Slave Mode Disable
Trigger Source Disable
Internal Clock
Channel1 Disable
Channel2 Disable
Channel3 Disable
Channel4 Disable
Combined Channels Disable
XOR activation
One Pulse Mode
Configuration
Reset Configuration
NVIC Settings
DMA Settings
Parameter Settings
User Constants
Configure the below parameters :
Search (Crtl+F)
Counter Settings
Prescaler (PSC - 16 ... 64000
Counter Mode Up
Counter Period (Auto.. 4294967295
Internal Clock Divisio... No Division
auto-reload preload Disable
Trigger Output (TRGO) Pa...
64MHz/64000=1Khz~1ms
Maximum count=1ms*2^32
Pinout view
System view
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Table 9. Alternate function mapping (continued)

Port		AF0 SYS	AF1 TIM1/2	AF2 TIM3/4/5	AF3 TIM8/9/10/11	AF4 I2C1/2/3	AF5 SPI1/SPI2/I2S2/I2S2ext	AF6 SPI3/I2Sext/I2S3	AF7 USART1/2/3/I2S3ext	AF8 UART4/5/USART6	AF9 CAN1/2 TIM12/13/14	AF10 OTG_FS/OTG_HS	AF11 ETH	AF12 FSMC/SDIO/OTG_FS	AF13 DCMI	AF14	AF15
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	-	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N		-	-	-	-	-	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1		-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD		-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	-	DCMI_D10	-	EVENTOUT
	PB6	-	-	TIM4_CH1		I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	DCMI_D5	-	EVENTOUT
	PB7	-	-	TIM4_CH2		I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCMI_D6	-	EVENTOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN ETH_RMII_TX_EN	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0 ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1 ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT

Alternate function mode=5

STM32f4Discovery:
I am using SPI2 here
to communicate with
NAND flash

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Table 5. Flash module organization (STM32F40x and STM32F41x)

Block	Name	Block base addresses	Size
Main memory	Sector 0	0x0800 0000 - 0x0800 3FFF	16 Kbytes
	Sector 1	0x0800 4000 - 0x0800 7FFF	16 Kbytes
	Sector 2	0x0800 8000 - 0x0800 BFFF	16 Kbytes
	Sector 3	0x0800 C000 - 0x0800 FFFF	16 Kbytes
	Sector 4	0x0801 0000 - 0x0801 FFFF	64 Kbytes
	Sector 5	0x0802 0000 - 0x0803 FFFF	128 Kbytes
	Sector 6	0x0804 0000 - 0x0805 FFFF	128 Kbytes
	. . .	. . .	. . .
	Sector 11	0x080E 0000 - 0x080F FFFF	128 Kbytes
System memory		0x1FFF 0000 - 0x1FFF 77FF	30 Kbytes
OTP area		0x1FFF 7800 - 0x1FFF 7A0F	528 bytes
Option bytes		0x1FFF C000 - 0x1FFF C00F	16 bytes

I am using this sector of flash memory of stm32f4discovery board to store the address of LAST NAND FLASH memory wher i have written the SENSOR DATA

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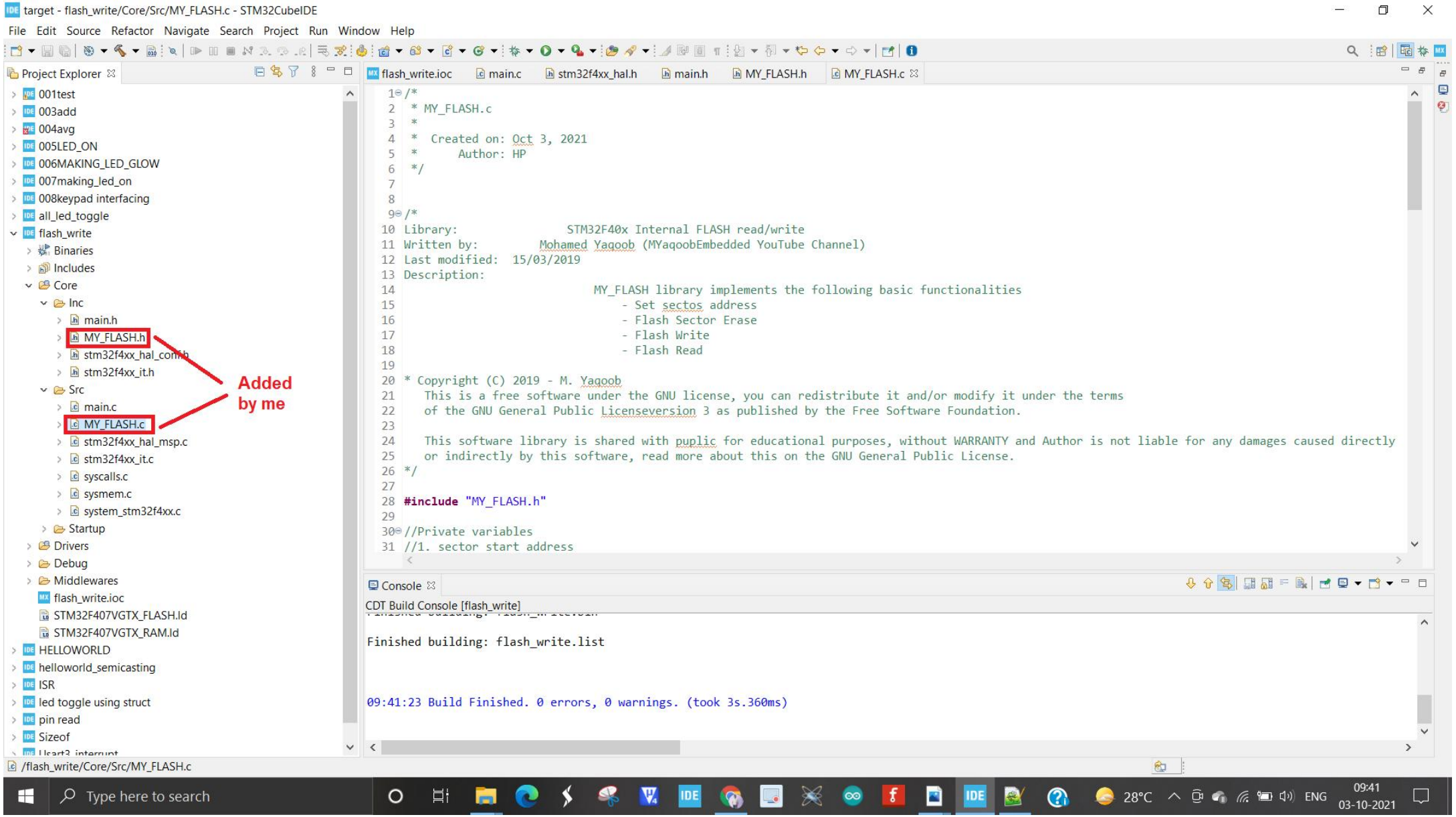
target - flash_write/Core/Src/MY_FLASH.c - STM32CubeIDE
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Project Explorer
001test
003add
004avg
005LED_ON
006MAKING_LED_GLOW
007making_led_on
008keypad interfacing
all_led_toggle
flash_write
Binaries
Includes
Core
Inc
main.h
MY_FLASH.h
stm32f4xx_hal_conf.h
stm32f4xx_it.h
Src
main.c
MY_FLASH.c
stm32f4xx_hal_msp.c
stm32f4xx_it.c
syscalls.c
sysmem.c
system_stm32f4xx.c
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STM32F407VGTX_FLASH.ld
STM32F407VGTX_RAM.ld
HELLOWORLD
helloworld_semicasting
ISR
led toggle using struct
pin read
Sizeof
Added by me
flash_write.ioc
main.c
stm32f4xx_hal.h
main.h
MY_FLASH.h
MY_FLASH.c
/*
* MY_FLASH.c
*
* Created on: Oct 3, 2021
* Author: HP
*/
/*
Library: STM32F40x Internal FLASH read/write
Written by: Mohamed Yaqoob (MYaqoobEmbedded YouTube Channel)
Last modified: 15/03/2019
Description:
MY_FLASH library implements the following basic functionalities
- Set sectos address
- Flash Sector Erase
- Flash Write
- Flash Read
* Copyright (C) 2019 - M. Yaqoob
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*/
#include "MY_FLASH.h"
//Private variables
//1. sector start address
Console
CDT Build Console [flash_write]
Finished building: flash_write.list
09:41:23 Build Finished. 0 errors, 0 warnings. (took 3s.360ms)
/flash_write/Core/Src/MY_FLASH.c
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target - MY_TASK/Core/Src/main.c - STM32CubeIDE

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Project Explorer

- 001test
- 003add
- 004avg
- 005LED_ON
- 006MAKING_LED_GLOW
- 007making_led_on
- 008keypad interfacing
- all_led_toggle
- flash_write
  - Binaries
  - Includes
  - Core
    - Inc
    - Src
      - main.c
      - MY_FLASH.c
      - stm32f4xx_hal_msp.c
      - stm32f4xx_it.c
      - syscalls.c
      - sysmem.c
      - system_stm32f4xx.c
    - Startup
  - Drivers
  - Debug
  - Middlewares
  - flash_write.ioc
  - STM32F407VGTX_FLASH.ld
  - STM32F407VGTX_RAM.ld
- HELLOWORLD
- helloworld_semicasting
- ISR
- led toggle using struct
- MY_TASK
  - Binaries
  - Includes
  - Core
    - Inc
    - Src

MY_TASK.ioc | *main.c | MY_FLASH.h | MY_FLASH.c

```
34 /* USER CODE BEGIN PD */
35 /* USER CODE END PD */
36
37 /* Private macro -------------------------------
38 /* USER CODE BEGIN PM */
39
40 /* USER CODE END PM */
41
42 /* Private variables ---------------------------
43 SPI_HandleTypeDef hspi2;
44
45 TIM_HandleTypeDef htim5;
46
47 /* USER CODE BEGIN PV */
48 //MT29F1G01AAADD instructions
49 const uint8_t WRITE_ENABLE=0x06;
50 /* USER CODE END PV */
51
52 /* Private function prototypes -----------------
53 void SystemClock_Config(void);
54 static void MX_GPIO_Init(void);
55 static void MX_SPI2_Init(void);
56 static void MX_TIM5_Init(void);
57 /* USER CODE BEGIN PFP */
58
59 /* USER CODE END PFP */
60
61 /* Private user code ---------------------------
62 /* USER CODE BEGIN 0 */
63 uint8_t Sensor_Data[300];          //I am assumin
64 int latest_Nand_flash_addr;  //I am assuming in
65 int timer_val;
66 /* USER CODE END 0 */
67
68 /**
69   * @brief  The application entry point.
70   * @retval int
71   */
72 int main(void)
73 {
74   /* USER CODE BEGIN 1 */
75
76   /* USER CODE END 1 */
```

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1Gb x1: SPI NAND Flash Memory
SPI NAND Command Definitions

SPI NAND Command Definitions

Table 3: SPI NAND Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
BLOCK ERASE	D8h	3	0	0	Block erase
GET FEATURE	0Fh	1	0	1	Get features
PAGE READ	13h	3	0	0	Array read
PROGRAM EXECUTE	10h	3	0	0	Enter block/page address, no data, execute
PROGRAM LOAD RANDOM DATA	02h	2	0	1 to 2112	Load program data—2kB MAX
PROGRAM LOAD	84h	2	0	1 to 2112	Enter cache address/data
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112	Output cache data at addr
READ FROM CACHE x2	3Bh	2	1	1 to 2112	Output cache data on SI and SO
READ FROM CACHE x4	6Bh	2	1	1 to 2112	Output cache data on SI, SO, WP#, HOLD#
READ ID	9Fh	0	1	2	Read device ID
RESET	FFh	0	0	0	Reset the device
SET FEATURE	1Fh	1	0	1	Set features
WRITE DISABLE	04h	0	0	0	
WRITE ENABLE	06h	0	0	0	

Enabling WRITE by 06h

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1Gb x1: SPI NAND Flash Memory

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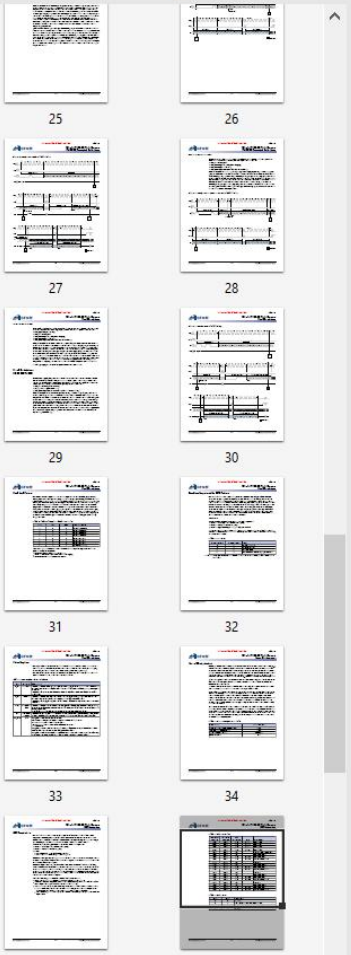

USER_DATA

BAD BLOCK

Table 11: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
801h	800h	No		Reserved (bad block data)
803h	802h	No		User meta data II
807h	804h	Yes	Spare 0	User meta data I
80Fh	808h	Yes	Spare 0	ECC for main/spare 0
811h	810h	No		Reserved
813h	812h	No		User meta data II
817h	814h	Yes	Spare 1	User meta data I
81Fh	818h	Yes	Spare 1	ECC for main/spare 1
821h	820h	No		Reserved
823h	822h	No		User meta data II
827h	824h	Yes	Spare 2	User meta data I
82Fh	828h	Yes	Spare 2	ECC for main/spare 2
831h	830h	No		Reserved
833h	832h	No		User meta data II
837h	834h	Yes	Spare 3	User meta data I
83Fh	838h	Yes	Spare 3	ECC for main/spare 3

Table 12: ECC Status

Bit 1	Bit 0	Description
0	0	No errors
0	1	1- to 4-bit error detected and corrected
1	0	Bit errors greater than four bits detected and not corrected

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ECC Protection

The serial device offers data corruption protection by offering 4-bit internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting the ECC bit in the OTP register. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the "active" state.

ECC_Enable Procedure

To enable/disable ECC, perform the following command sequence:
- Issue the SET FEATURES register write (1Fh).
- Issue the OTP feature address (B0h).
- Then:
  - To enable ECC Set Bit 4, ECC Enable, to 1.
  - To disable ECC Clear Bit 4, ECC Enable, to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a 1- to 4-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:
- Spare area definitions provided in the ECC Protection table below.
- WRITEs to ECC are supported for main and spare areas 0, and 1. WRITEs to the ECC area are prohibited (see the ECC Protection table below).
- When using partial-page programming, the following conditions must both be met:
  - In the main user area and in user meta data area I, single partial-page programming operations must be used (see the ECC Protection table below).
  - Within a page, the user can perform a maximum of four partial-page programming operations.

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