

# Analog Electronics Notes

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# MOS DEVICE PHYSICS.

→ The level of abstraction of knowledge required to study analog is

Quantum Physics → Solid state physics → Semiconductor physics  
→ device Modelling → design of circuits.

## MosFet as switch.

\* To use mosfet as a switch. the drain to source Resistance should be very low. when gate voltage of mosfet (nmos) is very high, in ideal case it should be zero. & the resistance should be very high for low gate Voltage. in ideal case it should be infinity.

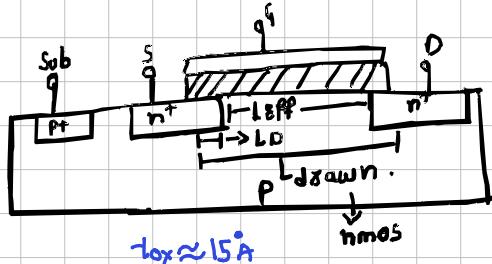
## MosFet structure.

\* The effective length of mosfet is given by  $L_{drain} - 2L_D = L_{eff}$

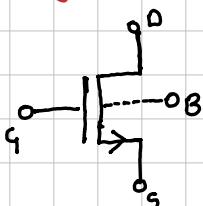
\* mosfet is a symmetrical device i.e the drain & source of the device can be interchanged.

\* The Substrate of the mosfet must be reverse bias with respect to source. or else the current will directly flow from S/D to the substrate. if it is forward bias. this is called latch up.

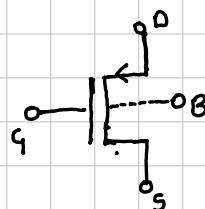
\* PMos is negation of nmos. & it is fabricated in an N-well & substrate. is connected to highest potential.



## Mosfet Symbol



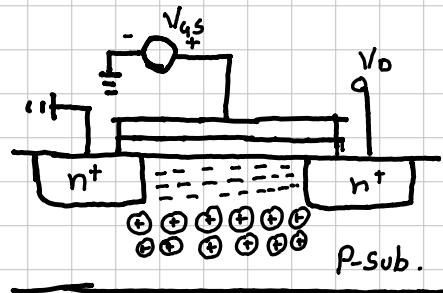
Nmos.



Pmos.

## Mosfet V-I Characteristics.

\* When we apply voltage to the gate, the holes move away from gate and electron move towards the gate. This will create a channel. If we increase  $V_g$  then the depletion region will increase. This region can be modelled as two cap. i.e. gate oxide cap & depletion cap connected in series. If we increase  $V_g$  the current will start to flow. Then we can say device is inverted. The  $V_g$  required for this inverted channel is called  $V_{th}$ . If  $V_g$  is increased further the charge in depletion region will be same but charge density i.e. current will increase.



$$V_{th} = \phi_{ms} + 2\phi_f + \frac{\phi_{dep}}{C_{ox}}$$

$\phi_{ms}$  :- PolySilicon & silicon workfunction.

$$\phi_f = V_T \ln \left( \frac{N_{sub}}{N_i} \right) \quad N_{sub} \rightarrow \text{charge density. } N_i \rightarrow \text{intrinsic carrier}$$

$$\phi_{dep} = \sqrt{4q\epsilon_s / \phi_f N_{sub}} \quad V_T = \text{thermal voltage.}$$

$$C_{ox} = \frac{\epsilon_s}{t_{ox}} \approx 17.25 \text{ fF/}\mu\text{m}^2$$

\* For Pmos theory is same but the polarity is reversed.

## Derivation of I-V characteristics.

- \* Current is the amount of charge flowed per unit time i.e it is equal to

$$I_D = Q_d \cdot V \quad \textcircled{1}$$

$Q_d \rightarrow$  charge density

$V \rightarrow$  velocity of charge.



- \* for  $V_{GS} > V_{TH}$  the charge density is proportional to  $V_{GS} - V_{TH}$ . for  $V_{DS} \neq V_{GS} = 0$ .

$$Q_d = W C_{ox} (V_{GS} - V_{TH}) \quad \textcircled{2}$$

- \* when we increase  $V_{DS} > 0$  the channel potential varies from  $V_S(x) = 0$  to  $V_D(x) = V_{DD}$ .  $\therefore$  the charge density can be written as.

$$Q_d = W C_{ox} (V_{GS} - V_{TH} - V(x)) \quad \textcircled{3} \quad V(x) \text{ varies from } 0 \text{ to } V_D$$

- \* Substitute equation 3 into 1.

$$I_D = -W C_{ox} (V_{GS} - V_{TH} - V(x)) \cdot V \quad \textcircled{4} \quad V \rightarrow \text{velocity of electron.}$$

- \* Negative sign is due to negative charge we know that.

$$V = U_n \vec{E} \Rightarrow V = U_n - \frac{dV}{dx} \quad \textcircled{5} \quad V \Rightarrow \text{potential.}$$

- Substituting equation 5 in 4.

$$I_D = W C_{ox} (V_{GS} - V_{TH} - V(x)) \times U_n \times \frac{dV}{dx}$$

Integrating on both side.

$$\int_0^L I_D dx = \int W C_{ox} (V_{GS} - V_{TH} - V(x)) \times U_n x dV$$

$\therefore$  the current in channel is given by

$$I_D = \frac{W C_{ox} U_n}{L} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

\* for  $V_{GS} - V_{TH} \geq V_{DS}$   $\therefore$  the device act as voltage controlled resistor.

$$I_D \approx \frac{W C_{ox} U_n}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$\therefore R_{on} = \frac{1}{\frac{W C_{ox} U_n}{L} (V_{GS} - V_{TH})}$$

\* for  $V_{GS} - V_{TH} < V_{DS}$  the current in the mosfet become constant due to the pinch off. the effective length of transistor decrease. there is current even after the pinch off because there is large electric field in the channel. which will shoot electron to the drain of mosfet.

$$I_D = \frac{W C_{ox} U_n}{2x L'} (V_{GS} - V_{TH})^2$$

\* In saturation mosfet act as the current source when  $L$  is constant NMOS current source inject current in to ground. whereas PMOS current source draw current from the VDD.

## MOS Transconductance.

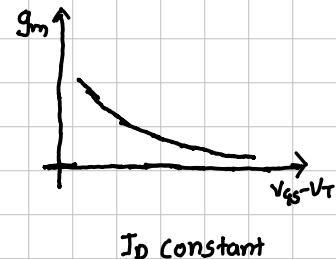
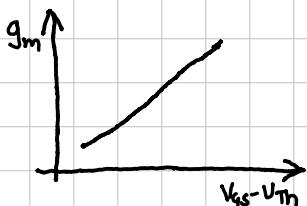
→ The change in drain current with change in gate-source voltage is called transconductance. It is denoted by  $g_m$ .

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS} \text{ const}} \Rightarrow U_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})$$

$$g_m = U_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})$$

$$g_m = \sqrt{2 \times U_n C_{ox} \frac{W}{L} I_D}$$

$$g_m = \frac{2 I_D}{V_{GS} - V_{Th}}$$



\*  $g_m$  increases with overdrive voltage when  $W/L$  kept constant whereas.  
 $g_m$  decreases with overdrive voltage when  $I_D$  is kept constant.

\* the pinch off occurs when Voltage of drain is at  $V_{GS} - V_{TH}$  if voltage of drain is increased further the effective length of mosfet is decreased and current is given by

$$I_D = \frac{U_s W}{L'} C_{ox} \left( V_{GS} - V_{TH} \right)^2 \quad L' \rightarrow \text{Effective length after pinch off}$$

\* mobility of electron is twice the mobility of holes

> Transconductance of mosfet

$$* g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{\text{constant } V_{DS}} \Rightarrow U_s \frac{W}{L} C_{ox} \left( V_{GS} - V_{TH} \right) \Rightarrow \sqrt{\frac{U_s W}{L} C_{ox} I_D}$$

### Body effect.

→ when Negative Voltage is applied to the body , more positive charge hole move towards the body which will increase the channel width . in order to balance this charge we need to add more positive charge to the gate . this will increase the  $V_{TH}$  of the transistor .

$$V_{TH} = V_{TH0} + \delta \left[ \sqrt{2\phi_f + \phi_{SB}} - \sqrt{2\phi_f} \right] \quad \delta = \sqrt{\frac{2qE_s N_{sub}}{C_{ox}}}$$

→  $\delta$  range is from 0.3 to 0.4

### channel length modulation.

→ The length of the channel will decrease when the voltage of the Drain increase . in other words the current id is function of  $V_{DS}$  . the effective change in length is given by .

$$L' = L - \Delta L \quad \therefore \frac{L'}{L} = 1 - \frac{\Delta L}{L}$$

$$I_D = \frac{K_W}{L} \frac{(V_{GS} - V_T)^2}{L} \Rightarrow \frac{K_W}{L} \frac{(V_{GS} - V_T)^2}{1 - \frac{\Delta L}{L}} \quad K \Rightarrow \frac{C_ox V_{th}}{2}$$

$$I_D \approx \frac{K_W}{L} (V_{GS} - V_T)^2 \left[ 1 + \frac{\Delta L}{L} \right] \quad \frac{\Delta L}{L} \propto V_{DS} \Rightarrow \frac{\Delta L}{L} = \lambda V_{DS}$$

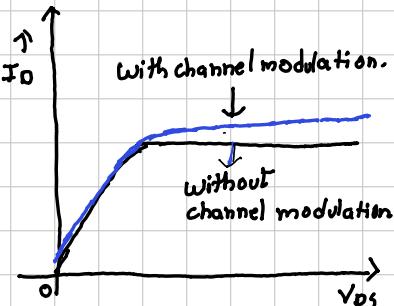
$$I_D \approx \frac{K_W}{L} (V_{GS} - V_T)^2 \left[ 1 + \lambda V_{DS} \right]$$

→  $\lambda$  is called channel modulation coefficient

→ the gm of the transistor is .

$$g_m = \frac{K_W}{L} (V_{GS} - V_T) (1 + \lambda V_{DS})$$

→ This formula is less accurate for small channel mosfet. In short channel mosfet  $I_D$  is also dependent on  $V_{DS}$ .



### Subthreshold conductance.

→ we have assumed that the current in mosfet is zero for  $V_{GS} < V_T$  but this assumption is not right. there is current in the channel. this current is due to the weak inversion. & the current will rise exponentially with respect to  $V_{GS}$ . when subthreshold current reaches 100nA the gate voltage is taken as  $V_t$  of transistor.

$$I_D = I_0 e^{\frac{V_{GS} - V_T}{nV_T}} \quad I_0 \propto \frac{W}{L} \quad n \rightarrow \text{ideality factor} \quad V_T \rightarrow \text{thermal voltage.}$$

→ for voltage below  $V_T$  the current will drop 10 time per 80mV of voltage drop.

## Mos device model :-

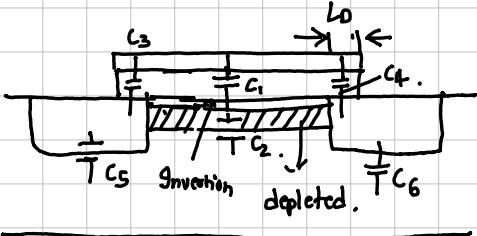
→ Parasitic caps of mosfet

↳ gate to channel  $\rightarrow C_1$  (oxide).

↳ channel to substrate  $\rightarrow C_2$  (depletion)

↳ gate to Source & Drain  $\rightarrow C_3 \& C_4$   $\rightarrow$  (overlap).

↳ Substrate to source & drain  $\rightarrow C_5 \& C_6$   $\rightarrow$  (junction)



$$C_1 = WL C_{ox}$$

$$C_{ox} = \epsilon / t_{ox}$$

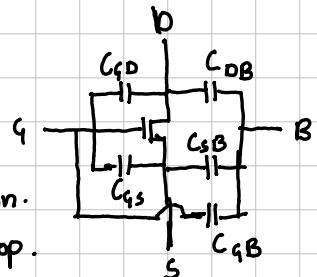
$$C_2 = WL \sqrt{q E_s; N_{sub}} / (4 \phi_F)$$

$N_{sub} \rightarrow$  donor concentration.

$\phi_F \rightarrow$  voltage drop.

$$C_3 \& C_4 \Rightarrow C_{ox} L_D X W$$

$$\Rightarrow C_{ov} W \rightarrow C_{ov} \rightarrow \text{overlap cap per unit width.}$$



$C_5 \& C_6$

↳  $C_j \times \text{Area} \rightarrow$  due to bottom plate.

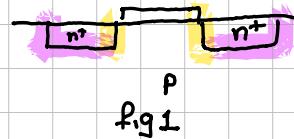
↳  $C_{jsw} \times \text{Perimeter} \rightarrow$  due to Side wall (perimeter)

$$C_j = C_{j0} / \left[ 1 + \frac{V_R}{\phi_B} \right]^m. \quad \begin{aligned} \rightarrow V_R &\rightarrow \text{reverse bias voltage.} \\ \rightarrow \phi_B &\rightarrow \text{built in potential.} \\ m &\rightarrow 0.3 \text{ to } 0.4 \end{aligned}$$

Similary for  $C_{jsw}$

→  $C_{jsw}$  for region marked in yellow from figure

1 may be different compared to region marked in pink. but we assume it is equal to other regions



Case I  $\Rightarrow$  when device is off  $V_{GS} < V_{TH}$ .

1)  $C_{GD} = C_{GS} = C_{oVW}$

2) gate to bulk  $\Rightarrow C_1 \parallel C_2$

3)  $C_{DB}, C_{SB} \Rightarrow$  depends on bias voltage with substrate.

Case II :- when device is in triode,  $V_{GS} < V_{TH}$   $V_S = V_D$

1) the gate to channel capacitance is divide between source & drain.

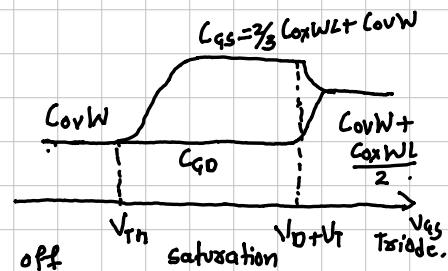
1)  $C_{GD} = C_{GS} = C_{oVW} + \frac{C_{oXWL}}{2}$

Case III :- when device is in saturation.

$V_{GS} < V_{TH}$   $V_{GS} - V_T < V_{DS}$ .

$C_{GS} = \frac{2}{3} C_{oXWL} + C_{oVW}$

$C_{GD} = C_{oVW}$



\* the capacitance doesn't provide smooth transition from one region to other. this will create difficult to converge in simulation.

\*  $C_{GB}$  is neglected in saturation & triode region. because of formation of channel which act as a shield between gate & bulk.

## Mos small signal model

- Small signal analysis is applied when perturbation is small & & non-linear effect are not concerned.
- drain current is the function of drain voltage which is modelled by

$$\delta_0 = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\gamma_2 U_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 \lambda} = \frac{1}{I_0 \lambda}$$

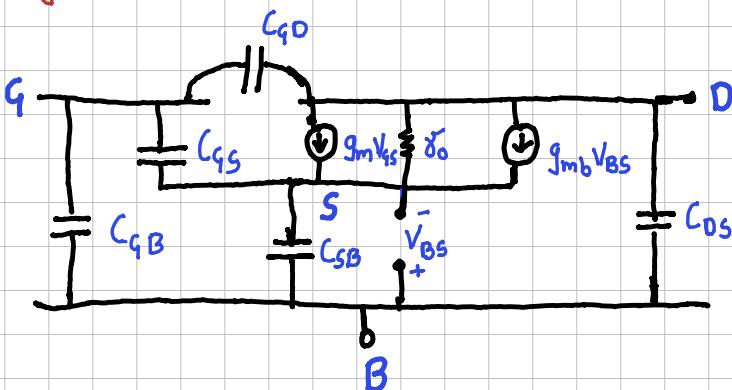
- the bulk potential effect the threshold voltage of mosfet. It effect the current  $I_0$ . it behave as the second gate.

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = U_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \frac{\partial V_{Th}}{\partial V_{BS}}$$

$$\frac{\partial V_{Th}}{\partial V_{BS}} = -\frac{\partial V_{Th}}{\partial V_{SB}} = -\frac{\gamma}{2} (2\phi_F + V_{SB})^{\frac{\gamma}{2}}$$

$$g_{mb} = g_m \eta \quad \text{where } \eta = -\frac{\gamma}{2} (2\phi_F + V_{SB})^{-\frac{1}{2}}$$

## Small signal model.



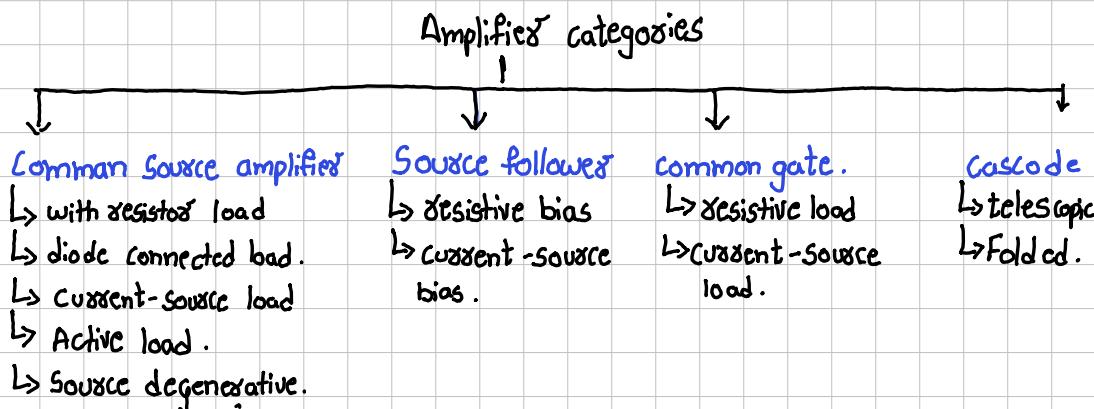
- For pmos the small signal is similar to that of nmos.

## level one Spice parameters:-

- \* VTO :- threshold Voltage with zero  $V_{SB}$   $\rightarrow V$
- \* GAMMA :- body - Effect co-efficient  $\rightarrow V^{1/2}$ .
- \* PHI :-  $2\phi_F \rightarrow V$
- \* TOX :- gate oxide thickness  $\rightarrow m$ .
- \* NSUB :- Substrate doping  $\rightarrow cm^{-3}$
- \* LD :- source/drain side diffusion  $\rightarrow m$ .
- \* UO :- channel mobility  $\rightarrow cm^2 s/V$ .
- \* LAMBDA :- channel-length modulation coefficient  $\rightarrow V^{-1}$
- \* CJ :- source/drain bottom-plate junction capacitance per unit area.  $F/m^2$
- \* CJSW :- sidewall junction capacitance per unit length  $\rightarrow F/m$ .
- \* PB :- source/drain junction built-in potential.  $\rightarrow V$
- \* MJ :- exponent in CJ Equation  $\rightarrow$  unitless
- \* MJSW :- exponent in CJSW Equation  $\rightarrow$  unitless.
- \* CGDO :- gate-drain overlap capacitance per unit width  $\rightarrow F/m$ .
- \* CGSO :- gate-source overlap capacitance per unit width  $\rightarrow F/m$ .
- \* JS :- source/drain leakage current per unit area  $\rightarrow A/m^3$

# SINGLE STAGE AMPLIFIERS.

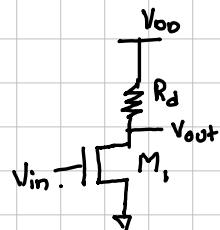
- \* The ideal input and output relation of amplifier  $y(t) = a_0 + a_1 x(t)$ .
- \* the real input & output relation of amplifier due to distortion is given by  $y(t) = a_0 + a_1 x(t) + \underbrace{a_2 x^2(t) + a_3 x^3(t)}_{\text{higher order harmonics.}} \dots \dots$
- \* Parameters that used to evaluate the performance of amplifier are
  - 1) Speed
  - 2) gain
  - 3) maximum swing
  - 4) power consumption
  - 5) supply voltage
  - 6) linearity
  - 7) input output impedance.



## Common Source Stage. [CS].

\* CS with Resistance.

$$\therefore V_{out} = V_{DD} - R_D \times \left[ \frac{1}{2} C_{ox} \frac{W}{L} U_n (V_{GS} - V_{Th})^2 \right]$$



Triode region  $V_{out} < V_{in} - V_{Th}$ .

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D U_n C_{ox} \frac{W}{L} (V_{in} - V_{Th}) = -g_m R_D . =$$

\* Since  $g_m$  is function of  $V_{in}$  the swing of signal should be small to prevent non linear behaviour.

$$A_v = - \sqrt{2 U_n C_{ox} \frac{W}{L} I_D \frac{V_{RD}}{I_D}} \Rightarrow - \sqrt{2 U_n C_{ox} \frac{W}{L} \frac{V_{RD}}{J I_D}}$$

\*  $A_v$  can be increased by increasing  $W/L$  which in lead to increase in cap & high  $V_D$  which will reduce the swing

\* if  $V_{RD}$  is kept constant and  $I_D$  is reduced which will increase  $R_D$  & the time constant

\* for large  $R_D$  the channel length modulation become significant.

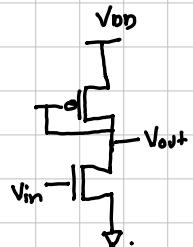
$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D C_{ox} \frac{W}{L} U_n (V_{in} - V_{Th}) (1 + \lambda V_{os}) - \frac{R_D C_{ox} W}{2} (V_{in} - V_{Th})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

$$A_v = -g_m R_D - \frac{R_D}{\delta o} A_v = A_v = -g_m (R_D \delta o)$$

\* Maximum gain is achieved when  $R_D = \infty$  ie  $= -g_m \delta o$  which is almost equal to 10.

## CS Stage with diode connected load.

It is difficult to fabricate resistors on chip so we use diode connected resistors to get resistors. the resistance of diode connected resistor is equal to.



$$\delta = \frac{1}{g_{mp} + g_{mbp}} \parallel \delta_{op} \approx \frac{1}{g_{mp} + g_{mbp}}$$

$$\therefore \text{gain } Av = -g_{mn} \delta \parallel \delta_{on} = -g_{mn} \left( \frac{1}{g_{mp} + g_{mbp}} \parallel \delta_{on} \right) \approx \frac{-g_{mn}}{g_{mp} + g_{mbp}}$$

$$\therefore Av = \frac{-g_{mn}}{g_{mp}(1+\eta)} = \frac{\sqrt{W/L \times u_n}}{\sqrt{W/L \times u_p}} \times \frac{1}{(1+\eta)} \quad \eta = \frac{g_{mbp}}{g_{mp}}$$

\* the gain is independent of bias current or voltage it is more linear compared to previous amplifiers.

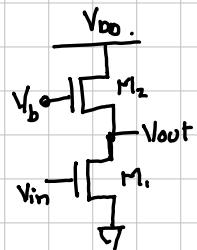
\* gain is weak function of  $W/L$  if  $u_n = 2u_p$  then  $(W/L)_n = 12.5(W/L)_p$  to get gain of 5.

\* In today technology channel length modulation can't be ignored  $\therefore$   
gain is given by

$$Av = -g_{mn} \left( \frac{1}{g_{mp} + g_{mbp}} \parallel \delta_{on} \parallel \delta_{op} \right)$$

## CS Stage with Current Source.

- \* to achieve higher gain we need to have larger  $R_o$  in order to achieve that we use current source.



$$Av = -g_m (\delta_{o_1} || \delta_{o_2})$$

→ to achieve larger swing  $V_{dsat}$  of  $M_2$  should be less. this can be achieved by increasing width, but this will lead to reduction of  $\delta_{o_2}$ . then we have to change  $\lambda$  by increasing length to increase  $\delta_{o_2}$ . but increasing in width will also increase the capacitance at output node.

$$g_m, \delta_{o_1} = \sqrt{2 \left( \frac{W}{L} \right) UnLox I_D \frac{1}{I_D \lambda}}$$

- \* gain increase with increasing  $L$  as  $\lambda$  is function of  $L$ .
- \* gain increase with decrease in  $I_D$ .
- \* increase in length of  $M_2$  will increase  $\delta_{o_2}$  but it will also increase the  $V_{dsat}$  of  $M_2$ .

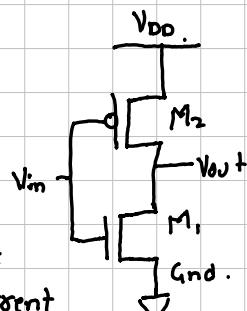
## CS Stage with active load

- \* the gain of the following circuit is

$$Av = -(g_m + g_{m_2})(\delta_{o_1} || \delta_{o_2})$$

- \* the following circuit has same impedance as current source circuit but it has higher gain compared to current source.

- \* Since  $V_{GS1} + |V_{GS2}| = V_{DD}$ . the variation in  $V_{DD}$  or  $V_{TH}$  will translate.

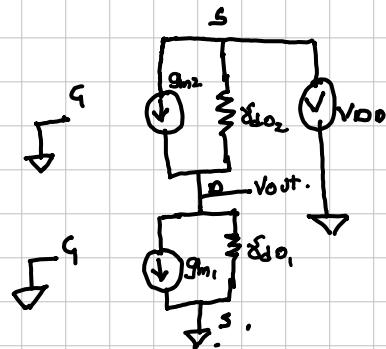


to current at output. the bias point of the circuit depends upon the PVT. this is the draw back of the circuit.

\* the output gain given by variation in supply

$$V_{out} = \left( g_m Z_{O_2} V_{DD} + V_{DD} \right) \frac{\delta d_{O_2}}{\delta d_{O_2} + \delta d_{O_1}}$$

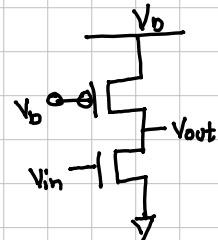
$$\therefore \frac{V_{out}}{V_{DD}} = \frac{(g_m Z_{O_2} + 1) \delta d_{O_1}}{\delta d_{O_2} + \delta d_{O_1}}$$



- CS with triode load.

\* here mosfet is operating in deep triode.

$$R_{on} = \frac{1}{W_2 C_{ox_2} U_{T_2} (V_{DD} - V_b - V_T)}$$



\* the draw back of the following circuit is the Ron depend on.  $V_b$ ,  $V_T$ ,  $W, L$ ,  $V_{DD}$  which change with PVT. and it is difficult to produce constant bias voltage  $V_b$ .

CS with source degenerated.

\* this configuration will make output more linear compared to other configuration. it make gain less dependent on  $g_m$

\* the output of this circuit is linearized but the gain is reduced due to the feed back.

$$G_M = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial I_D}{\partial V_{GS}} \times \frac{\partial V_{GS}}{\partial V_{in}} \quad (1)$$

We know that

$$V_{GS} = V_{in} - I_D R_S$$

$$\therefore \frac{\partial V_{GS}}{\partial V_{in}} = \left(1 - \frac{\partial I_D}{\partial V_{in}}\right) R_S \Rightarrow \left(1 - G_M\right) R_S \quad (2)$$

Substitute 2 in 1.

$$G_M = g_m \left(1 - G_M\right) R_S \Rightarrow G_M = \frac{g_m}{1 + g_m R_S}$$

$$\therefore \text{Small signal gain} = -G_M R_D = -\frac{g_m R_D}{1 + g_m R_S} \approx -\frac{R_D}{R_S} \text{ if } g_m R_S \gg 1.$$

\* Gain of Source degenerative circuit with body effect and channel length modulation is given below.

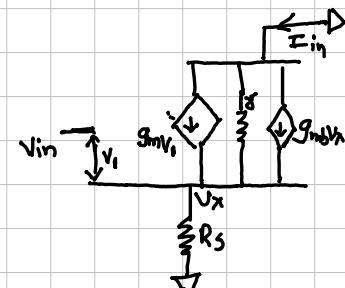
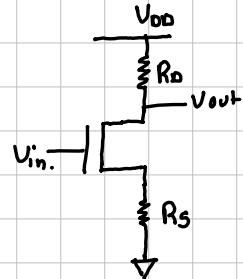
$$\therefore I_{out} = g_m V_i - g_{mb} V_x - \frac{I_{out} R_S}{\delta_o}$$

$$I_{out} = g_m \left( V_{in} - I_{out} R_S \right) + g_{mb} \left( -I_{out} R_S \right) - \frac{I_{out} R_S}{\delta_o}$$

$$G_M = \frac{g_m \delta_o}{R_S + \left[ 1 + (g_m + g_{mb}) R_S \right] \delta_o}$$

$$A_v = \frac{-g_m \delta_o || R_{eq}}{R_S + \left[ 1 + (g_m + g_{mb}) R_S \right] \delta_o}$$

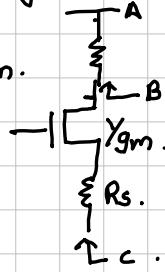
$$R_{eq} = R_D || \left[ R_S + \delta_o + (g_m + g_{mb}) \delta_o R_S \right]$$



finding gain by inspection for source degeneration

gain is equal to impedance looking into drain.

divide by the impedance looking into the source.



$$A_V = \frac{-R_o}{Y_{gm} + R_o} \Rightarrow \frac{R_{AB}}{R_{BC}} = \frac{-R_o}{Y_{gm} + R_s}$$

\* after source degeneration output resistance is increase therefore output resistance is

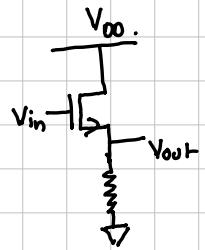
$$R_{out} = \left[ 1 + (g_m + g_{mb}) R_s \right] R_o + R_s \parallel R_o$$

\* any circuit can be represented by Norton equivalent circuit.  
by short circuit current parallel with open circuit resistance.  
and gain is given by  $-g_m R_{eq}$ .



## Source follower $\rightarrow$ Common drain.

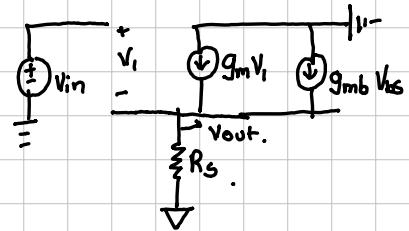
\* To achieve large gain for common source we need to have large output resistance. When this is connected to next stage with low impedance, the effective impedance decrease. So the voltage gain. We can use Source follower as a buffer between two stages. The gain of source follower is almost equal to 1.



$$V_{bs} = -V_{out}$$

$$V_{out} = R_s [g_m V_i - g_{mb} V_{out}]$$

$$V_{out} = R_s [g_m [V_{in} - R_s V_{out}] - g_{mb} V_{out}]$$



$$\frac{V_{out}}{V_{in}} = \frac{g_m R_s}{1 + [g_m + g_{mb}] R_s} \quad \text{if } (g_m + g_{mb}) R_s \gg 1 \approx \frac{g_m}{g_m + g_{mb}} \approx \frac{1}{1 + \eta} =$$

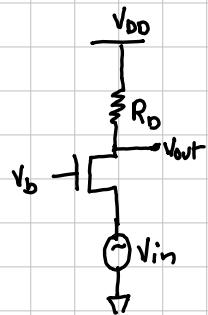
- \* Even  $R_s = \infty$  the output gain will not be equal to 1.
- \* If  $V_{in}$  increase by  $\sqrt{2}$   $V_{out}$  will increase by 2. This will create non-linearity in gain. To resolve this issue output resistance is replaced by a constant current source.
- \* It has high input impedance & moderate output impedance.
- \* It has low output headroom for swing.

Common gate.

$$* V_{out} = V_{DD} - \frac{1}{2} u_o C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th})^2 R_D.$$

∴

$$\frac{\partial V_{out}}{\partial V_{in}} = -\frac{1}{2} u_o C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th}) \left( -1 - \frac{\partial V_{in}}{\partial V_{in}} \right) R_D.$$

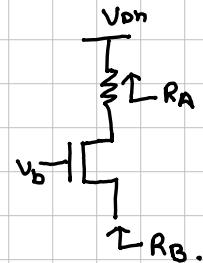


$$\frac{\partial V_{in}}{\partial V_{in}} = \frac{\partial V_{in}}{\partial V_{SB}} \frac{\partial V_{SB}}{\partial V_{in}} = n \times \frac{\partial V_{in}}{\partial V_{in}} = n$$

$$A_V = +\frac{1}{2} u_o C_{ox} \frac{W}{L} (V_b - V_{in} - V_{Th}) (1 + n) R_D.$$

$$A_V = g_m (1 + n) R_D.$$

$$\text{gain by inspection.} = \frac{\text{Impedance at drain } (R_A)}{\text{Impedance at source } (R_S)} = \frac{R_D}{(g_m + g_{mb})} = (g_m + g_{mb}) R_D$$



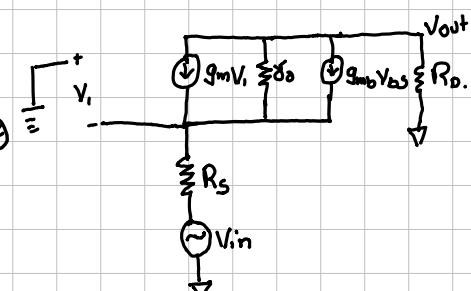
\* gain considering  $\delta_o$  &  $R_S$ .

$$V_i = \frac{R_S V_{out}}{R_D} - V_{in}. \quad ①$$

$$\delta_o \left[ \frac{-V_{out}}{R_D} - g_m V_i - g_{mb} V_i \right] - \frac{V_{out} R_S}{R_D} + V_{in} = V_{out} \quad ②$$

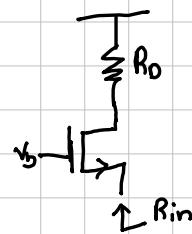
from 1 & 2.

$$A_V = \frac{(g_m + g_{mb}) \delta_o + 1}{\delta_o + (g_m + g_{mb}) \delta_o R_S + R_S + R_D} R_D$$



\* Input impedance at the Source is

$$R_{in} = \frac{R_o + g_o}{1 + (g_m + g_{mb}) g_o}$$



### Cascade stage.

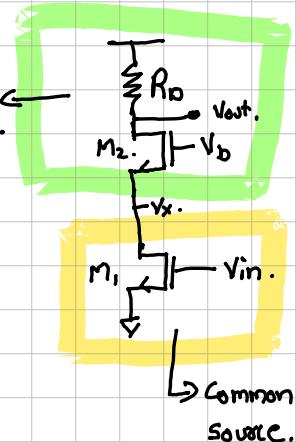
\* the input from common Source is converted into current & this current is feed to common gate this type of configuration is called cascade stage

\*  $M_1$  provide the gain to small signal  $V_{in}$  &  $M_2$  route the current to the  $R_o$ . device  $M_1$  is called input device & device  $M_2$  is called cascode. the device configuration is called telescopic cascode.

\* let us consider if we apply  $\Delta V$  voltage to  $V_{in}$ . and  $\delta = \lambda = 0$ .  $\delta_{o_2} = \infty$  then output current is  $g_m \Delta V$ . the voltage at  $V_x$  is  $(\gamma g_{m_2}) g_m \Delta V$  & the Voltage at the output is  $R_o g_m \Delta V$ .

\* let us consider if we keep  $V_{in}$  constant & vary  $V_b$ . the Mosfet  $M_1$  act as a current source. the node  $X$  act as source follower which has gain equal to 1. the node output doesn't change with the input due to constant current is flowing in the circuit.

\* To get both the device into saturation we need to have  $V_{out} \geq V_{dsat1} + V_{dsat2}$



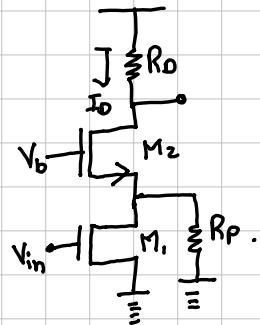
$$A_v = -I_D R_D$$

$$I_D = \frac{R_P}{R_P + g_m + g_{mb}} g_m V_{in}.$$

Assume  $\delta o_2 = \infty$

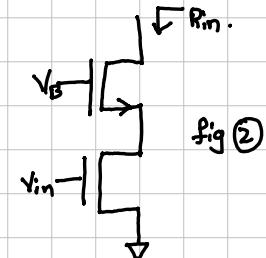
$\cancel{g_m + g_{mb}}$

current divider between  
resistance at  $M_2$  &  $R_P$ .



$$A_v = \frac{-R_P}{R_P + g_m + g_{mb}} g_m V_{in}.$$

$$\begin{aligned} R_{in} \text{ of figure 2} &= \delta o_2 + \delta o_1 + (g_{m2} + g_{mb}) \delta o_2 \delta o_1, \\ &\approx (g_{m2} + g_{mb}) \delta o_2 \delta o_1, \end{aligned}$$



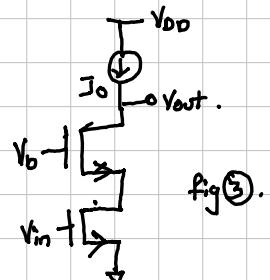
gain for figure 3 is

$$A_v = G_m R_{out}$$

$$R_{out} = \delta o_1 + \delta o_2 + (g_{m2} + g_{mb2}) \delta o_2 \delta o_1.$$

$$I_{out} = \frac{\delta o_1 g_m V_{in}}{\delta o_2 + \left(\frac{1}{g_{m1} + g_{mb2}}\right) || \delta o_2}.$$

$$A_v = G_m R_{out} \Rightarrow g_{m1} \delta o_1 \left[ (g_{m2} + g_{mb2}) \delta o_2 + 1 \right].$$

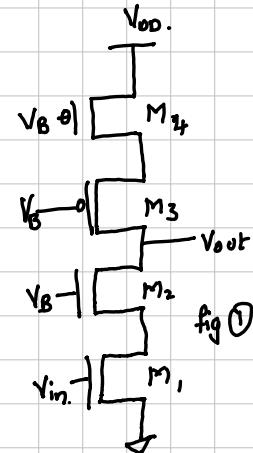


The output impedance of figure 1 is .

$$[\delta_{o_4} + \delta_{o_3} + (g_{m_3} + g_{m_3})\delta_{o_3}\delta_{o_4}] // [\delta_{o_2} + \delta_{o_1} + (g_{m_2} + g_{m_2})\delta_{o_2}\delta_{o_1}]$$

$$\text{gain } A_V \approx g_{m_1} \left[ (g_{m_3} + g_{m_3}) \cdot \delta_{o_3}\delta_{o_4} // (g_{m_2} + g_{m_2}) \delta_{o_2}\delta_{o_1} \right].$$

- \* Since cascode has high impedance it can be used as shield for voltage variations. in the circuit.



### Folded Cascode.

- \* cascode circuit can also be made by using PMOS - NMOS or NMOS - PMOS configuration .

$$\text{* the current } I_x = I_1 + I_2$$

- \* In fig 2  $V_{in}$  become more positive.  $I_1$  decrease forcing  $I_2$  to increase. hence  $V_{out}$  to drop.

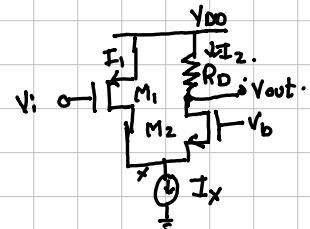


fig ②

- \* if  $V_{in}$  (figure 2) decrease from  $V_{DD}$  to zero M<sub>2</sub> carries all current &  $V_{in} < V_{DD} - U_{Th}$ . then  $I_2 = I_x - I_1$ ,  $V_{out} = V_{DD} - I_2 R_D$ .

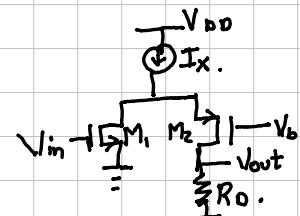


fig ③.

- \* if  $V_{in}$  is decreased further.  $I_1 = I_x$  &  $I_2 = 0$ .

- \* if  $V_{in}$  falls below this level i.e.  $I_1 > I_x$  then M<sub>1</sub> Enters into triode region.

# DIFFERENTIAL AMPLIFIERS

- \* Single Ended :- output is taken between ground & the signal.
- \* differential Signal:- the signal is measured between two nodes. & the two nodes should have equal impedance to the potential. if Single End peak to peak is  $V_o$ . the differential peak to peak is  $2V_o$ . the center point of differential signal is called common mode signal.
- \* the advantage of differential over Single End is it is immune to the noise. the noise coupling will be more in high frequency circuit. this noise can be eliminated by the differential signal.
- \* differential will also reduce power coupling from  $V_{dd}$  to output. consider an example of common source where  $V_{dd}$  change.  $\Delta V$  this will also lead to change at  $V_{out}$ . Since we are taking differential output at output this changes can be cancelled.
- \* differential signalling also increase the output swing. & make circuit highly linear. Some of draw back of differential circuit is it consume more area.

## Basic differential pair

- \* by our intuition we can build differential amplifier as shown in figure 1 and  $V_{in_1}$  &  $V_{in_2}$  to  $V_{cm}$ . and applying differential input at  $V_{in_1}$  &  $V_{in_2}$ . this will give differential output at  $V_{out_1}$  &  $V_{out_2}$ . the problem with this circuit if there is any mismatch in the bias point output will not be differential. this problem is resolved by using differential pair.

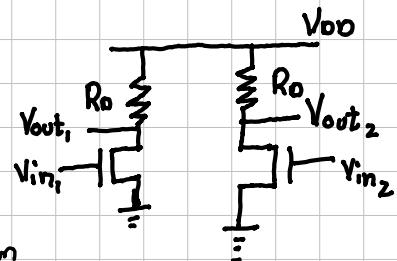
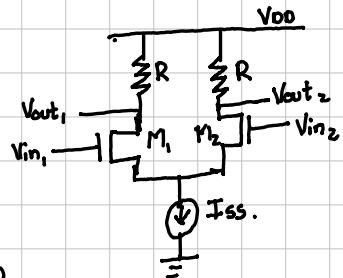


fig 1

\* In differential pair bias is done by current source  $I_{SS}$  where  $I_{SS} = I_1 + I_2$  independent of  $V_{in_1}$  &  $V_{in_2}$ : if  $V_{in_1} = V_{in_2}$  then  $I_1 = I_2 = I_{SS}/2$  and  $V_{out_{cm}} = V_{DD} - \frac{I_{SS} \times R}{2}$



\* for large Signal analysis we can neglect body & channel length modulation Effect ie  $\delta$  &  $\lambda = 0$

## Qualitative Analysis

→ let us assume  $V_{in_1} - V_{in_2}$  varies  $-∞$  to  $∞$

**Case I :-**  $V_{in_1}$  is more negative than  $V_{in_2}$ .

then  $M_1 = \text{off}$ ,  $M_2 = \text{ON}$ ,  $V_{out_1} = V_{DD}$ .

$$V_{out_2} = V_{DD} - \frac{I_{SS} R_D}{2}$$

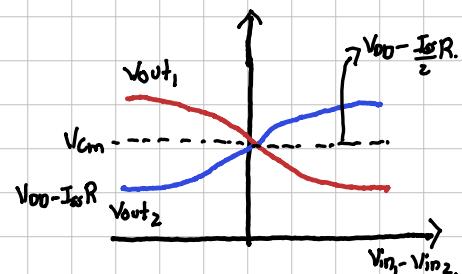


fig - 1

\* as we increase  $V_{in_1}$ ,  $M_1$  starts conducting current in  $M_2$  starts decreasing since  $I_1 + I_2 = I_{SS}$  then  $V_{out_1}$  will reduce &  $V_{out_2}$  will increase.

**Case II :-**  $V_{in_1} = V_{in_2}$

$$\text{then } V_{out_1} = V_{out_2} \text{ i.e. } V_{DD} - \frac{I_{SS} R_D}{2}$$

**Case III :-**  $V_{in_1}$  is more positive than  $V_{in_2}$ .

then  $M_1$  carry more current than  $M_2$  ∴ the voltage at  $V_{out_1}$  is less than  $V_{out_2}$ . if we further increase  $V_{in_1}$  then  $M_2$  will be off then  $V_{out_1} = V_{DD} - I_{SS} R$ . &  $V_{out_2} = V_{DD}$ .

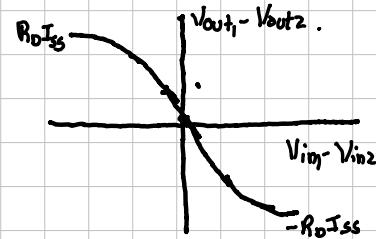


fig - 2

\* The maximum & minimum level are  $V_{DD}$  &  $V_{DD} - I_{SS} R$  which are independent of input common mode voltage.

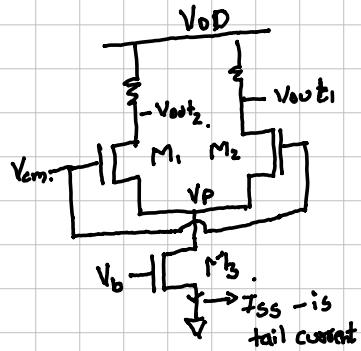
- \* gain will be maximum and linear when  $V_{in_1} = V_{in_2}$  & become more nonlinear as  $|V_{in_2} - V_{in_1}| \gg 0$ . which can be seen from figure-2 of previous page.

## Common mode analysis of differential Amplifier.

- \* let us set  $V_{in_1} = V_{in_2} = V_{cm}$  & vary  $V_{cm}$  from 0 to  $V_{DD}$  and Analysis the above circuit.

### Case I :- $V_{cm} = 0$

when  $V_{cm} = 0$   $M_1$  &  $M_2$  are turned off  $V_{out_1}$  &  $V_{out_2} = V_{DD}$  & transistor  $M_3$  is in triode region. &  $V_p = 0$  & circuit can't be used for amplification.



### Case II :- $V_{cm}$ is increased.

- \* When  $V_p < V_b - V_{Th}$ : Transistor  $M_3$  act as a resistor the circuit will behave has a source follower where  $V_p = V_{cm} - V_{Th}$ . & the current  $I_1$  &  $I_2$  will increase with increase with  $V_{cm}$ .

- \* when  $V_p > V_b - V_{Th}$ : if we further increase  $V_{cm}$   $V_p > V_b - V_{Th}$  the transistor  $M_3$  will be in saturation. this is the ideal condition for amplification . where current  $I_1 + I_2 = I_{SS}$  &  $V_{cm} \geq V_{GS3} + V_{GS3} - V_{Th3}$  .

### Case III :- $V_{cm}$ is increased further

as we increase  $V_{cm} > V_{out} + V_{Th}$ , the transistors  $M_1$  &  $M_2$  will come out of saturation. this set upper limit for  $V_{cm}$

$$V_{GS3} + V_{GS3} - V_{Th3} \leq V_{cm} \leq \min \left[ V_{DD} - \frac{I_{SS}}{2} R + V_{Th}, V_{DD} \right]$$

\*  $V_{cm}$  input is always less than  $V_{cm}$  output. if the gain of the circuit is higher input swing will be lower. output can go as high as  $V_{DD}$  & low as  $V_{cm} - V_{Th}$  for transistor to remain in saturation. the maximum peak to peak output swing is  $V_{DD} - (V_{cm} - V_{Th})$  i.e  $V_{DD} - (V_{GS_1} + V_{GS_3} - V_{Th_3} - V_{Th_1})$ . =  $V_{DD} - (V_{sat_1} + V_{sat_3})$ .

## Large Signal Analysis

\* The output of the system is  $V_{out_1}, -V_{out_2}$ . which is equal to  $V_{DD} - I_1 R - (I_2 R) \Rightarrow R(I_2 - I_1)$ . & the Voltage at node P [previous figure] is  $V_{in_1} - V_{GS_1} = V_{in_2} - V_{GS_2}$  i.e  $V_{in_1} - V_{in_2} = V_{GS_1} - V_{GS_2}$ .

$$V_{GS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} W/L}} + V_{Th}$$

$$V_{in_1} - V_{in_2} = \sqrt{\frac{2 I_{D1}}{\mu_n C_{ox} W/L}} - \sqrt{\frac{2 I_{D2}}{\mu_n C_{ox} W/L}}$$

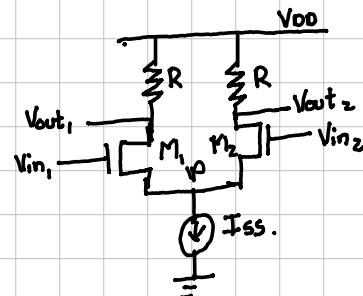
Squaring on both side.

$$(V_{in_1} - V_{in_2})^2 = \frac{2}{\mu_n C_{ox} W/L} \left[ I_{ss} - 2 \sqrt{I_1 I_2} \right]$$

Squaring on both side. & apply ind + 4  $I_1 I_2 = (I_1 + I_2)^2 - (I_1 - I_2)^2$ :

$$\begin{aligned} & \left[ \frac{\mu_n C_{ox} W/L}{2} (V_{in_1} - V_{in_2})^2 - I_{ss} \right]^2 = (I_1 + I_2)^2 - (I_1 - I_2)^2 \\ \Rightarrow & \left( \frac{\mu_n C_{ox} W/L}{2} (V_{in_1} - V_{in_2})^2 + I_{ss}^2 - \mu_n C_{ox} W/L (V_{in_1} - V_{in_2})^2 I_{ss} \right) = (I_{ss})^2 - (I_1 - I_2)^2 \end{aligned}$$

$$I_{D1} - I_{D2} = \sqrt{\mu_n C_{ox} W/L I_{ss} (V_{in_1} - V_{in_2})} \sqrt{1 - \frac{\mu_n C_{ox} (W/L)}{4 I_{ss}} (V_{in_1} - V_{in_2})^2}$$



differencing on both sides.

$$\frac{\partial \Delta I_o}{\partial \Delta V_{in}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[ \frac{\frac{4I_{ss}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{ss}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}} \right]$$

$G_m$  is maximum when  $\Delta V_{in} = 0$  i.e.  $= \sqrt{\mu_n C_{ox} W/L} I_{ss}$

$$\Delta V_{out} = R \Delta I = R G_m \Delta V_{in}.$$

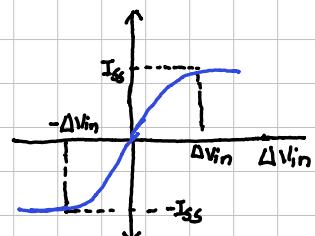
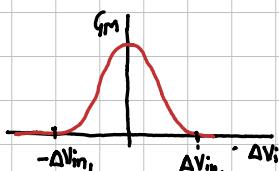
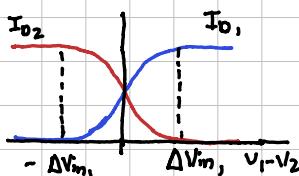
$$\frac{\Delta V_{out}}{\Delta V_{in}} = R G_m = R \sqrt{\mu_n C_{ox} (W/L)} I_{ss}$$

\* Gain is same as gain of single device i.e.  $R \sqrt{2 \mu_n C_{ox} W/L I_{ss}} / 2 = R g_m$ .

\* Gain is zero when  $\Delta V_{in} = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox} W/L}}$

\* As we increase  $|V_{in_1} - V_{in_2}|$  one of the transistors will go off other will draw all the current  $I_{ss}$ .  $\therefore$  the maximum  $\Delta V_{in}$  change is

$$\Delta V_{in} = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox} W/L}}$$



## Small Signal Analysis.

let us ground  $V_{in_2}$  & find the effect of  $V_{in_1}$  on  $V_{out_1}$  &  $V_{out_2}$ .

- \* from fig 2 we can see the output  $V_x$  can be found by considering it as common source amplifier

$$\frac{V_x}{V_{in}} = -\frac{R_o}{Y_{gm_2} + Y_{gm_1}} \quad (1)$$

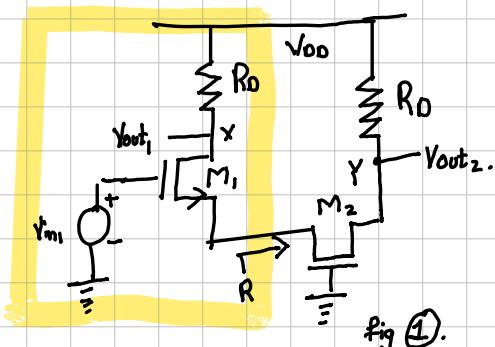


fig (1).

- \* The circuit in the yellow box in fig 1 is an source follower circuit which can be modelled into Thevenin Voltage of  $V_{in}$  with series with resistor of  $Y_{gm}$ , as shown in figure 3 yellow box. and the circuit will behave as the common gate amplifier

$$\therefore \frac{V_x}{V_{in_1}} = \frac{+R_o}{Y_{gm_1} + Y_{gm_2}} \quad (2)$$

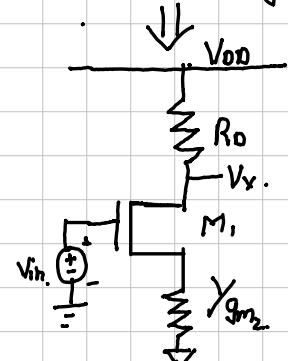


fig (2)

Subtracting 2 from 1.

$$\frac{V_x - V_y}{V_{in_1}} \Big|_{V_{in_2}=0} = \frac{-2R_o}{Y_{gm_1} + Y_{gm_2}}$$

due to symmetry  $V_{in_2}$  when  $V_{in_2}=0$  is same as above output is superposition of both.

$$V_x - V_y = \frac{-2R_o}{Y_{gm_1} + Y_{gm_2}} \left[ V_{in_1} - V_{in_2} \right]$$

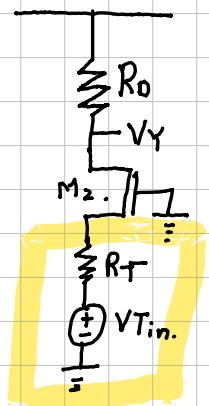


fig (3)

We know that  $g_{m_1} = g_{m_2} = g_m$ . when both transistors are matched

$$V_x - V_y = -g_m R_D [V_{in_1} - V_{in_2}]$$

**Lemma I** :- Consider a Symmetric Circuit where  $D_1$  is symmetric to  $D_2$  and both are linear if we apply differential signal to both the input the node p voltage is constant. For ac Analysis we can assume the node is at virtual ground. as shown in figure 1-b.

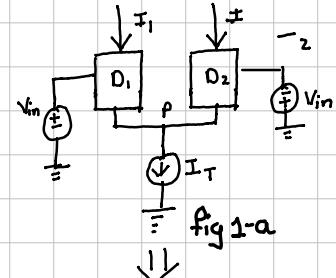


fig 1-a

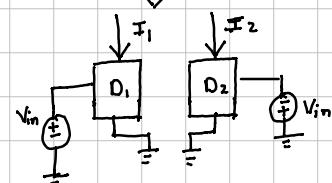


fig 1-b

**Lemma II** :- Consider a Symmetric circuit where  $D_1$  is symmetric to  $D_2$  and both are linear if we apply common mode Signal to both the input. there is no current in Node P we can consider the circuit is open at P. which is shown in figure 2-b.

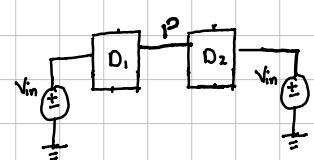


fig 2-a.

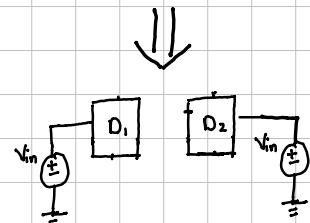


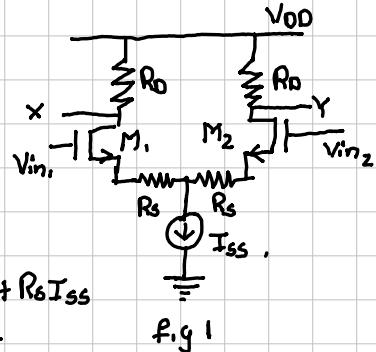
fig 2-b.

## Degenerated Differential pair.

\* this circuit make output more linearize.

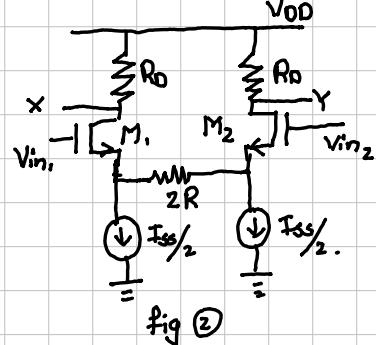
$$* \text{ gain} = \frac{R_D}{Y_{gm} + R_s}$$

$$* \text{ Maximum input range} = V_{in_1} - V_{in_2} = \sqrt{\frac{2I_{SS}}{V_{un} C_{ox} W/L}} + R_s I_{SS}$$



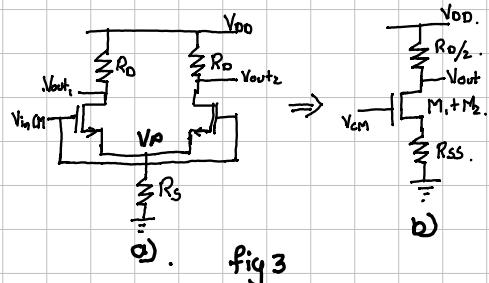
\* The gain of the circuit is reduced. It has less headroom since there is drop ( $I_{SS}/2 R_s$ ) in resistor. and gain is independent of  $gm$ .)

\* The headroom can be increased. in the figure 2 where. there is no current  $2R$  when  $V_{in_1}$  &  $V_{in_2}$  are equal so the drop across  $2R$  is zero. there will be drop only due to differential signal.



## Common mode response

\* Ideally Common mode response should not effect the output response. but due difference in  $gm$  of both the transistor or finite resistance of current mirror. fraction of CM Voltage will appear at the output.



\* let us assume the circuit is symmetric & has finite  $R_s$  as shown in the figure. 3-b. if  $V_{cm}$  is increased  $V_x$  &  $V_y$  decrease due to increase in current. which will change the small signal gain and the output swing the common signal gain is given by.

$$A_{cm} = \frac{V_{out,cm}}{V_{in,cm}} = \frac{R_o/2}{\frac{1}{2}g_m + R_s}$$

\* let us study the mismatch of  $R_o$  on the output of the circuit.

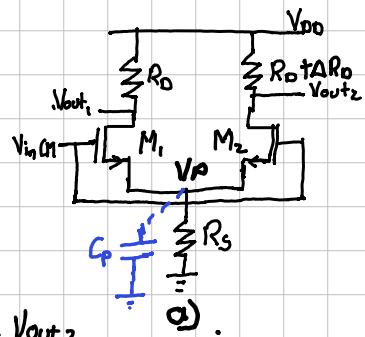
$V_p$  act as a source follower the change in  $V_p$  is given by

$$\Delta V_p = \frac{2R_s}{\frac{1}{2}g_m + 2R_s} V_{in,cm}.$$

$M_1$  &  $M_2$  act as Common Source with Source degenerative when output is taken at  $V_{out_1}$  &  $V_{out_2}$ .

$$\Delta V_{out_1} = -\Delta V_{cm} \frac{R_o}{\frac{1}{2}g_m + 2R_s}$$

$$\Delta V_{out_2} = -\Delta V_{cm} \frac{R_o + \Delta R_o}{\frac{1}{2}g_m + 2R_s}$$



\* If the common mode noise for higher frequency input. due to the parasitic capacitance [C<sub>p</sub>] of current mirror will be high at output is high due to the low impedance path created by cap

## The Effect of Mismatch of transconductance on the output.

\* The mismatch is mainly due the variation in length, width, or  $V_T$  of the mosfet the current in the each Mosfet is given by

$$I_{D_1} = g_{m_1} (V_{in cm} - V_p) \quad \& \quad I_{D_2} = g_{m_2} (V_{in cm} - V_p), \quad (I_{D_1} + I_{D_2}) R_s = V_p$$

$$\therefore (g_{m_1} + g_{m_2}) (V_{in cm} - V_p) R_{ss} = V_p$$

$$V_p = \frac{(g_{m_1} + g_{m_2}) R_{ss}}{(g_{m_1} + g_{m_2}) R_{ss} + 1} V_{in cm}.$$

Output Voltage is given by

$$V_x = -g_{m_1} (V_{cm} - V_p) R_D$$

$$V_x = \frac{-g_{m_1} R_D V_{in cm}}{(g_{m_1} + g_{m_2}) R_{ss} + 1} \quad \& \quad V_y = \frac{-g_{m_2} R_D}{(g_{m_1} + g_{m_2}) R_{ss} + 1} V_{in cm}.$$

$$V_x - V_y = \frac{-[g_{m_1} - g_{m_2}] R_D V_{in cm}}{(g_{m_1} + g_{m_2}) R_{ss} + 1} = \frac{-\Delta g_m R_D V_{in cm}}{(g_{m_1} + g_{m_2}) R_{ss} + 1}$$

\* Common Mode Rejection Ratio :- It is the ratio of differential gain with the common mode gain. for ideal op-amp CMRR will be  $\infty$

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

\* Differential gain of Amplifier with different  $g_m$  is

$$\left| A_{DM} \right| = \frac{R_D}{2} \frac{g_{m_1} + g_{m_2} + 4g_{m_1}g_{m_2} R_{ss}}{1 + (g_{m_1} + g_{m_2}) R_{ss}}$$

$$\therefore CMRR = \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m}$$

$$\approx \frac{g_m(1+2g_m R_{SS})}{\Delta g_m} \quad \text{where} \quad g_m = \frac{g_{m1} + g_{m2}}{2}.$$

## Differential pair with mos load.

\* The gain of the following Circuit is

$$Av = -g_{m_1} \left[ \frac{1}{g_{m_3}} \left| \delta \alpha_3 \right| \right] \delta \alpha_1$$

