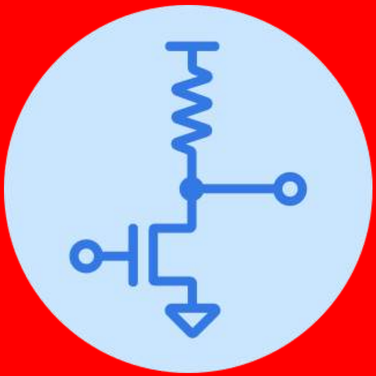
Analog Electronics Notes



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CONTENT.

MOS DEVICE PHYSICS.

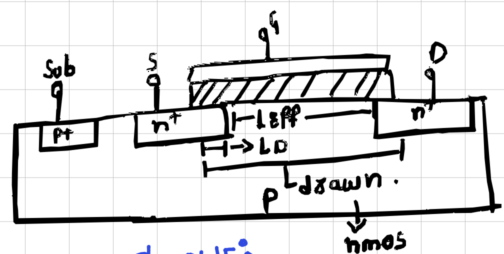
→ The level of abstraction of knowledge required to study analog is
Quantum physics → Solid state physics → Semiconductor physics → device Modelling → design of circults.

Mosfet as switch.

* To use mosfet as a switch. the drain to source Resistane should be very low. when gate voltage of mosfet (nmos) is very high, in ideal case it should be zero. & the resistance should Very high for low gate Voltage. in ideal case it should be infinity.

Mosfet structure.

* The effective length of mosfet is given by $L_{drawn} - 2L_D = L_{eff}$



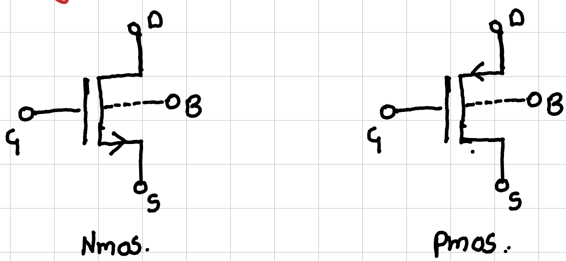
$t_{ox} \approx 15\mathring{A}$

* mosfet is a symetrical device i.e the drain & Source of the device can be interchanged.

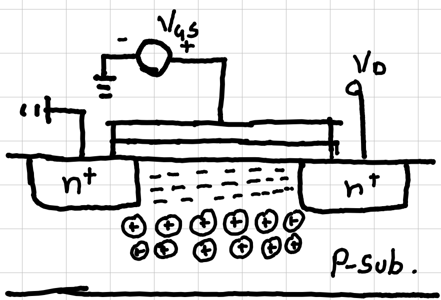
* The Substrate of the mosfet must be reverse bias with respect to Source. or else the current will directly flow from S/D to the substrate, if it is forward bias. this is called latch up.

* PMOS is negatation of nmos. & it is fabricated in an N-well & substrated. is connected to highest potential.

Mosfet Symbol



Mosfet V-I characteristics.



* when we apply Voltage to the gate. the holes move away from gate and electron move towards the gate. this will create a channel. if we increase V_G then the deplection region will increase. this region can be modelled as two cap. i.e gate oxide cap & depletion cap connected in series. if we increase V_G the current will start to flow. then we can say device is inverted. the V_G required for this inverted channel is called V_{TH}. if V_G is increased feasther the charge in depletion region will be same but charge density i.e current will increase.

$$V_{TH} = \phi_{MS} + 2\phi_F + \frac{\phi_{dep}}{C_{ox}}$$

ϕ_{MS} :- Polysilicon & silicon workfunction.

$\phi_F = V_T \ln\left(\frac{N_{sub}}{N_i}\right)$ Nsub → charge density. Ni → intrensic carrier
V_T = thermal voltage.

$$\phi_{dep} = \sqrt{4 q \epsilon_{si} |\phi_F| N_{sub}}$$

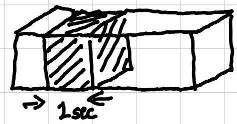
$$C_{ox} = \frac{\epsilon_{si}}{t_{ox}} \approx 17.25\ fF/um^2$$

* for Pmos theory is same but the polarity is reversed.

Derivation of I-V characteristics.

* current in the amount of charge flowed per unit time i.e it is Equal to

$$I_D = Q_d . V \qquad (1)$$



$Q_d \rightarrow$ charge density
$V \rightarrow$ Velocity of charge.

* for $V_{GS} > V_{Th}$ the charge density is Proportional to $V_{GS} - V_{Th}$. for V_{DS} & $V_{GS} = 0$.

$$Q_d = W C_{ox} (V_{GS} - V_{Th}). \qquad (2).$$

* when we increase $V_{DS} > 0$ the channel potential varies from $V_S(x) = 0$ to $V_D(x) = V_{DD}$. $\therefore$ the charge density can be written as.

$$Q_d = W C_{ox} (V_{GS} - V_{Th} - V(x)) - (3)$$ $V(x)$ Varies from 0 to V_D.

* Substitude Equation 3 into 1.

$$I_D = -W C_{ox} (V_{GS} - V_{Th} - V(x)) . V \qquad (4)$$ $V \rightarrow$ velosity of electron.

* Negative sign is due to Negative charge we know that.

$$V = U_n \vec{E} \Rightarrow V = U_n \cdot \frac{dV}{dx} \qquad (5)$$ $V \Rightarrow$ potential.

Substituting Equation 5 in 4.

$$I_D = W C_{ox} (V_{GS} - V_{Th} - V(x)) \times U_n \times \frac{dV}{dx}.$$

Intigrating on both side.

$$\int_0^L I_D dx = \int_{V(0)=0}^{V(L)=0} WC_{ox}\left(V_{GS}-V_{Th}-V(x)\right) \times U_n \times dV$$

∴ the current in channel is given by

$$I_D = \frac{WC_{ox}U_n}{L}\left[(V_{GS}-V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right].$$

* for $V_{GS}-V_{Th} \geq V_{DS}$ ∴ the device act as voltage controlled resistor.

$$I_D \approx \frac{WC_{ox}U_n}{L}\left((V_{GS}-V_{Th})V_{DS}\right)$$

$$\therefore R_{on} = \frac{1}{\frac{W}{L}C_{ox}U_n(V_{GS}-V_{Th})}$$

* for $V_{GS}-V_{Th} < V_{DS}$ the current in the mosfet become constant due to the pintch off. the effective length of transistor decrease. there is current even after the pintch off because there is large electric field in the channel. which will shoot electron to the. drain of mosfet.

$$I_D = \frac{WC_{ox}U_n}{2 \times L'}\left(V_{GS}-V_{Th}\right)^2.$$

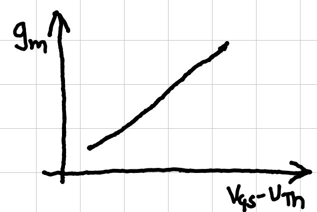
* In saturation mosfet act as the current source when L is constant Nmos current source inject current in to ground. where as pmos current source draw current from the VDD.

MOS Transconductance.

→ The change in drain current with change in gate-source voltage is called trans conductance. it is denoted by g_m.

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}\ \text{const}} \Rightarrow \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th}).$$

$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})$

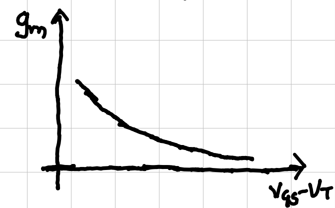


W/L constant

$g_m = \sqrt{2 \times \mu_n C_{ox} \frac{W}{L} I_D}$

W/L constant

$g_m = \frac{2 I_D}{V_{GS} - V_{Th}}.$



I_D constant

* g_m increase with overdrive Voltage when W/L kept constant whereas. g_m decrease with overdrive Voltage when I_D is kept constant.

* the pinch off occurs when Voltage of drain is at $V_{GS} - V_{Th}$ if voltage of drain is increased further the effective length of mosfet is decreased and current is given by

$$I_D = \frac{u W}{2 L'} C_{ox} (V_{GS} - V_{Th})^2$$ L' -> effective length after pinch off

* mobility of eletron is twice the mobility of holes

> Transconductance of mosfet

* $$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\text{constant } V_{DS}} \Rightarrow u \frac{W}{L} C_{ox} (V_{GS} - V_{Th}) \Rightarrow \sqrt{2 u \frac{W}{L} C_{ox} I_D}$$

Body effect.

-> when Negative Voltage is applied to the body, more positive charge hole move towards the body which will increase. the channel width. in order to balance. this charge we need to add more positive charge to the gate. this will increase the V_{Th} of the transistor.

$$V_{Th} = V_{Tho} + \gamma \left[\sqrt{2\phi_F + \phi_{SB}} - \sqrt{2\phi_F} \right] \qquad \gamma = \frac{\sqrt{2 q \epsilon_{Si} N_{sub}}}{C_{ox}}$$

-> γ range is from 0.3 to 0.4

Channel length modulation.

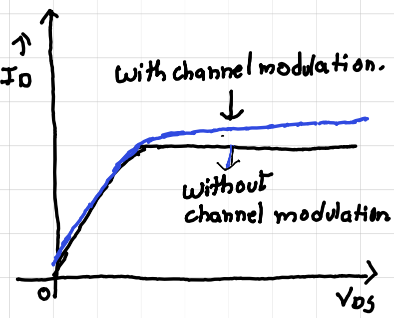
-> The length of the channel will decrease when the voltage of the Drain. increase. in other words the current i_d is function of V_{DS}. the effective change in length is given by.

$$L' = L - \Delta L. \quad \therefore \frac{L'}{L} = 1 - \frac{\Delta L}{L}.$$

$$I_d = \frac{KW}{L \times \frac{L'}{L}}(V_{GS}-V_T)^2 \Rightarrow \frac{KW \cdot (V_{GS}-V_T)^2}{L \times \left[1-\frac{\Delta L}{L}\right]} \qquad K \Rightarrow \frac{C_{ox} \times \mu_n}{2}.$$

$$I_d \approx \frac{KW}{L}(V_{GS}-V_T)^2\left[1+\frac{\Delta L}{L}\right]. \qquad \frac{\Delta L}{L} \propto V_{DS} \Rightarrow \frac{\Delta L}{L} = \lambda V_{DS}.$$

$$I_d \approx \frac{KW}{L}(V_{GS}-V_T)^2\left[1+\lambda V_{DS}\right].$$



→ λ is called channel modulation coefficient

→ the gm of the transistor is.

$$g_m = 2\frac{KW}{L}(V_{GS}-V_T)(1+\lambda V_{DS}). \qquad K = \frac{C_{ox}\mu}{2}$$

→ This formula is less accurate for small channel mosfet. In short channel mosfet I_D is also dependent on V_{DS}.

Subthreshold conductance.

→ we have assumed that the current in mosfet is zero for $V_{GS} < V_T$ but this assumption is not right. there is current in the channel. this current is due to the. weak inversion. & the current will rise exponentially with respect to V_{GS}. when subthreshold current reaches 100nA the gate voltage is taken as V_T of transistor.

$$I_D = I_0 e^{\frac{V_{GS}}{nV_t}} \qquad I_0 \propto W/L. \qquad n \rightarrow \text{Ideality factor} \qquad V_T \rightarrow \text{thermal voltage}.$$

→ for voltage below V_T the current will drop 10 time per 80mV of voltage drop.

Mos device model :-

→ Parasatic caps of mosfet

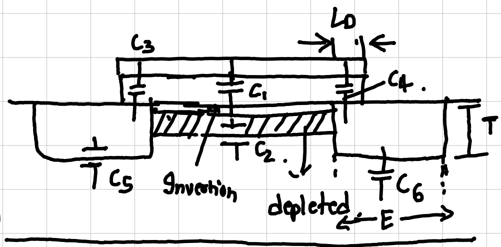
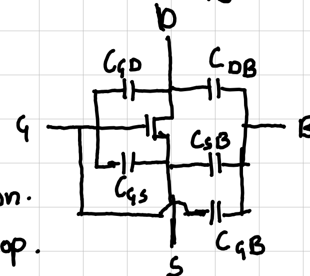


fig 1

- → gate to channel → C_1 (oxide).
- → channel to substrate → C_2 (depletion)
- → gate to Source & Drain → C_3 & C_4 → (overlap).
- → Substrate to source & drain → C_5 & C_6 → (Junction)

$C_1 = WL C_{ox}$. $C_{ox} = \varepsilon / t_{ox}$.



$C_2 = WL\sqrt{q\varepsilon_{Si}N_{sub}/(4\phi_F)}$

N_{sub} → donar Concentration.

ϕ_F → Voltage drop.

C_3 & C_4 ⇒ $C_{ox} L_D \times W$

⇒ $C_{ov}W$ → C_{ov} → overlap cap per unit width.

C_5 & C_6

- → $C_j \times$ Area → due to bottom plate. ⇒ Area $= W \times E$ from fig 1.
- → $C_{jsw} \times$ Perimeter → due to Side wall (perimeter) ⇒ perimeter $= 2(W+E)T$

$$C_j = C_{j0} \Big/ \left[1 + \frac{V_R}{\phi_B}\right]^m.$$

→ V_R → reverse bias voltage.
→ ϕ_B → built in potential.
m → 0.3 to 0.4

→ Similary for C_{jsw}

→ C_{jsw} for region marked in yellow from figure 2 may be different compared to region marked in pink. but we assume it is Equal to other regions

fig2

Case I ⇒ when device is off $V_{GS} < V_{Th}$.

1) $C_{GD} = C_{GS} = C_{ov} W$

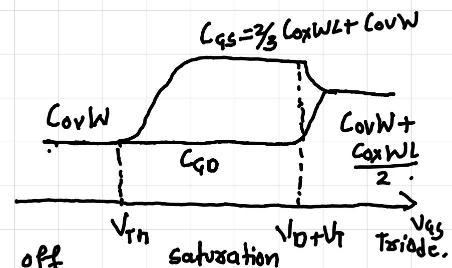
2) gate to bulk ⇒ $C_1 \| C_2$

3) C_{DB}, C_{SB} ⇒ depends on bias voltage with substrate.

Case II :- when device is in triode, $V_{GS} > V_{Th}$ $V_S = V_D$

1) the gate to channel capacitance is divide between source & drain.

1) $C_{GD} = C_{GS} = C_{ov} W + \frac{C_{ox} WL}{2}$.



Case III :- when device is in saturation.
$V_{GS} > V_{Th}$ $V_{GS} - V_T < V_{DS}$.

$C_{GS} = \frac{2}{3} C_{ox} WL + C_{ov} W$

$C_{GD} = C_{ov} W$

* the capacitance doesn't provide smooth tranition from one region to other. this will create difficult to converge in Simulation.

* C_{GB} is Negleted in Saturation & triode region. because of formation of channel which act as a sheid between gate & bulk.

Mos small signal model

-> Small signal analysis is applied when perturbation is small & & non-linear effect are not conserned.

-> drain current is the function of drain Voltage which is modelly by

$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 \lambda} = \frac{1}{I_D \lambda}.$$

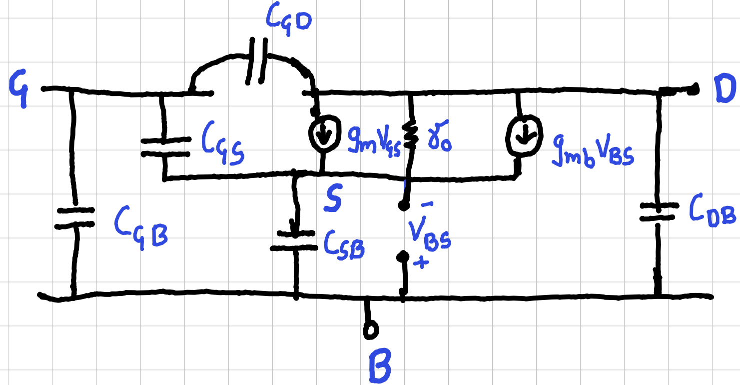
-> the bulk potential effect the threshold Voltage of mosfet. It effect the current I_D. it behave as the second gate.

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = u_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \frac{\partial V_{Th}}{\partial V_{BS}}.$$

$$\frac{\partial V_{Th}}{\partial V_{BS}} = -\frac{\partial V_{Th}}{\partial V_{SB}} = -\frac{\gamma}{2} (2\phi_F + V_{SB})^{-1/2}$$

$$g_{mb} = g_m \eta \quad \text{where } \eta = -\frac{\gamma}{2} (2\phi_F + V_{SB})^{-1/2}.$$

Small signal model.



-> for Pmos the small signal is similar to that of nmos.

level one Spice parameters :-

* VTO :- threshold Voltage with zero V_{SB} → V
* GAMMA :- body-Effect co-Efficient → $V^{1/2}$.
* PHI :- $2\phi_F$ → V
* TOX :- gate oxide thickness → m.
* NSUB :- Substrate doping → cm^{-3}
* LD :- source/drain side diffusion → m.
* UO :- channel mobility → $cm^2 s/V$.
* LAMBDA :- channel-length modulation. coefficient → V^{-1}
* CJ :- source/drain bottom-plate junction capacitance per unit area. F/m^2
* CJSW :- Sidewall junction capacitance Per unit length → F/m.
* PB :- Source/drain. Junction built-in potential. → V
* MJ :- Exponent in CJ Equation → unitless
* MJSW :- Exponent in CJSW Equation → Unitless.
* CGDO :- gate-drain overlap capacitance per unit Width → F/m.
* CGSO :- gate-source overlap capacitance per unit width → F/m.
* JS :- source/drain leakage current per unit area → A/m^3

SINGLE STAGE AMPLIFIERS.

* The ideal input and output relation of amplifier $y(t) = a_0 + a_1 x(t)$.

* the real input & output relation of amplifier due to distortion is given by $y(t) = a_0 + a_1 x(t) + \underbrace{a_2 x^2(t) + a_3 x^3(t) \ldots\ldots}_{\text{higher order harmonics.}}$

* Parameters that used to Evaluate the performance of amplifier are
  1) speed 2) gain 3) maximum swing 4) power consumtion
  5) supply Voltage 6) linearity 7) input ouput impedence.

Amplifier categories

Comman Source amplifier
- ↳ with resistor load
- ↳ diode connected load.
- ↳ current-source load
- ↳ Active load.
- ↳ Source degenerative.

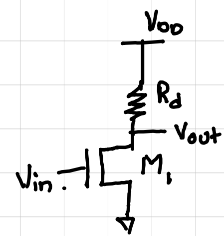
Source follower
- ↳ resistive bias
- ↳ current-source bias.

common gate.
- ↳ resistive load
- ↳ current-source load.

cascode
- ↳ telescopic
- ↳ Folded.

Comman Souxce Stage. [CS].

* CS with Resistance.



$$\therefore V_{out} = V_{DD} - R_d \times \left[\frac{1}{2} C_{ox} \frac{W}{L} u_n (V_{GS} - V_{TH})^2 \right]$$

triode region $V_{out} < V_{in} - V_{Th}$.

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D u_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \doteq -g_m R_D.$$

* Since g_m is function of V_{in} the swing of signal should be small to prevent non linear behaviour.

$$A_v = -\sqrt{2 u_n C_{ox} \frac{W}{L} I_D} \frac{V_{RD}}{I_D} \Rightarrow -\sqrt{2 u_n C_{ox} \frac{W}{L}} \frac{V_{RD}}{\sqrt{I_D}}$$

* Av canbe increased by increasing W/L which in lead to increase. in cap & high V_{RD} which will reduce the swing

* if V_{RD} is kept constant and I_D is reduced which will increase R_D & the time constant

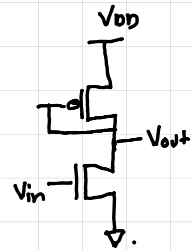
* for large R_D the channel length modulation become signifant.

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D C_{ox} \frac{W}{L} u_n (V_{in} - V_{Th})(1 + \lambda V_{DS}) - \frac{R_D C_{ox}}{2} \frac{W}{L} (V_{in} - V_{th})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

$$A_v = -g_m R_D - \frac{R_D}{r_o} A_v = A_v = -g_m [R_D \| r_o].$$

* Maximum. gain is achived when $R_D = \infty$ ie $= -g_m r_o$ which is almost Equal to 10.

CS Stage with diode connected load.



It is difficult to fabricate resistor on chip so we use diode connected resistor to get resistor. the resistance of diode connected resistor is Equal to.

$$r = \frac{1}{g_{mp}+g_{mbp}} \parallel r_{op} \approx \frac{1}{g_{mp}+g_{mbp}}.$$

$$\therefore \text{ gain } A_V = -g_{m_n} r \parallel r_{on} = -g_{mn}\left(\frac{1}{g_{mp}+g_{mbp}} \parallel r_{on}\right) \approx \frac{-g_{mn}}{g_{mp}+g_{mbp}}$$

$$\therefore A_V = \frac{-g_{mn}}{g_{mp}(1+\eta)} = \frac{\sqrt{W/L \times u_n}}{\sqrt{W/L \times u_p}} \times \frac{1}{(1+\eta)} \qquad \eta = \frac{g_{mbp}}{g_{mp}}$$

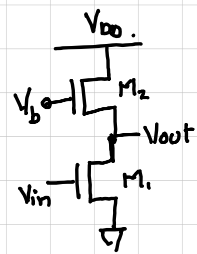
* the gain is independent of bias current or Voltage it is more linear Compared to previous amplifier.

* gain is weak function of W/L if $u_n = 2u_p$ then $(W/L)_n = 12.5(W/L)_p$ to get gain of 5.

* In today technology channel length modulation can't be ignored $\therefore$ gain is given by

$$A_V = -g_{m_n}\left(\frac{1}{g_{mp}+g_{mbp}} \parallel r_{on} \parallel r_{op}\right).$$

CS Stage with Current Source.



* to achive higher gain we need to have larger R_o in order to achive that we use current source.

$$A_v = -g_m \left(r_{o_1} \| r_{o_2} \right).$$

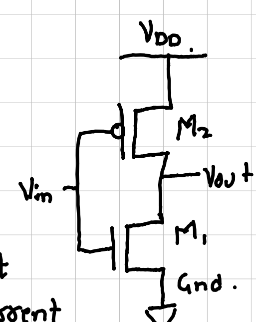
-> to achive larger swing V_{dsat} of m_2 should be less. this can be achived by increasing width. but this will lead to reduction of r_{o_2}. then we have to change λ by increasing length to increase r_{o_2}. but increasing in width will also increase the capacitance at output node.

$$g_{m_1} r_{o_1} = \sqrt{2\left(\frac{W}{L}\right) \mu_n C_{ox} I_D} \, \frac{1}{I_D \lambda}$$

* gain increase. with increasing L as λ is function of L.
* gain increase with decrease in I_D

* increase in length of M_2 will increase r_{o_2} but it will also increase the V_{Dsat} of M_2.

CS Stage with active load



* the gain of the fallowing circult is

$$A_v = -\left(g_{m_1} + g_{m_2} \right) \left(r_{o_1} \| r_{o_2} \right)$$

* the fallowing circult has same impedence as current source circult but it has higher gain compared to current source.

* Since $V_{GS_1} + |V_{GS_2}| = V_{DD}$. the variation in V_{DD} or V_{TH} will translate.

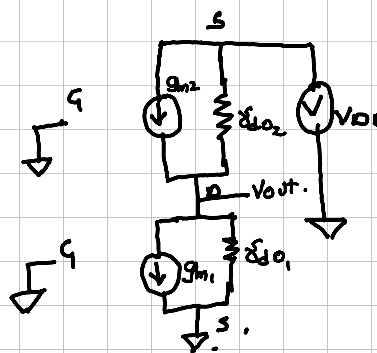
1

to current at output. the bias point of the circuit depends upon the PVT. this is the draw back of the circuit.

* the output gain given by variation in supply

$$V_{out} = \left(g_{m_2} V_{DD} r_{o_2} + V_{DD}\right) \frac{r_{do_1}}{r_{do_2} + r_{do_1}}$$

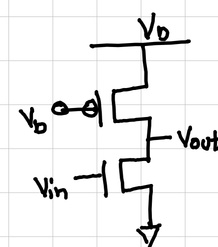
$$\therefore \frac{V_{out}}{V_{DD}} = \frac{(g_{m_2} r_{o_2} + 1)\, r_{do_1}}{r_{do_2} + r_{do_1}}.$$



- CS with triode load.

* here mosfet is operating in deep triode.

$$R_{on} = \frac{1}{\frac{W_2}{L_2} C_{ox_2} \mu_{n_2} (V_{DD} - V_b - V_T)}.$$



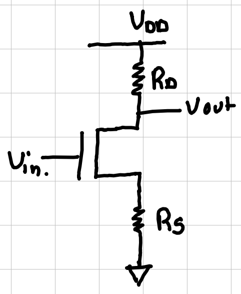
* the draw back of the fallowing circuit is the Ron depend on. V_b, V_T, W, L, V_{DD} which change with PVT. and it is difficult to produce constant bias voltage. V_b.

CS with Source degenerated.

* this configration will make output more linear compared to other configration. it make gain less dependent on gm

* the ouput of this circuit is linearized but the gain is reduced due to the. feed back.

$$G_M = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial I_D}{\partial V_{GS}} \times \frac{\partial V_{GS}}{\partial V_{in}} \quad (1)$$



We know that

$$V_{GS} = V_{in} - I_D R_S .$$

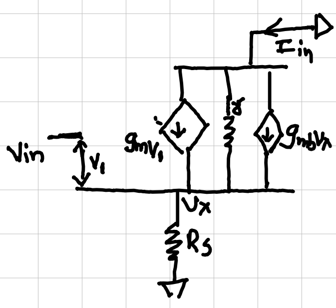
$$\therefore \frac{\partial V_{GS}}{\partial V_{in}} = \left(1 - \frac{\partial I_D}{\partial V_{in}}\right) R_S \Rightarrow \left(1 - G_M\right) R_S \quad (2)$$

Substitute 2 in (1).

$$G_M = g_m \left[1 - G_M\right) R_S \Rightarrow G_M = \frac{g_m}{1 + g_m R_S}.$$

$$\therefore \text{Small signal gain} = -G_M R_D = \frac{-g_m R_D}{1 + g_m R_S} \approx \frac{-R_D}{R_S} \quad \text{if } g_m R_S >> 1.$$

* Gain of source degenerative circuit with body effect and channel length modulation is given below.



$$\therefore I_{out} = g_m V_1 - g_{mb} V_x - \frac{I_{out} R_S}{r_o}.$$

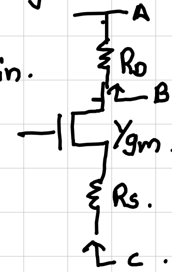
$$I_{out} = g_m \left(V_{in} - I_{out} R_S\right) + g_{mb}\left(-I_{out} R_S\right) - \frac{I_{out} R_S}{r_o}$$

$$G_M = \frac{g_m r_o}{R_S + \left[1 + (g_m + g_{mb}) R_S\right] r_o}$$

$$A_v = \frac{-g_m r_o \,||\, R_{eq}}{R_S + \left[1 + (g_m + g_{mb}) R_S\right] r_o}$$

$$R_{eq} = R_D \,||\, \left[R_S + r_o + (g_m + g_{mb}) r_o R_S\right]$$

finding gain by inspection for source degeneration



gain is equal to impedence looking into drain. divide by the impedence looking into the. source→c.

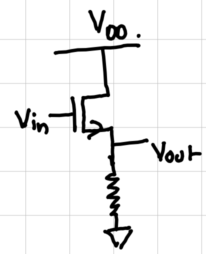
$$A_V = \frac{-R_D}{1/g_m + R_D}. \Rightarrow \frac{R_{AB}}{R_{BC}.} = \frac{-R_D}{1/g_m + R_S}$$

* after source degeneration output resistance is increase therefore output resistance is

$$R_{out} = \left[\left[1 + (g_m + g_{mb}) R_S\right] r_o + R_S\right] \| R_D$$

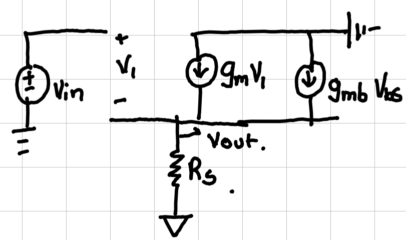
* any circult can be represented by nortan equivalent circult. by short circult current parallel with open circult resistance. and gain is given by $-G_M R_{Eq}$.

Source follower -> Common drain.



* To achive large gain for common source we need to have large output resistance. when this is connected to next stage with low impedence. the effective impedence decrease. so the voltage. gain. we can use source follower as a buffer between two stage. the gain of source follower is almost equal to 1.

$V_{bs} = -V_{out}$



$$V_{out} = R_s\left[g_m V_1 - g_{mb} V_{out}\right].$$

$$V_{out} = R_s\left[g_m\left[V_{in} - R_s V_{out}\right] - g_{mb} V_{out}\right].$$

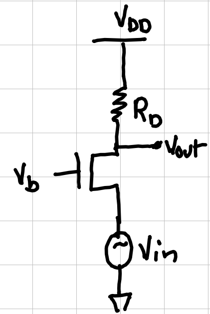
$$\frac{V_{out}}{V_{in}} = \frac{g_m R_s}{1+\left[g_m+g_{mb}\right]R_s}. \quad \text{if } (g_m+g_{mb})R_s \gg 1 \approx \frac{g_m}{g_m+g_{mb}} \approx \frac{1}{1+\eta}. =$$

* Even $R_s = \infty$ the output gain will not be Equal to 1.
* if V_{in} increase by $\sqrt{2}$ Iout & Vout will increase by 2 this will. Create non-linearity in gain to resolve this issue output resistance is replaced by a constant Current Source.

* It has high input impedence & moderate output impedence.

* It has low output headroom for swing.

Comman gate.



* $V_{out} = V_{DD} - \frac{1}{2} u_o C_{ox} \frac{W}{L} \left(V_b - V_{in} - V_{Th}\right)^2 R_D.$

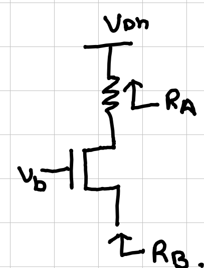
$\therefore$

$$\frac{\partial V_{out}}{\partial V_{in}} = -\frac{1}{2} u_o C_{ox} \frac{W}{L} \left(V_b - V_{in} - V_{Th}\right)\left(-1 - \frac{\partial V_{Th}}{\partial V_{in}}\right) R_D.$$

$$\frac{\partial V_{Th}}{\partial V_{in}} = \frac{\partial V_{Th}}{\partial V_{SB}} \frac{\partial V_{SB}}{\partial V_{in}} = \eta \times \frac{\partial V_{in}}{\partial V_{in}} = \eta$$

$$A_V = +\frac{1}{2} u_o C_{ox} \frac{W}{L} \left(V_b - V_{in} - V_{Th}\right)\left(1 + \eta\right) R_D.$$

$$A_V = g_m (1+\eta) R_D.$$

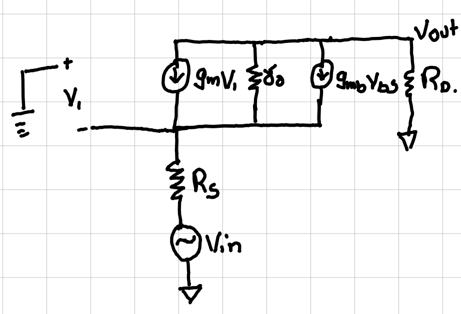


gain by inspection. $= \frac{\text{Impedence at drain } (R_A)}{\text{Impedence at source } (R_B)} = \frac{R_D}{1/(g_m + g_{mb})}$

$= (g_m + g_{mb}) R_D$

* gain considering r_o & R_s.

$V_1 = +\frac{R_s V_{out}}{R_D} - V_{in}.$ ①



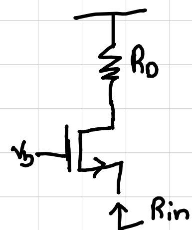
$r_o \left[\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1 \right] - \frac{V_{out}}{R_D} R_s + V_{in} = V_{out}$ ②

from 1 & 2.

$$A_V = \frac{\left((g_m + g_{mb}) r_o + 1\right) R_D}{r_o + (g_m + g_{mb}) r_o R_s + R_s + R_D}$$

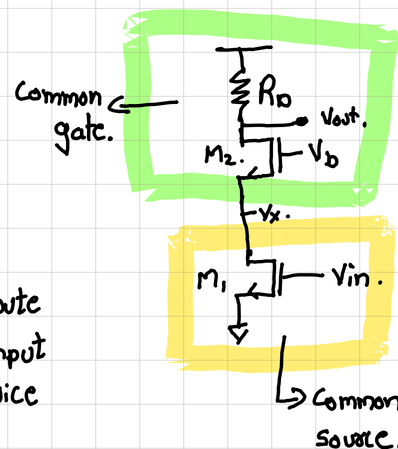
* Input impedence at the Source is

$$R_{in} = \frac{R_D + r_o}{1 + (g_m + g_{mb}) r_o}$$



Cascode stage.

* the input from common Source is Converted into current & this current is feed to common gate this type of configration is called cascode stage



* M_1 provide the gain to small signal vin & M_2 route the current to the R_D. device M_1 is called input device & device M_2 is called cascode. the device configration is called telescopic cascode.

* let us consider if we apply ΔV voltage to Vin. and $r = \lambda = 0$. $r_{o_2} = \infty$ then output current is $g_{m_1} \Delta V$. the voltage at V_x is $\left(1/g_{m_2} \right) g_{m_1} \Delta V$ & the. Voltage at the output is $R_D g_{m_1} \Delta V$.

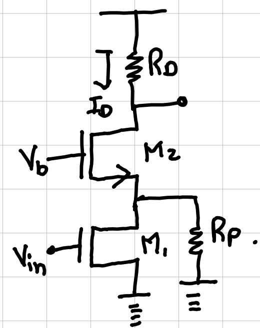
* let us consider if we keep Vin constant & vary V_b. the Mosfet M_1 act as a current source. the node X act as Source follower which has gain Equal to 1. the node ouput doesn't change with. the input due to constant current is flowing in the circult.

* To get both the device into saturation we need to have $V_{out} \geq V_{dsat1} + V_{dsat2}$.

$A_v = -I_D R_D$

$$I_D = \frac{R_P}{R_P + \frac{1}{g_m + g_{mb}}} g_{m_1} V_{in}. \quad \text{Assume } r_{o2} = \infty$$

→ current divider between resistance at M_2 & R_P.



$$A_V = \frac{-R_P \times R_D}{R_P + \frac{1}{g_m + g_{mb}}} g_m V_{in}.$$

$$R_{in} \text{ of figure } 2 = r_{o2} + r_{o1} + (g_{m_2} + g_{mb}) r_{o2} r_{o1}$$

$$\approx (g_{m_2} + g_{mb}) r_{o2} r_{o1}$$

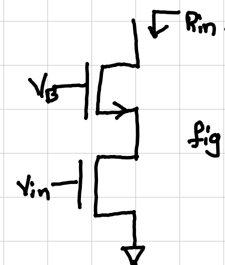


fig ②

gain for figure 3 is

$A_v = G_m R_{out}$

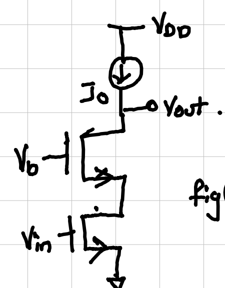


fig ③.

$$R_{out} = r_{o1} + r_{o2} + (g_{m_2} + g_{mb2}) r_{o2} r_{o1}.$$

$$I_{out} = \frac{r_{o1} g_m V_{in}.}{r_{o2} + \left(\frac{1}{g_{m_1} + g_{mb2}}\right) \| r_{o2}}.$$

$$A_v = G_m R_{out} \Rightarrow g_{m_1} r_{o1} \left[(g_{m2} + g_{mb2}) r_{o2} + 1 \right].$$

The output impedence of figure 1 is .

$$\left[r_{o4}+r_{o3}+(g_{m3}+g_{mb3})r_{o3}r_{o4}\right] \,\|\, \left[r_{o2}+r_{o1}+(g_{m2}+g_{mb})r_{o1}r_{o2}\right]$$

gain $A_V \approx g_{m1}\left[(g_{m3}+g_{mb3})\cdot r_{o3}r_{o4} \,\|\, (g_{m2}+g_{mb2})r_{o2}r_{o1}\right]$.

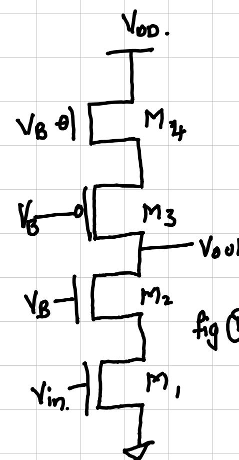


fig ①

* Since cascode has high impedence it can be used as shield for voltage variations. in the circuit.

Folded cascode.

* cascode circuit can also be made by using PMos - Nmos or Nmos - pmos configuration.

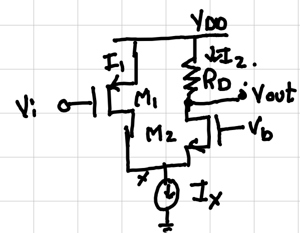


fig ②

* the current $I_X = I_1 + I_2$

* In fig 2 Vin become more positive. I_1 decrease. forcing I_{D2} to increase. hence Vout to drop.

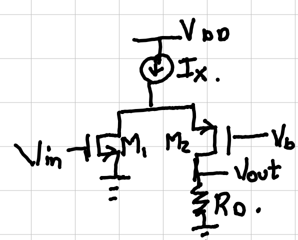


fig ③.

* if Vin (figure 2) decrease from V_{DD} to zero M_2 carries all current & $V_{in} < V_{DD} - V_{Th}$. then $I_2 = I_X - I_1$, $V_{out} = V_{DD} - I_2 R_D$.

* if Vin is decreased further. $I_1 = I_X$ & $I_2 = 0$.

* if Vin falls below this level i.e $I_1 > I_X$ then M_1 enters into triode. region.

DIFFERENTIAL AMPLIFIERS

* Single Ended :- output is taken between ground & the Signal.

* differential Signal :- the signal is measured between two nodes. & the two nodes should have Equal impedence to the potential. if single End peak to peak is V_0. the differential peak to peak is $2V_0$. the center point of differential signal is called common mode signal.

* the advantage of differential over Single End is it is immune to the noise. the noise coupling will be more in high frequency circuit. this noise can be eleminated by the differential signal.

* differential will also reduce power coupling from V_{DD} to output. consider an Example of common source where Vdd charge. ΔV this will also lead to change at Vout. Since we are taking differential output at output this changes can be cancelled.

* differential signalling also increase the output swing. & make circuit highly linear some of draw back of differential circuit is it consume more area.

Basic differential pair

* by our intuition. we can build differential amplifier as shown in figure 1 and V_{in_1} & V_{in_2} to V_{cm}. and applying differential input at V_{in_1} & V_{in_2}. this will give differential output at V_{out_1} & V_{out_2}. the problem with this circuit if there is any mismatch in. the bias point output will not be differential. this problem is resolved by using differential pair.

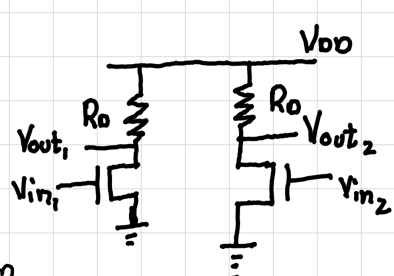
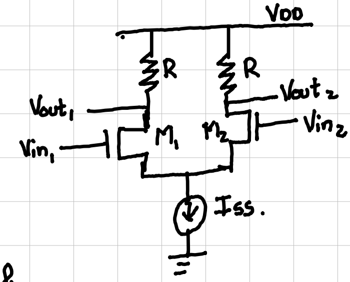


fig 1

* In differential pair bias is done by current Source I_{SS} where $I_{SS} = I_1 + I_2$ independent of V_{in_1} & V_{in_2} : if $V_{in_1} = V_{in_2}$ then $I_1 = I_2 = I_{SS}/2$ and $V_{out\,cm} = V_{DD} - \frac{I_{SS}}{2} \times R$



* for large signal analysis we can neglect body & channel length modulation effect i.e γ & $\lambda = 0$

Qualitative Analysis

→ let us assume $V_{in_1} - V_{in_2}$ varies $-\infty$ to ∞

Case I :- V_{in_1} is more negative than V_{in_2}.
then $M_1 = $ off $M_2 = $ ON, $V_{out_1} = V_{DD}$.
$V_{out_2} = V_{DD} - I_{SS} R_D$

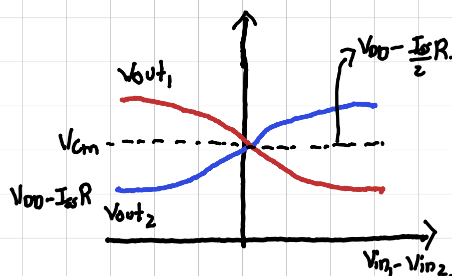


fig-1

* as we increase V_{in_1} M_1 starts conducting current in M_2 starts decreasing since $I_1 + I_2 = I_{SS}$ then V_{out_1} will reduce & V_{out_2} will increase.

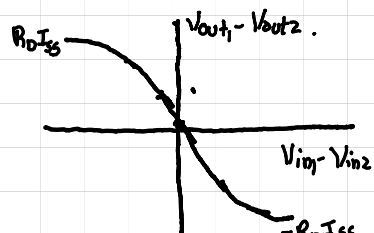


fig-2.

Case II :- $V_{in_1} = V_{in_2}$
then $V_{out_1} = V_{out_2}$ i.e $V_{DD} - \frac{I_{SS}}{2} R_D$.

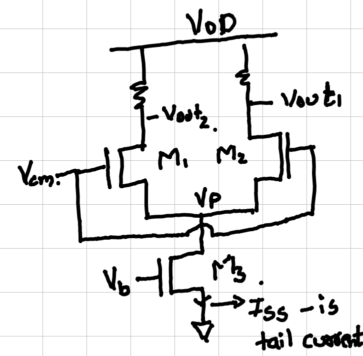
Case II :- V_{in_1} is more positive than V_{in_2}.
then M_1 carry more current than m_2 ∴ the Voltage at V_{out_1} is less than V_{out_2}. if we further increase V_{in_1} then M_2 will be off then $V_{out_1} = V_{DD} - I_{SS} R$. & $V_{out_2} = V_{DD}$.

* The maximum & minimum level are V_{DD} & $V_{DD} - I_{SS} R$ which are independent of input common mode voltage.

* gain will be maximum and linear when $V_{in_1} = V_{in_2}$ & become more nonlinear as $|V_{in_2} - V_{in_1}| \gg 0$. which can be seen from figure-2 of previous page.

Comman mode analysis of differential Amplifier.

* let us set $V_{in_1} = V_{in_2} = V_{cm}$ & vary V_{cm} from 0 to V_{DD} and Analysis the above circuit.



Case I :- $V_{cm} = 0$

when $V_{cm} = 0$ M_1 & M_2 are turned off V_{out_1} & $V_{out_2} = V_{DD}$ & transistor M_3 is in triode region. & $V_p = 0$ & circuit can't be used for amplification.

Case II :- V_{cm} is increased.

* when $V_p < V_b - V_{Th}$: Transistor M_3 act as a resistor the circuit will behave has a source fallower where $V_p = V_{cm} - V_{Th}$. & the current I_1 & I_2. will increase with increase with V_{cm}.

* when $V_p > V_b - V_{Th}$: if we further increase V_{cm} $V_p > V_b - V_{Th}$ the transistor M_3 will be in saturation. this is the ideal condition for amplification. where current $I_1 + I_2 = I_{SS}$ & $V_{cm} \geq V_{GS_1} + V_{GS_3} - V_{Th_3}$.

Case III :- V_{cm} is increased further

as we increase $V_{cm} > V_{out} + V_{Th_1}$ the transistor M_1 & M_2 will come out of saturation. this set upper limit for V_{cm}

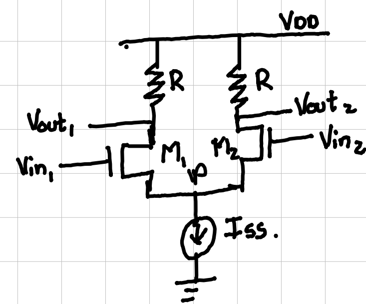
$$V_{GS} + V_{GS_3} - V_{Th_3} \leq V_{cm} \leq \min\left[V_{DD} - \frac{I_{SS}}{2}R + V_{Th},\ V_{DD}\right]$$

* V_{cm} input is always less than V_{cm} output. if the gain of the circuit is higher input swing will be lower. output can go as high as V_{DD} & low as $V_{cm} - V_{Th}$ for transistor to remain in saturation. the maximum peak to peak output swing is $V_{DD} - (V_{cm} - V_{Th})$ i.e $V_{DD} - (V_{GS_1} + V_{GS_3} - V_{Th_3} - V_{Th_1})$. $= V_{DD} - (V_{Dsat_1} + V_{Dsat_3})$.

Large Signal Analysis

* The output of the system is $V_{out_1} - V_{out_2}$. which is equal to $V_{DD} - I_1 R - (V_{DD} - I_2 R) \Rightarrow R(I_2 - I_1)$. & the Voltage at node P [previous figure] is $V_{in_1} - V_{GS_1} = V_{in_2} - V_{GS_2}$ i.e $V_{in_1} - V_{in_2} = V_{GS_1} - V_{GS_2}$.

$$V_{GS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} W/L}} + V_{Th}.$$



$$V_{in_1} - V_{in_2} = \sqrt{\frac{2 I_{D_1}}{\mu_n C_{ox} W/L}} - \sqrt{\frac{2 I_{D_2}}{\mu_n C_{ox} W/L}}.$$

Squaring on both side.

$$(V_{in_1} - V_{in_2})^2 = \frac{2}{\mu_n C_{ox} W/L}\left[I_{ss} - 2\sqrt{I_1 I_2}\right]$$

Squaring on both size. & applying $+4 I_1 I_2 = (I_1 + I_2)^2 - (I_1 - I_2)^2$:

$$\left[\frac{\mu_n C_{ox} W/L}{2}(V_{in_1} - V_{in_2})^2 - I_{ss}\right]^2 = (I_1 + I_2)^2 - (I_1 - I_2)^2.$$

$$\Rightarrow \left(\frac{\mu_n C_{ox} W/L}{2}\right)^2 (V_{in_1} - V_{in_2})^4 + I_{ss}^2 - \mu_n C_{ox} W/L (V_{in_1} - V_{in_2})^2 I_{ss} = (I_{ss})^2 - (I_1 - I_2)^2.$$

$$I_{D_1} - I_{D_2} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{ss}}\,(V_{in_1} - V_{in_2}) \sqrt{1 - \frac{\mu_n C_{ox}(W/L)}{4 I_{ss}}(V_{in_1} - V_{in_2})^2}$$

differencing on both side.

$$\frac{\partial \Delta I_o}{\partial \Delta V_{in}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[\frac{\frac{4 I_{ss}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4 I_{ss}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}} \right]$$

G_M is maximum when $\Delta V_{in} = 0$ i.e $= \sqrt{\mu_n C_{ox} W/L \, I_{ss}}$

$$\Delta V_{out} = R \Delta I = R G_M \Delta V_{in}.$$

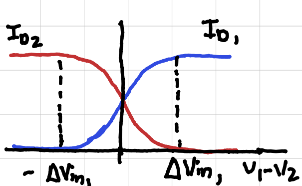
$$\frac{\Delta V_{out}}{\Delta V_{in}} = R G_M = R\sqrt{\mu_n C_{ox} (W/L) I_{ss}}$$

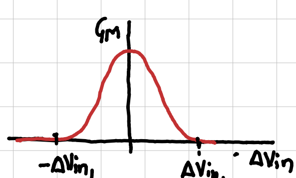
* Gain is same as gain of single device i.e $R\sqrt{2 \times \mu_n C_{ox} W/L \times \frac{I_{ss}}{2}} = R g_m$.

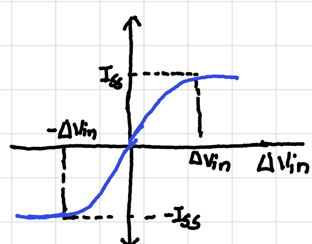
* Gain is zero when $\Delta V_{in} = \sqrt{\frac{2 I_{ss}}{\mu_n C_{ox} W/L}}$

* As we increase $|V_{in_1} - V_{in_2}|$ one of the transistor will go off other will draw all the current I_{ss}. $\therefore$ the maximum ΔV_{in} change. is

$$\Delta V_{in_1} = \sqrt{\frac{2 I_{ss}}{\mu_n C_{ox} W/L}}.$$







Small signal Analysis.

let us ground V_{in2} & find the effect of V_{in1} on V_{out1} & V_{out2}.

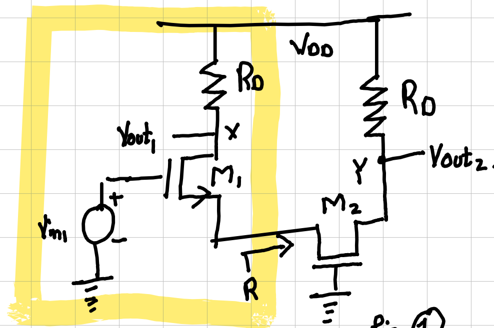


fig ①.

* from fig 2 we can see the. output V_x can be found by considering it as Common Source amplifier

$$\frac{V_x}{V_{in}} = \frac{-R_D}{1/g_{m2} + 1/g_{m1}} \quad ①$$

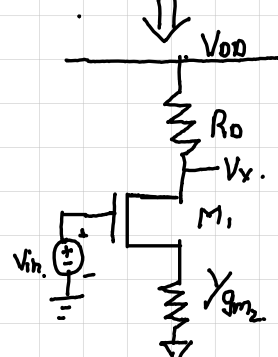


fig ②

* The circuit in the yellow box in fig 1 is an Source follower circuit which. can be modelled into Thevenin voltage of Vin with series with resistor of $1/g_{m1}$ as shown in figure 3 yellow box. and the circuit will behave as the. common gate amplifier

$$\therefore \frac{V_Y}{V_{in1}} = \frac{+R_D}{1/g_{m1} + 1/g_{m2}} \quad ②$$

+

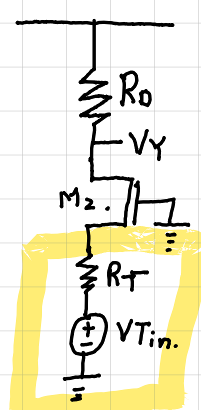


fig ③

subtrating 2 from 1.

$$\left.\frac{V_x - V_Y}{V_{in1}}\right|_{V_{in2}=0} = \frac{-2R_D}{1/g_{m1} + 1/g_{m2}}.$$

due to symetry. V_{in2} when $V_{in1}=0$ is same as above out put is superposition of both.

$$V_x - V_Y = \frac{-2R_D}{1/g_{m1} + 1/g_{m2}}\left[V_{in1} - V_{in2}\right]$$

We know that $g_{m_1} = g_{m_2} = g_m$. when both transistor are matched

$$V_X - V_Y = -g_m R_D \left[V_{in_1} - V_{in_2} \right]$$

Lemma I :- Consider a symetric circult where D_1 is symetric to D_2 and both are linear if we apply differentical signal to both the input the node P voltage is constant. for ac Analysis we can assume the node is at Virtual ground. as shown in figure 1-b.

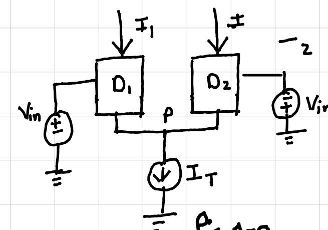


fig 1-a

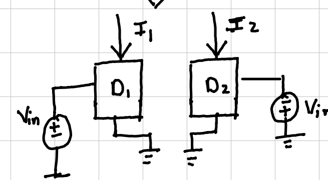


fig 1-b

Lemma II :- Consider a symetric circult where D_1 is symatric to D_2 and both are linear if we apply common mode signal to both the input. there is no current in Node P we can consider the circult is open at P. which is shown in figure 2-b.

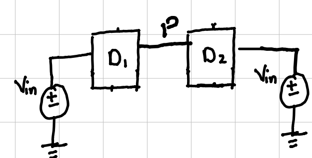


fig 2-a.

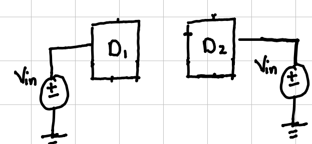


fig 2-b.

Degenerated Differential pair.

* this circuit make output more linearize.

* $\text{gain} = \dfrac{R_D}{1/g_m + R_s}$

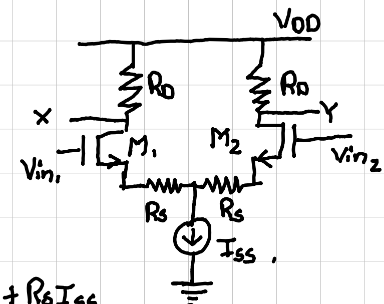


fig 1

* Maximum input range $= V_{in_1} - V_{in_2} = \sqrt{\dfrac{2I_{ss}}{\mu_n C_{ox} W/L}} + R_s I_{ss}$

* The gain of the circuit is reduced. It has less head room since there is drop $(I_{ss}/2)R_s$ in resistor. and gain is independent of g_m.)

* The head room can be increased. in the figure 2 where. there is No current 2R when V_{in_1} & V_{in_2} are Equal so the drop across 2R is zero. there will be drop onely due to differential signal.

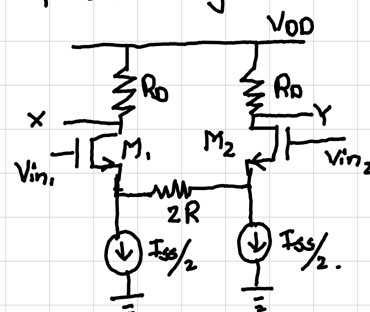
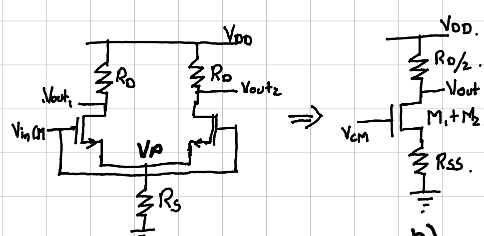


fig ②

Comman mode response

* Ideally Comman mode responce should not effect the output responce. but due difference. in g_m of both the transistor or finite resistance of current mirror. fraction of CM Voltage will appear at the output.



a). fig 3

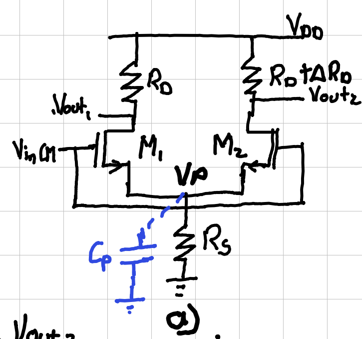
* let us assume the circuit is symetric & has finite R_S as shown in the figure. 3-b. if V_{cm} is increased V_X & V_Y decrease due to increase in current. which will change the small signal gain and. the output swing the common signal gain is given by.

$$A_{CM} = \frac{V_{out\,cm}}{V_{in\,cm}} = \frac{R_D/2}{1/2g_m + R_S}$$

* let us study the mismatch of R_D on the output of the circuit.

V_P act as a source fallower the change in V_P is given by

$$\Delta V_P = \frac{2R_S}{1/g_m + 2R_S} V_{in\,cm}.$$



M_1 & M_2 act as common source with source degenerative when output is taken at V_{out1} & V_{out2}.

$$\Delta V_{out1} = -\Delta V_{cm} \frac{R_D}{1/g_m + 2R_S}$$

$$\Delta V_{out2} = -\Delta V_{cm} \frac{R_D + \Delta R_D}{1/g_m + 2R_S}$$

* If the common mode noise for higher frequency input. due to the parasatic capacitance [C_P] of current mirror will be high at output is high due to the low impedence path created by cap

The Effect of Mismatch of transconductance on the output.

* The mismatch is mainly due the variation in Length, width, or V_T of the mosfet the current in the Each Mos fet is given by

$$I_{D1} = g_{m1}(V_{incm} - V_P) \quad \& \quad I_{D2} = g_{m2}(V_{incm} - V_P), \quad (I_{D1} + I_{D2})R_S = V_P$$

$$\therefore (g_{m1} + g_{m2})(V_{incm} - V_P)R_{SS} = V_P$$

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in\,cm}.$$

Output Voltage is given by

$$V_X = -g_{m1}(V_{cm} - V_P)R_D$$

$$V_X = \frac{-g_{m1} \times R_D\, V_{incm}}{(g_{m1} + g_{m2})R_{SS} + 1}, \quad \& \quad V_Y = \frac{-g_{m2}\, R_D}{(g_{m1} + g_{m2})R_{SS} + 1} V_{incm}.$$

$$V_X - V_Y = \frac{-[g_{m1} - g_{m2}]R_D\, V_{incm}}{(g_{m1} + g_{m2})R_{SS} + 1}. = \frac{-\Delta g_m R_D\, V_{incm}}{(g_{m1} + g_{m2})R_{SS} + 1}.$$

* Comman Mode rejection ratio :- It is the ratio of differential gain with the comman mode gain. for ideal op-amp CMRR will be ∞

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

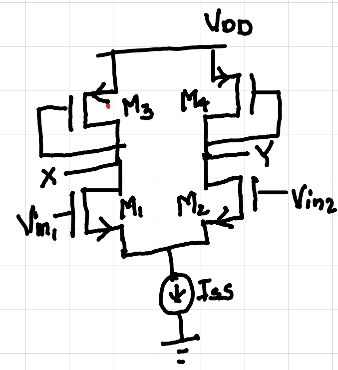
* differential gain. of Amplifier with different gm is

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}.$$

$$\therefore \quad CMRR = \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{2 \Delta g_m}.$$

$$\approx \frac{g_m (1 + 2 g_m R_{SS})}{\Delta g_m}. \quad \text{where } g_m = \frac{g_{m1} + g_{m2}}{2}.$$

Differential pair with mos load.



* The gain of the following circuit is

$$A_v = -g_{m1} \left[\frac{1}{g_{m3}} \| r_{o3} \| r_{o1} \right]$$

$$\approx \frac{-g_{m1}}{g_{m3}}$$