trivalent inpurities -> boron, gallium, indium, aluminum.

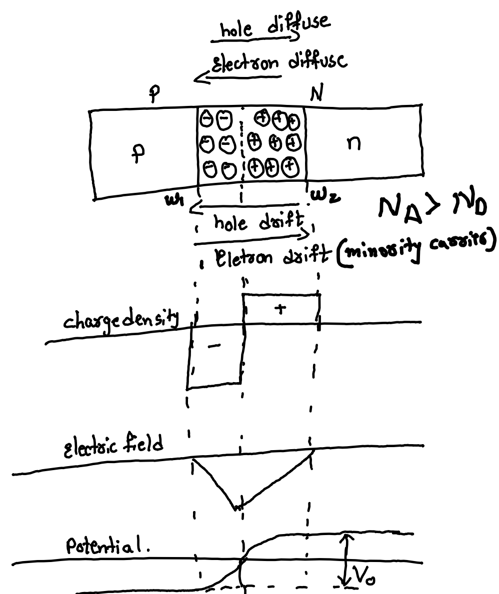
Pentavalent inpurities :- Arsenic, phosphorous, Antimony

-> the graient of charge concentration, in p & n type material help to diffuse the hole and electron.

-> there is built in potential in the diode from n to p due to the depletion region.

-> Under Equlibrium diffusion current setup electric field which lead to the drift current in apposite direction.

-> the p-side is doped more than the n side the charge density in p side is more than the n type.



-> the built in potential is given by formula

$$V_0 = V_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$V_T = \frac{KT}{q} = 26mV$$

$$n_i = 1.5 \times 10^{10} \text{ at } 300k.$$

-> In forward bias the diffusion current is more than drift current

-> In reverse bias the drift current is more than diffusion current. there are less minority carrier for drift current in reverse bias.

→ the diode Equation is given by the formula

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$$

→ I_S depends on → area of diode, → doping concentration.

* first order model of diode

$I = I_S\left(e^{\frac{V_D}{V_T}} - 1\right)$

→ Depletion region charge(Q) → $A_D\sqrt{2\,\varepsilon_{si}\,q\,\frac{N_A N_D}{N_A + N_D}\left(V_0 - V_D\right)}$ → Voltage of diode

→ Depletion region width. $W_2 - W_1 \rightarrow \sqrt{\frac{2\varepsilon_{si}}{q}\,\frac{N_A + N_D}{N_A N_D}\left(V_0 - V_D\right)}$

→ electric field$(E_j) = \sqrt{\frac{2q}{\varepsilon_{si}}\,\frac{N_A N_D}{N_A + N_D}\left(V_0 - V_D\right)}$ V_0 → Voltage across depletion layer.

→ $\varepsilon_{si} = 11.5 \times \varepsilon_0$

→ $\frac{W_2}{-W_1} = \frac{N_A}{N_D}$ W_2 → width of n type, W_1 → width of p type.

→ Junction capacitance $(C_j) \rightarrow A_D\sqrt{\frac{\varepsilon_{si}\,q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\left(V_0 - V_D\right)^{-1}}$

→ $C_j = \frac{C_{jo}}{\left(1 - V_D/V_0\right)^m}$ C_{jo} → capacitance under zero bias

→ m → grading constant $m = $ ½ → abrupt diode, ⅓ → linear or graded diode.

→ $C_{jo} = A_D\sqrt{\frac{\varepsilon_{si}}{2}\,q\,\frac{N_A N_D}{N_A + N_D}\,V_0^{-1}}$

A_D → Area of diode.

→ Equation C_j is valid for abrupt diode. where transition from p to N material is instantanously

Large Signal depletion-region Capacitance

-> junction capacitance is Voltage dependent

-> In digital circult voltage is moved rapidly wide range under this circumstance it is attractive to replace Voltage dependent non-linear C_j with. linear capacitance C_{eq}

$$C_{eq} = \frac{Q_i}{V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} \times C_{j0}$$

Temprature dependence of diode.

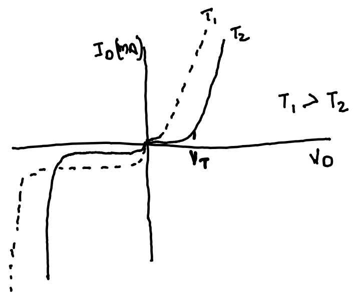
-> the break down Voltage increase with temprature

-> the reverse saturation current double for every 10°c increase in temprature

$$I_s(T_2) = I_o(T_1) \times 2^{(T_2 - T_1)/10}$$

-> cut in Voltage (V_T) decrease with Increase in temprature.

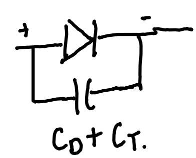
$$\frac{dV}{dT} = -2.5\, mV/°C$$



* diode capacitance.

Transition capacitance C_T

-> during forward bias width decrease & C_T increase & converse is true for reverse biased.



Diffusion capacitance.

-> Diffusion capacitance is predominant in forward bias.

-> Diffusion capacitance is with change

-> $C_D = \frac{dq}{dV}$ -> the change in the number of minority carrier with change in the voltage.

-> it is in the range of 10-20uF in forword bias

-> It effect the switching time of the diode the switching time constant of the diode equal to $r_d \times C_D$. where r_d is dynamic forward resistance

Mosfet

- → Consider $V_{GS}=0$ & $V_S=0$ $V_D=0$ $V_B=0$. It can be modelled as connection of two diode back to back. these act as Extremely high resistance between source to drain
- → the positive voltage is applied to gate with respective Body. this act as Parallel plate capacitor
- → the positive charge on the gate repell the holes in the body which create the depletion region.
- → the width of depletion region $W_d=\sqrt{\frac{2\epsilon_{si}V_0}{qN_A}}$ N_A → Substrate doping
- → the charge on depletion layer $Q_d=\sqrt{2qN_A\epsilon_{si}V_0}$ V_0 → Voltage of depletion region.
- → As the gate voltage is increase, the potential on the silicon surface reach. Critial value. It is inverted to n type material. this is called strong inversion. it accours at a voltage Equal to twice the fermi potential.

$$V_F=-V_T\ln\left(\frac{N_A}{n_i}\right)$$

- → further increase in Voltage doesn't increase the depletion reagion but it increase the current in depletion region.
- → In strong inversion the charge stored is given by formula.

$$Q_{B0}=\sqrt{2qN_A\epsilon_{si}(|-2V_F+V_{SB}|)}$$ V_{SB} → Voltage across Source Body

- → The value of V_{GS} where strong inversion occur is called V_T
- → V_T is is function of
  - ↳ difference in work function between gate & substrate
  - ↳ oxide thickness, Inpurities trapped between channel & gate oxide
  - ↳ fermi voltage

V_F → surface potential

$$V_T=V_{T0}+\gamma\left(\sqrt{|-2V_F+V_{SB}|}-\sqrt{|-2V_F|}\right)$$

V_{T0} ⇒ V_T for $V_{SB}=0$

γ ⇒ Body effect co-efficient.