Analog Electronics

-the level of abstraction of knowlage required to study analog design is Quantum physics -> Solid state physics -> Semiconduc tox device physics -> device modelling -> design of circults.

Mosfet as a switch is high -> the resistance Ros is low it -> if gate of 17-mas is low -> the resistance Ros is high it conducts Electricity → 9f gate of n-mas act as open cisult Mosfet stanchac LJzaun. Ldaawn - 2LD = LEFF * typical value for LEAF = 10 nm 4 tox = 15 Å * mosfet is symetoical device * the substrate should be reverse biased with respet to source of

Drain to prevent latch up

* Pmos is created by negating all the doping types

* Pmas is fabricated in an N-well of substrate is connected to highest Patential (von)

Masfet Symbol Pmos

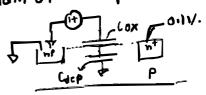
Mosfet V-I characteristics

->Thashold valtage (Vin)

* As Vg becomes more +ve the holes in the substrate [nmas] get repelled from the gate hence the depletion region is formed

* Increase Vq increase the width of the depletion region.

* the channel can be modeled as two cap connected in series with Voltage divided



* the value of vq the inversion of channel occurs is called UTH * if the value of liq is increased further the charge in depletion region demain constant. while the channel charge density continious to increase which increase ID

*
$$V_{TH} = \Phi_{M5} + 2\Phi_F + \frac{Q_{deP}}{Cox}$$

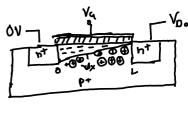
\$\pm_5 > difference between workfunction of polysitican 4 Silicon substrate.

* the Vin of the mosfet is adjusted by adding dopent to the channel area during fabrication



I-V characteristics of Mosfet * the charge per unit longth in mosfet is given Q(x) = · (ox W (V45-Vx-Vt) where Cox= Eo/tox

Id = QdXV where V -> Velocity of electron.



...
$$I_d = C_{ox} W \left(V_{qs} - V_x - V_t \right) V$$

we know that $V = U E + E = -\frac{dV}{dx}$

: Id = Cox W (Vgs-Vx-V4) u dv dx. $\int I_d dx = \int Cox W \left(V_{qs} - V_{xx} - V_t \right) u dV.$ * the current in the channel is constant

* the current in the Chamics

.: Id =
$$\cos \underline{\mathcal{U}} \text{ ul} \left(V_{qs} - V_t \right) V_{DS} - \frac{V_{DS}}{2}$$

* the peak current is when $V_{DS} = V_{qS} - V_t = \sum_{L} \left(V_{qS} - V_t \right) \frac{V_{DS}^2}{2}$

we call Ugs-YTH as overdrive voltage.

* Vos = Vqs-VTh -> triode region. * If Vas = Vqs-VTh then Id = Cox W uo (Vqs-Vt) Vas & Ron = 1 > Voltage controlled resistor

* the current becomes constant when
$$V_{DS} \geq V_{QS} - V_{Th}$$
 this region is called saturated region and the channel becomes pinched off. there will be current in the region after pinched off. due to the increase of Velocity of Electron in the pinched point. electron Simply shoot to the drain of the device

-> Heal amplifies y(t)= a. +a, x(t) -> sool amplifies ytt)=ao+a1xtt)+a2xtt)..... L> cause distostion -> Performance parameter: > Speed | > Noise | -> Speed | -> Apput ortput Impodence. | -> power dissipation. | -> working | > working c supply Amplifier, categories common gatestage Sover follower common source stage bossistive load Lowith residous load La resistive bias L> Custont - Source La Cuzzont-Source Ladiode Connect load load L> warent-source load bias 4 Active load L> source degenerative * Common Source with resistor load

coscode.

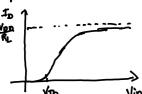
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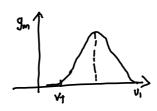
1> Folded

-> for triode region vout is

$$V_{out} = V_{DD} \times \frac{R_D}{R_L + R_0} = R_0 \Rightarrow H_{\chi}(O_{\chi} \frac{U}{L} (V_{\xi S} - V_T))$$

→ 9m change when we apply large signal i.e 9m depend on Vin.





To increase gain Increase

> #/ > It lead to increase in dexice capacitance. 4 Increase Vo which reduce the output swing (due to reduce in Ro due to increase in w) -> Vo constant In reduce -> Increase in Ro which lead to increase in output time constant.

> the channel length modulation become signifent when we increase RL.

$$A_{V} = -R_{L}g_{m} - \frac{R_{L}}{36}A_{V} \qquad |\forall \delta_{\delta} = |\xi/2(V_{GS} - V_{T})^{2}\lambda$$

-> diode connected mastel : if down is connected to gate.

-) If we neglect of since it is large the Equivalent resistance in

diade connect is gmtgmb

>:. the gain of diode connect is Av=-9mRD

+ is
$$A_V = g_m R_D$$

= $-g_{m_1} \times \frac{1}{g_{m_2} + g_{mb_2}}$.

$$= \frac{9m_1}{9m_2} \times \frac{1}{1 + 9mb_2} = \frac{-9m_1}{9m_2} \times \frac{1}{1 + n} = \frac{9mb_2}{9m_2}$$

$$\frac{3m_{2}}{\sqrt{2}} \frac{3m_{2}}{\sqrt{2}} I_{O_{1}} u_{1} I_{O_{1}} \times \frac{1}{1+n} I_{O_{1}} = I$$

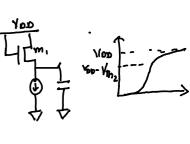
$$= \frac{\sqrt{\omega_{1}/L_{1}}}{\sqrt{\omega_{2}/L_{2}}} \times \frac{1}{1+n}$$

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-> If n is neglected bias is independent of bias current or Voltage there fore it is linear

if mosfet 1 is off Ip is zero the voltage will go to UDD. during this time it will reach.

VDD-UTA, fast then transistor turns off then it will go to UDD slowly due to reverse bias arrent. For high speed application we can consider it will reach VDD-VTAz.



 \Rightarrow gain is weak function of dimention we need to rise $\frac{\omega_{1/2}}{L_1}/W_{2/2}$ to 25 to get gain of 5.

→ In consent technology channel length modulation is quite signifient which can't be ignored

* common source with. Current source load.

* Common Source with active load.

L>bias Voltage ave dependent on PUT. if there > Assue with this configuration

* common source in triode region.

> draw back -> R depends on PUT like V7, W/L, Cox which is difficult to control & change with tempsature.

> 9m is function of Vas degenorative is used to make gain as weak function of Vin.

VUL Win I MI Rs (400) 9 Vin => 3 18 x 3vin.

$$V_{qs} = V_{in} - I_0 R_s \implies \frac{\partial V_{qs}}{\partial V_{in}} = 1 - \frac{\partial I_0}{\partial V_{in}} R_s.$$

$$\Rightarrow \frac{\partial I_0}{\partial V_{qs}} \times \frac{\partial V_{qs}}{\partial V_{in}} = \frac{\partial I_0}{\partial V_{qs}} \left(1 - \frac{\partial I_0}{\partial V_{in}} R_s\right).$$

$$\Rightarrow V_{m(New)} = g_{m(new)} \left(1 - V_{m(new)} R_s\right).$$

$$\Rightarrow V_{m(new)} = \frac{g_{m(new)}}{1 + g_{m(new)}} = \frac{g_{m(new)}}{1 + g_{m(new)}} R_s.$$

$$\Rightarrow \frac{g_{m} \times R_0}{1 + g_{m} R_s} \Rightarrow \text{Negliching body effect.}$$

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$$\Rightarrow \text{He disamback of this circuit is it sendice the gain of the circuit.}$$

$$\Rightarrow \text{With body effect gain changes to}$$

$$I_{in} = g_{m}V_{1} - g_{mb}V_{2} - I_{4n}R_{s}$$

$$V_{in} = \frac{g_{m}V_{0}}{g_{s}+[1+(g_{m}+g_{m})_{0}R_{s}]} X_{0}$$

Source fallower amplifices > If act as a Voltage buffled > If act as a Voltage out to > I uo (ox [] (Vm-Vost-Vrn) = Voot. () Vm-I - Voot > differentiating with respect to Vin 1 do Cox W 2 (Vin-Vort - 1/Th) Rs (1-drot - JVn) = dvort - Vin avin = dvort dVrn => dVrn × dVsB VsB. = + Vovt dVrh = M dVrn dVrn dVsB => dvort = Av = uo ax w (vin-4th - vort) Rs 1+ un cox [(Vin-VIH - Vort) Rs (1+ h => gm = Un Cox W/ (Vin- Vm - Novt) -> by difference tion of 1. 1 V4s = Vin- Vrn.
1 2 V4s = -1. .. 9mxn = \frac{40}{\frac{1}{45}} \times \frac{2\frac{1}{2}\frac{1} $Av = \frac{g_m R_5}{1 + g_m R_5 (1+h)}$ 390 = -18-9mb=9mb $A v = \frac{g_m Rs}{1 + (g_m + g_m b) Rs}$ > Even Ry>=> the gain of amplifies is always less than 1 . i.e gm => if Vas is increased by the factor JZ current in resistor increase by the factor of 2 this causes Non-linearity to sesdue this the sesistor is seplaced by constant Cussent Source . which is in saturation. Yout = Int 9mb Au = 9m 9m + 9mh