Design and Implementation of Analog Circuits and Systems

Design specification of building blocks and verifcation plan

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1 ADC Function Description

The Analog-to-Digital Converter (ADC) function described below performs the continuous conversion of a differential input voltage ($V_{\text{in}_p} - V_{\text{in}_n}$) with respect to a differential reference voltage ($V_{\text{ref}_p} - V_{\text{ref}_n}$) into a digital sign/magnitude bus. The conversion is executed at a constant sample rate using a dual-slope integrating function to achieve the best possible conversion time.

1.1 Parameters

- Supply voltage: $V_{\text{dd}} = 1.2\,\text{V}$
- Common mode voltage: $V_{\text{cm}} = 0.75\,\text{V}$
- Reference voltages: $V_{\text{ref}_p} = 1\,\text{V}$, $V_{\text{ref}_n} = 0.5\,\text{V}$
- Digital input clock: 50 MHz
- Full-Scale Range (FSR):
  - $V_{\text{in}_{\text{max}p}} = V_{\text{in}_{\text{max}n}} = 1\,\text{V}$
  - $V_{\text{in}_{\text{min}p}} = V_{\text{in}_{\text{min}n}} = 0.5\,\text{V}$ (absolute)
  - $V_{\text{in}_p} = V_{\text{in}_n} = \pm 0.25\,\text{V}$ (relative to V_{cm})
  - $V_{\text{in}_{\text{pp, single\_ended}}} = 0.5\,\text{V}$, $V_{\text{in}_{\text{pp, differential}}} = 1.0\,\text{V}$ (dynamic range, with respect to V_{cm})
- Output code: 11 bits (using sign/magnitude format)
- Output clock: Signaling a new sample available with a constant period expected
- Conversion time: Better than 2500 input clock cycles ($< 50\,\mu\text{s}$) leading to at least 20 kS/s sample rate
- Total Unadjusted Error (TUE): ±1 LSB typical is possible, aiming for less than ±3 LSB

2 Design specification of building blocks and verification plan:

2.1 Transfer Switch Model

The functionality of the dual-slope ADC relies significantly on its switches, as they play a crucial role in controlling the charging and discharging of the integrating capacitor throughout the conversion process. This ADC design employs four key switches:

1. S1: This switch establishes a connection between the analog input and the integrating capacitor during the charging phase, and it disconnects this connection during the conversion phase.

2. S2a and S2b: In the discharging phase, these switches link the integrating capacitor to the reference voltage.

3. S3: Prior to the initiation of a new conversion cycle, this switch resets or discharges the integrating capacitor.

This switch is designed to operate as a transfer gate, featuring a parallel configuration of nch mac and pch mac, with an inverter facilitating simultaneous activation for both enable and enable' which is directly chosen from the technology library. The schematic presented below depicts the configuration of the T-gate that has been established.

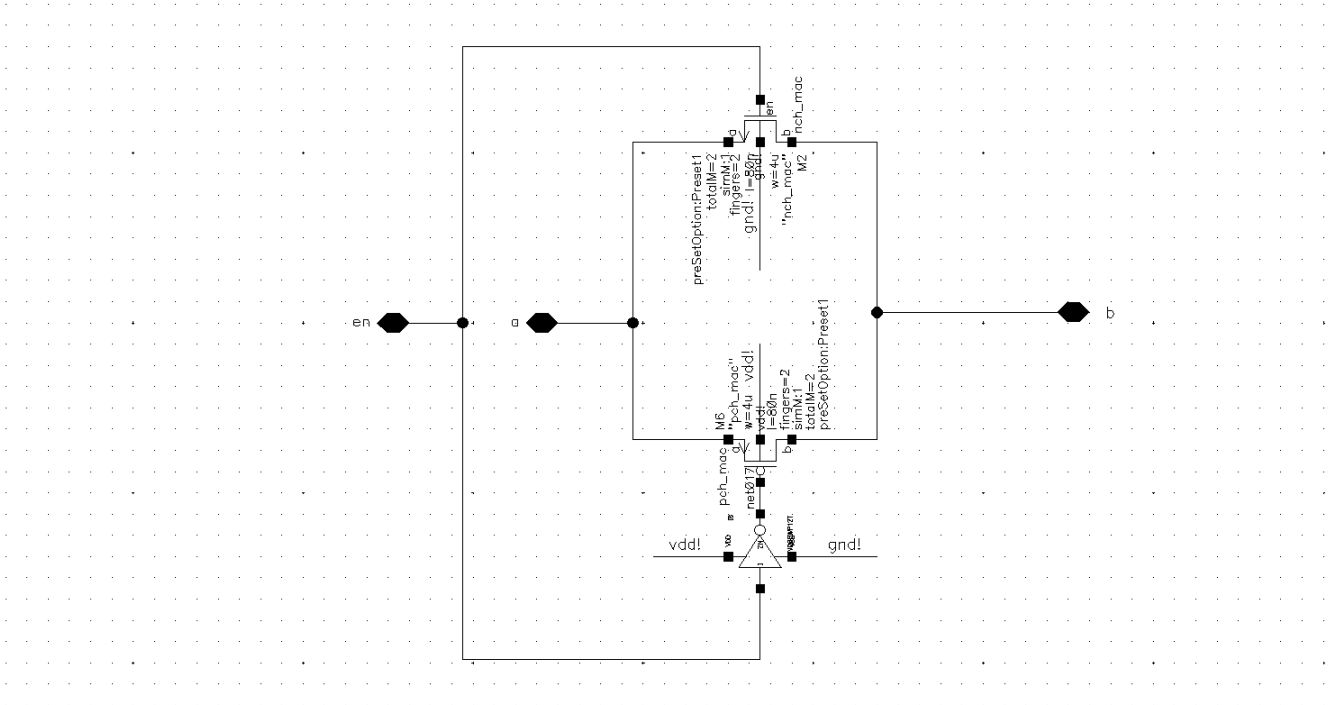

Figure 1: Schematic of the transmission gate.

By supplying the switch's En pin with a voltage device, the testbench is arranged according to the configuration outlined below for assessing the switch's resistance.

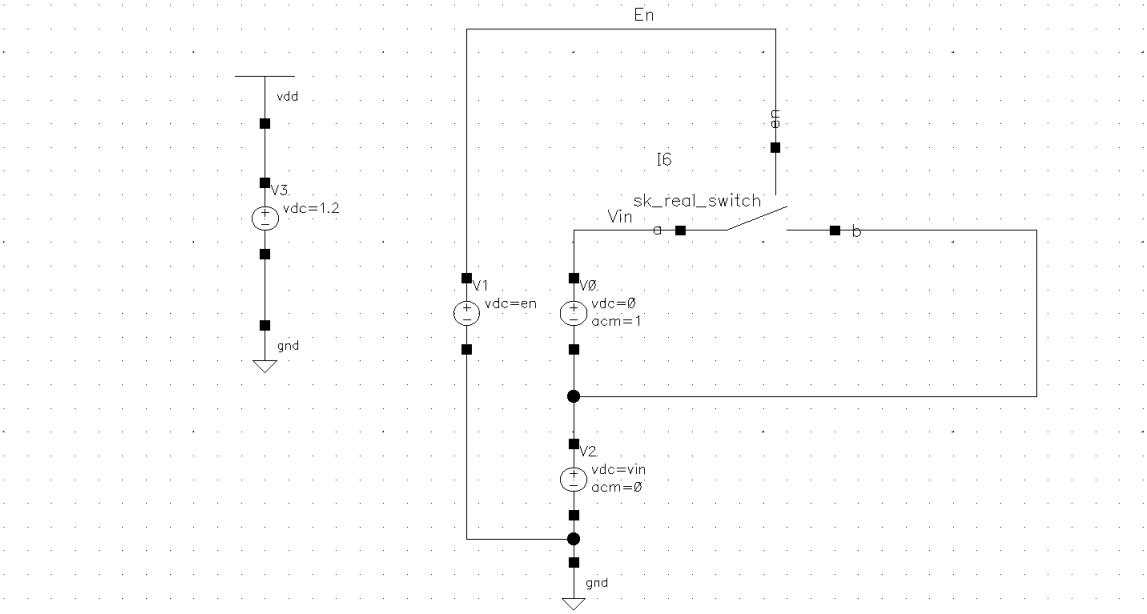

Figure 2: Test bench setup of transmission gate.

To assess the on resistance (Ron) of the designed switch, an AC analysis was configured and executed. The switch's input was subjected to an AC magnitude of 1V, which was then shorted with a DC voltage which was swept from 0V to 1.2V. The on-resistance (Ron) was determined graphically by calculating it as the reciprocal of the current through the input pin of the switch.
For the set (W/L) ratio's of the PMOS and NMOS transistors, the maximum achievable on resistance (Ron) was achieved to be 1.05K Ohm.

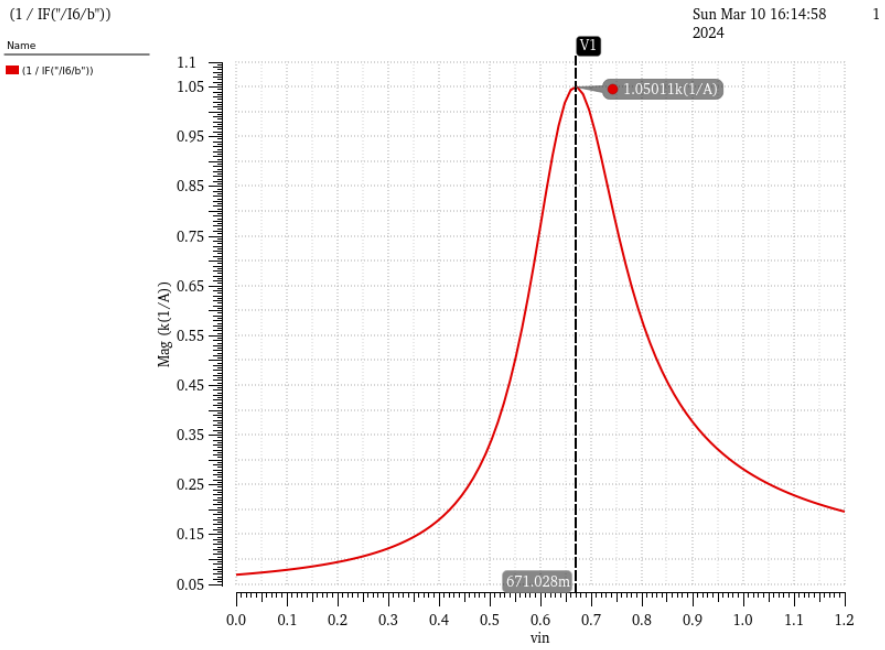

Figure 3: On Resistance of the designed T-gate.

To calculate the off resistance (Roff) of the designed switch, the same above mentioned AC analysis was swept with the enable voltage set to 0V.

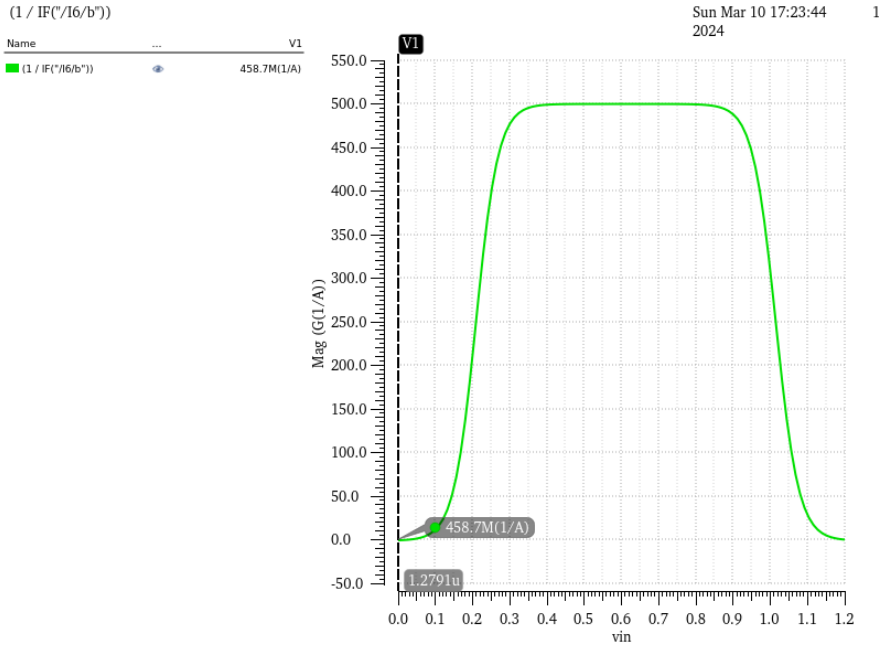

Figure 4: Off Resistance of the designed T-gate.

Table 1: Error Criteria for Switch On Resistance.

Error Type	Ideal Ron LSB Change	Ron to be maintained
NO error	$\pm <$ 2.2K Ohm	as low as possible
$\pm$1 LSB error	$\pm$4.2K Ohm	as low as Possible

Table 2: Error Criteria for Switch Off Resistance.

Error Type	Ideal Roff LSB Change	Roff to be maintained
NO error	$\pm <$1.5G Ohm	as high as possible
$\pm$1 LSB error	$\pm$4.5G Ohm	as high as Possible

2.2 Opamp Model:-

In this phase, Opamp will perform the Integration and Measurement Phase(De-integration phase) when Vin is connected for a fixed time T1. A capacitance is charged by current during a predetermined period, producing an output voltage $V_{out,int}$. The input voltage value will determine the slope of the capacitor's charge.The time duration of this phase is given as:

$$T1 = T_{\text{clk}} \times 2^N = \frac{1}{f_{\text{clk}}} \times 2^N = \frac{1}{50\,\text{MHz}} \times 2^{10} = 20.48\,\mu\text{s}$$

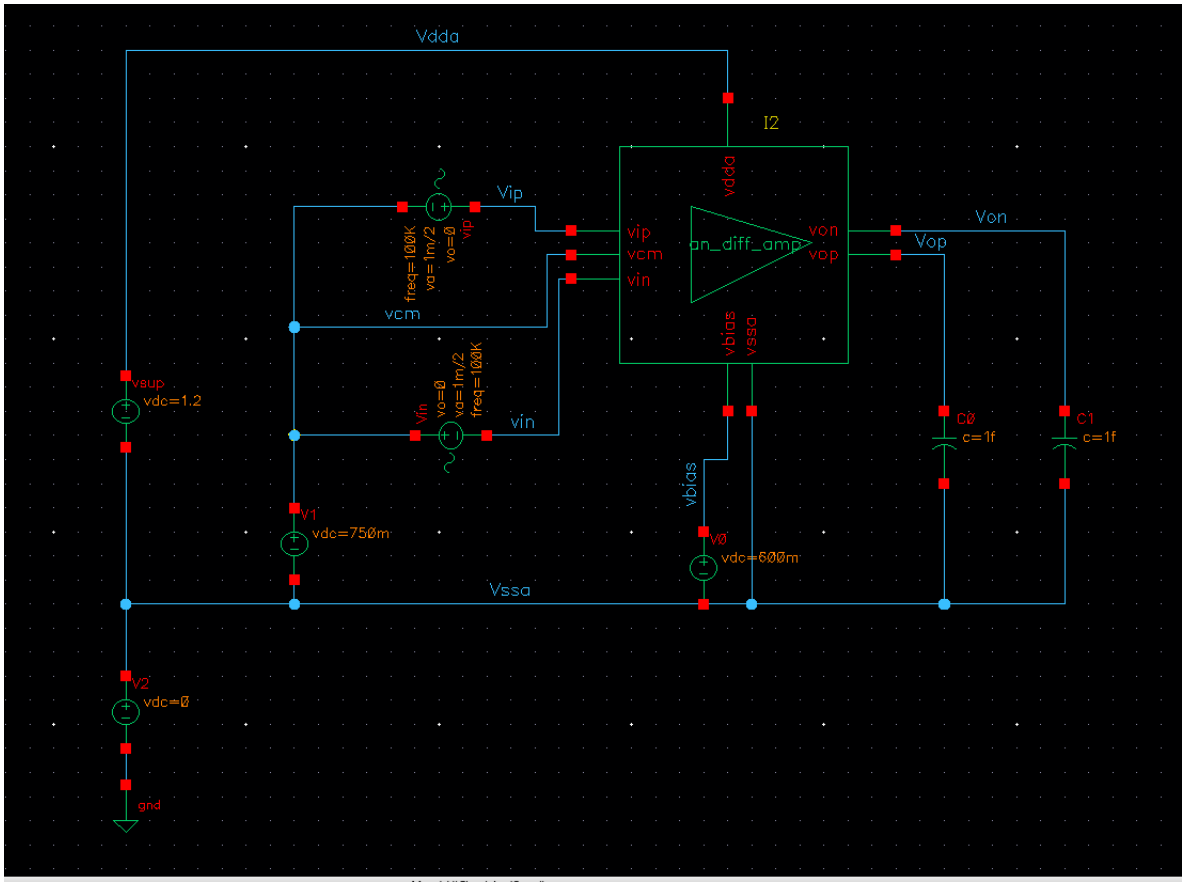

Figure 5: Test bench setup for Ideal Opamp Model

The test bench setup for the Opamp model, as depicted in Figure 5, has been proven effective for ideal elements across various simulations. Therefore, it will be utilized again for the same purpose, maintaining consistency and efficiency.

Transient analysis will be performed on the Integrator using the current test bench configuration. The focus will be on examining parameters such as VCM, VIP, and VIN to validate the functionality of the inputs, as well as monitoring the outputs VON and VOP.

Integrator **DC analysis** will be conducted to assess the circuit's offset by adjusting the design variables in the input VIP and VIN. This analysis involves plotting VOP and VON to identify the DC crossing point at zero. Additionally, the offset can be evaluated by

plotting the output DC voltage (VOP - VON) and measuring the offset at 0 DC voltage.

Integrator **AC analysis** will be performed to determine the circuit's cutoff frequency by plotting the difference in output voltage (VOP - VON) in decibels (dB).

Corner and Monte Carlo Simulations:-
The corner and Monte Carlo Simulations will be done for Integrator, Offset and Gain across the various corners at different temperatures (30 ∘ C, 27 ∘ C, 80 ∘ C) and voltages (1.02V,1.2V, 1.32V).

-The expressions that will be used to perform the corner and Monte Carlo simulations are:
Output Gain in dB = value(dB20((VF("/Vop") - VF("/Von"))) ymax(dB20((VF("/Vop") - VF("/Von")))) ?period nil ?xName "time")

Output Offset = cross((v("/Vop" ?result "dc") - v("/Von" ?result "dc")) (ymax((v("/Vop" ?result "dc") - v("/Von" ?result "dc"))) - 1.2) 1 "either" nil nil nil)

Cutofff requency = cross(dB20((V F ("/V op")V F ("/V on")))(ymax(dB20((V F ("/V op") V F ("/V on")))) 3)1"either"nilnilnil)

2.3 Comparator Model:-

In a dual-slope ADC, the comparator plays a key role in detecting when the output voltage of the integrator reaches a predefined reference level, marking the end of the integration phase. It's essential to note that the comparator may need to handle signals near the zero-volt reference level. Hence, it's crucial for a differential comparator to effectively compare small voltage differences with reliability.

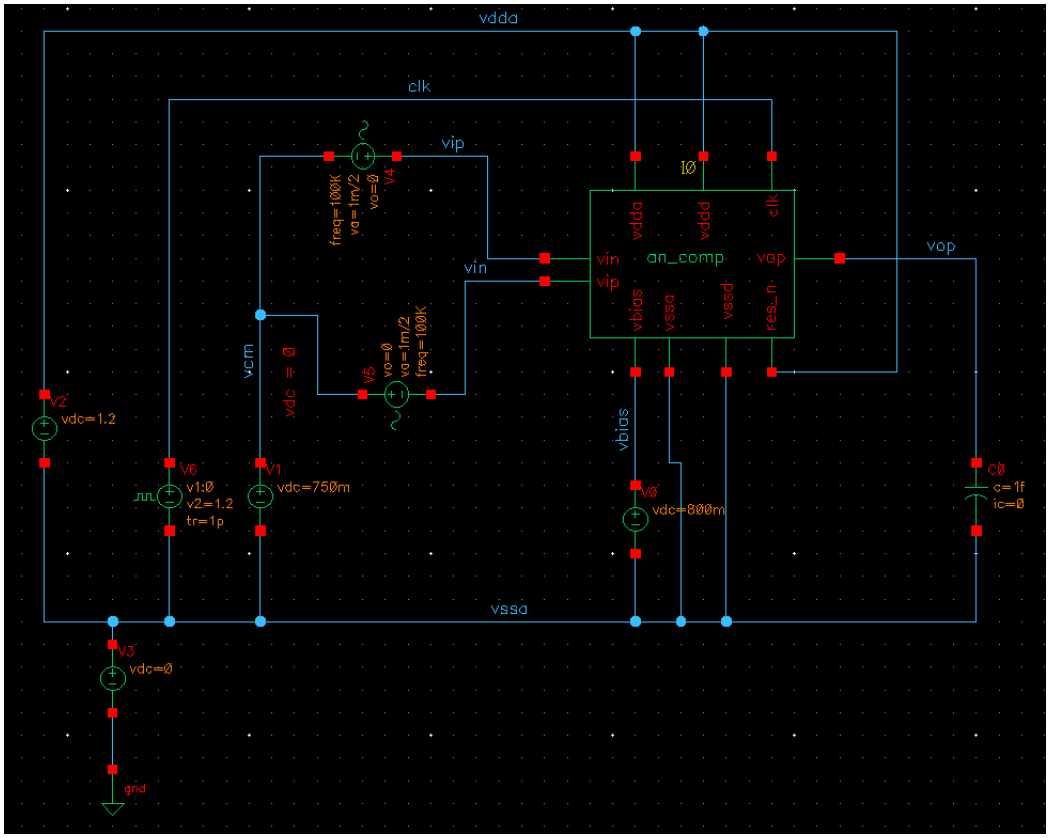

Figure 6: Test bench setup of ideal Comparator

The test bench setup utilized to evaluate ideal comparator elements can also be employed to assess the comparator itself as it can be seen in figure 6.

Transient analysis has been simulated using the test-bench above, where the output voltage (VOP) is plotted to observe the response of the comparator in order to verify the delay which can be verified by providing an input which is switching fast and then checking on how long it takes to reflect the output.
DC analysis was performed to quantify the comparator's offset at the zero crossing point, accomplished by measuring the time it takes to reach its maximum value. The offset can be determined by plotting the output voltage (VOP).

Corner and Monte Carlo Simulations:- During the corner simulation encompassing the offset of the comparator across various corners at different temperatures (30∘C, 27∘C, 80∘C) and voltages (1.02V, 1.2V,1.32V).

Expression to determine offset of the comparator by Monte Carlo Simulation is as shown:-
cross(v("/I0/net19"?result"dc")(ymax(v("/I0/net19"?result"dc"))0.6)1"either"nilnilnil)

2.4 Top level ADC model :-

The testbench of the top-level ADC has been set up and shown below.

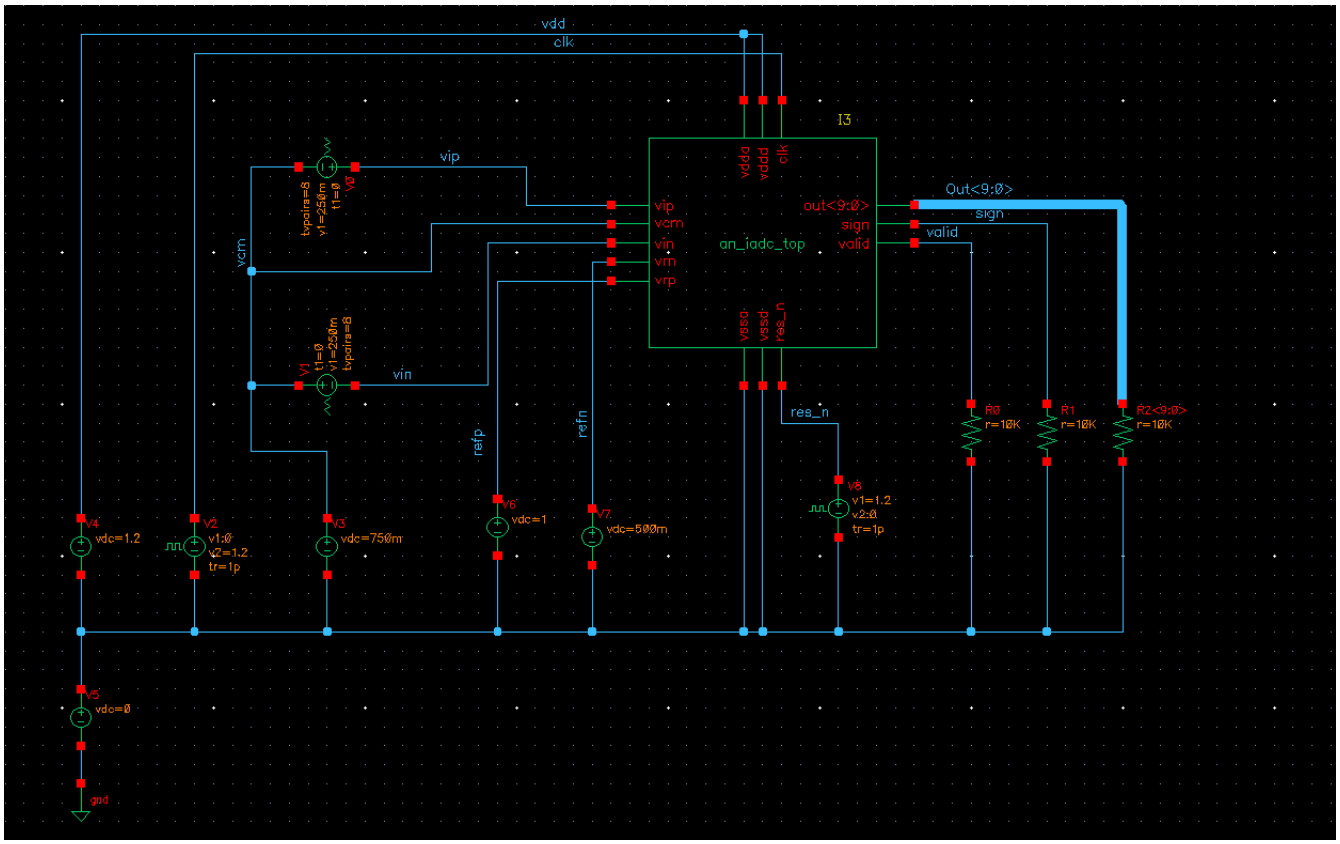

Figure 7: Test bench setup for top model ADC

The identical test bench can be repurposed for evaluating the top-level ADC model. Transient analysis serves as an initial step to observe outputs across various stages.

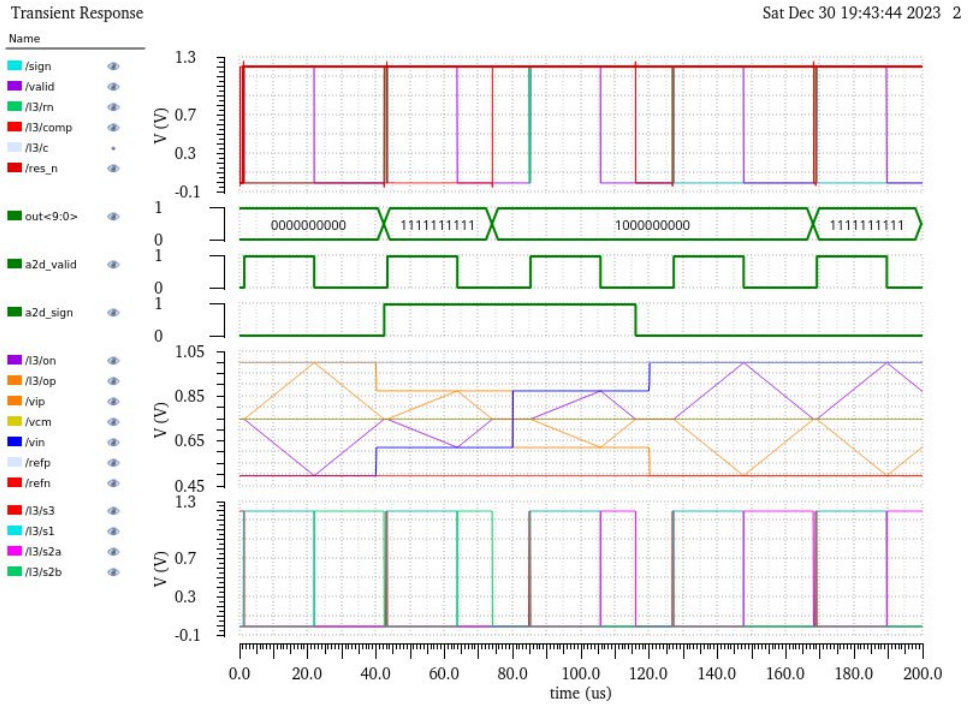

Figure 8: iADC transient behaviour.

Table 3: Block Pinouts of the top-level ADC.

Pin	**Direction Type**	**Function of the Pin**
V_{in_p}	Input	Input to the Opamp.
V_{in_n}	Input	Input to the Opamp.
V_{cm}	Input	Vcm of the Opamp.
V_{rp}	Input	Reference input voltage to the Opamp.
V_{rn}	Input	Reference input voltage to the Opamp.
V_{rn}	Input	Reference input voltage to the Opamp.
V_{out_p}	Output	Output of the Opamp.
V_{out_n}	Output	Output of the Opamp.
V_{op}	Output	Output of differential comparator.
Clk	Input	Clock input provided to the digital unit
res_n	Control	Resets the comparator's output to initial conditions.
V_{dda}	Power	Supply reference pin.
V_{ssa}	Power	Ground reference pin.
V_{bias}	Power	Sets up DC operating point of the comparator.
$comp_{clk}$	Input	Input of the digital control unit from the clock of the comparator.
$comp_{res\_n}$	Control	Reset of the digital control unit from the comparator's reset.
$S1$	Input	Switch to turn on during the integration.
$S2a$	Input	Switch to turn on during the de-integration when V_r is positive.
$S2b$	Input	Switch to turn on during the de-integration when V_r is negative.
$S3$	Input	Reset.
$Sign$	Input	Indicates whether the output is positive or negative.
$out < 9:0 >$	Output	Gives the digital 10-bit output data bus.

2.1 Behavior of the ADC Top Model with Ideal Op-Amp Gain, Offset, and Comparator Offset

-Op-Amp Gain:-

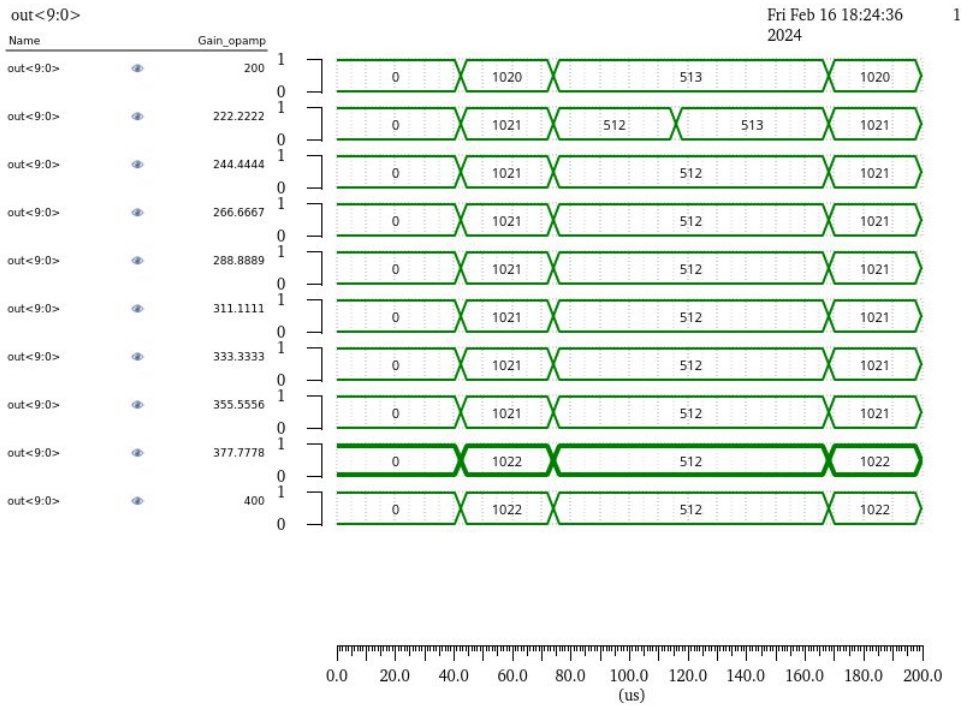

Figure 9: Op-Amp Gain variation in the Top Model ADC

-By adjusting the op-amp gain, it's noticeable that up to a gain of 1300, the digital data bus output exhibits no errors ideally, with values of 1023 and 512 for ±FSR and ±FSR/2, respectively. However, from a gain of 1300 down to 380, there is a single LSB error in the output data. Given that a single LSB error is negligible in an ideal ADC output, the ADC model is configured with a gain of 380.

Table 4: Error Criteria for Gain

Error Type	Ideal_Gain	Integrator_Gain
NO error	1.3K	as high as possible
±1 LSB error	380	as high as possible

Op-Amp Offset:- -Adjusting the Opamp offset within the range of $-0.1\,\text{mV}$ to $+0.09\,\text{mV}$ introduces an error of up to 1 LSB in the output data bus. Beyond this range, the error increases to around ±20. However, below this threshold, there is no observable error in the output data bus.

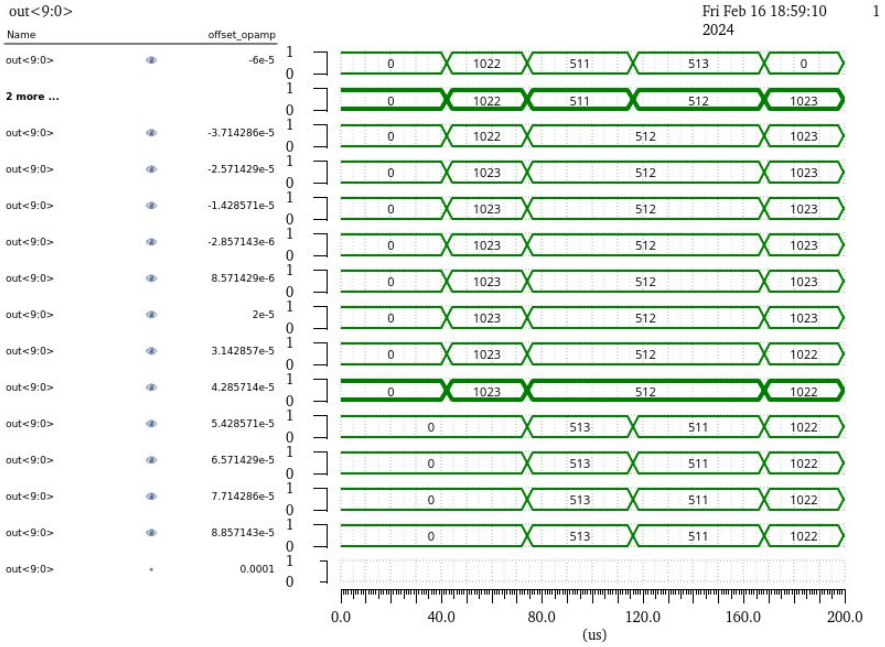

Figure 10: Op-Amp Offset variation in the Top Model ADC

Table 5: Error Criteria for Offset

Error Type	Ideal_Offset	Integrator_Offset
NO error	± <0.1mV	as Low as possible
±1 LSB error	±0.1mV	as Low as Possible

Comparator Offset:-

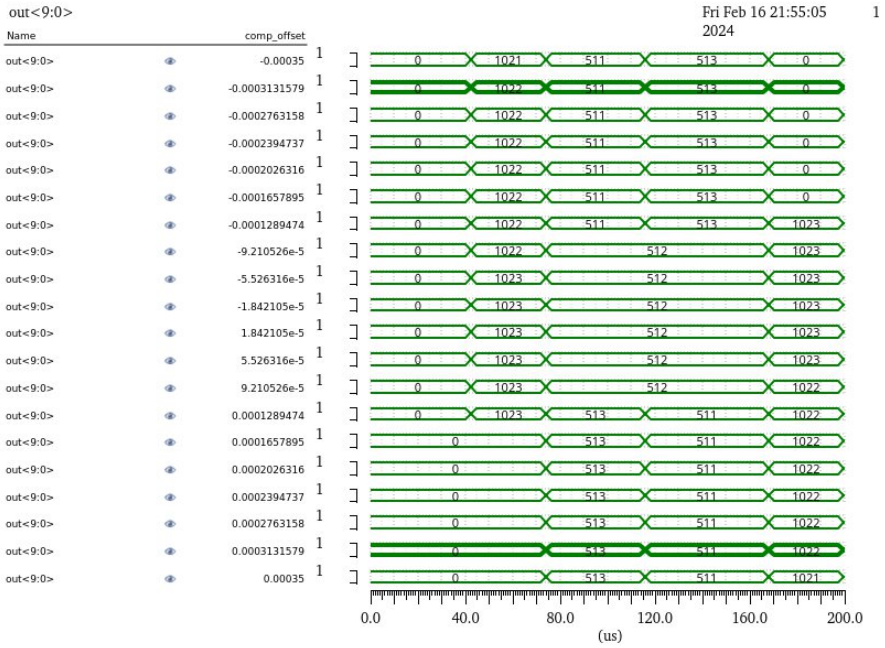

Figure 11: Comparator Offset variation in the Top Model ADC

-When adjusting the comparator offset within the range of ±0.64 mV, an error of up to 1 LSB is observed in the output digital bus. If the offset exceeds this range, the error increases to 2 LSB. Thus, it can be inferred that the offset error tolerance for the output is within ±0.64 mV.

Table 6: Error Criteria for Comparator

Error Type	Ideal_Offset	Comparator_Offset
NO error	± <0.64mV	as Low as possible
±1 LSB error	±0.64mV	as Low as Possible

2.2 Floorplanning.

For the floorplan of the proposed iADC, below shown RC values have been considered which fulfill the criteria of having a time constant of 20.48us and also are looking symmetrical which would also fulfill the need of stability in the design.

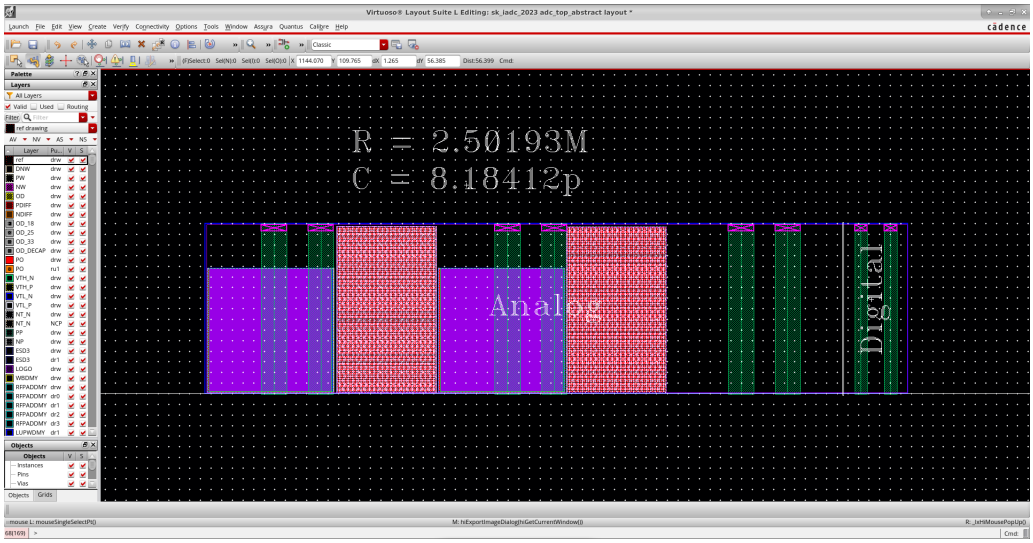

Figure 12: Floorplan of the iADC with the RC.

3 References

1. T. Chan Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed.
3. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed.
4. Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 4th ed.