

# Design and Implementation of Analog Circuits and Systems

Deliverable D2: Integrator AFE design report

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March 31, 2024

# 1 ADC Function Description

The Analog-to-Digital Converter (ADC) function described below performs the continuous conversion of a differential input voltage ( $V_{\text{in}_p} - V_{\text{in}_n}$ ) with respect to a differential reference voltage ( $V_{\text{ref}_p} - V_{\text{ref}_n}$ ) into a digital sign/magnitude bus. The conversion is executed at a constant sample rate using a dual-slope integrating function to achieve the best possible conversion time.

## Parameters

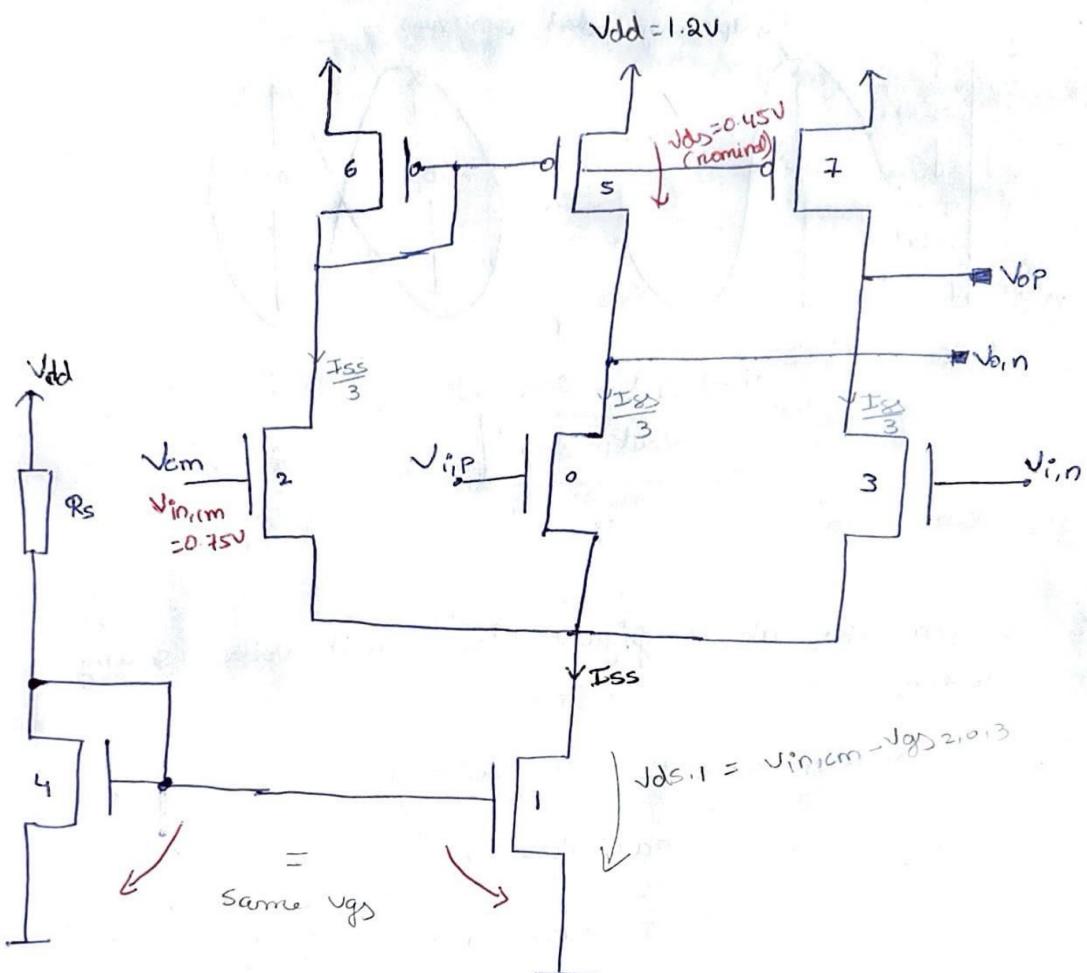
- Supply voltage:  $V_{\text{dd}} = 1.2 \text{ V}$
- Common mode voltage:  $V_{\text{cm}} = 0.75 \text{ V}$
- Reference voltages:  $V_{\text{ref}_p} = 1 \text{ V}$ ,  $V_{\text{ref}_n} = 0.5 \text{ V}$
- Digital input clock: 50 MHz
- Full-Scale Range (FSR):
  - $V_{\text{in}_{\text{max}_p}} = V_{\text{in}_{\text{max}_n}} = 1 \text{ V}$
  - $V_{\text{in}_{\text{min}_p}} = V_{\text{in}_{\text{min}_n}} = 0.5 \text{ V}$  (absolute)
  - $V_{\text{in}_p} = V_{\text{in}_n} = \pm 0.25 \text{ V}$  (relative to  $V_{\text{cm}}$ )
  - $V_{\text{in}_{\text{pp, single-ended}}} = 0.5 \text{ V}$ ,  $V_{\text{in}_{\text{pp, differential}}} = 1.0 \text{ V}$  (dynamic range, with respect to  $V_{\text{cm}}$ )
- Output code: 11 bits (using sign/magnitude format)
- Output clock: Signaling a new sample available with a constant period expected
- Conversion time: Better than 2500 input clock cycles ( $< 50 \mu\text{s}$ ) leading to at least 20 kS/s sample rate
- Total Unadjusted Error (TUE):  $\pm 1 \text{ LSB}$  typical is possible, aiming for less than  $\pm 3 \text{ LSB}$

## 2 Design of analog front end (AFE):

### 2.1 Analysis and Design of Integrator Circuit :-

\* DC

operating point analysis:-



\* The Common mode voltage  $V_{cm}$  is given as 0.75V.

∴ the voltage drop across transistors 5 & 7

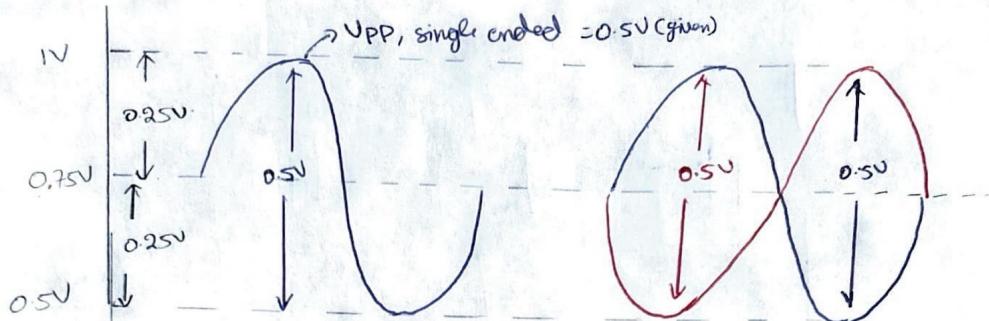
is

$$V_{DD} - V_{cm} = V_{DS,5,7}$$

$$1.2 - 0.75 = 0.45V$$

$$\therefore V_{DS,5,7} = 0.45V$$

- \* The maximum output swing (peak to peak differential)  $V_{out,PPD} = 1V$  (given).



$$V_{out, PPD} = 0.5(0.5)$$

$$\therefore V_{out, PPD} = 1V$$

- \* As per the above figure the output voltage swing between.

$$V_{out, max} = 1V \quad \& \quad V_{out, min} = 0.5V$$

So, max  $V_{DS, 5, 7}$  is

$$V_{DS, 5, 7, \max} = 1.2 - 0.5 = 0.7V$$

$$V_{DS, 5, 7, \min} = 1.2 - 1 = 0.2V.$$

- \* Maximum & minimum allowed voltage range :-

④ Transistors 0, 2 & 3

$$V_{IP, \min}, V_{IN, \min}, V_{INCM, \min} = V_{eff, 1} + V_{GS, 2, 0, 3}$$

$$V_{IP, \max}, V_{IN, \max} = V_{dd} - V_{eff, 5, 7} + V_{tp}$$

$$V_{INCM, \max} = V_{dd} - V_{GS, 6} + V_{tp}$$

- Max output voltage :-  $V_{out, Pmax} = V_{dd} - V_{eff, 5,7}$
- Min output voltage :-  $V_{out, Pmin} = V_{eff, 1} + V_{gs, 0,3} - V_{to, 1,3}$   
 $= V_{eff, 1} + V_{eff, 0,3}$ .

### Conclusion :-

- $V_{eff, 5,7}$  must be smaller 0.2V.
- For maintaining common mode  $V_{eff, 1}$ , should be smaller.
- To maximize o/p voltage swing all  $V_{eff}$  should be as small as possible.
- high  $\frac{g_m}{I_d}$  of all transistors.

$$g_m = \frac{2I_d}{V_{eff}} \Rightarrow V_{eff} = \frac{2I_d}{2g_m}$$

### \* Current source resistance.

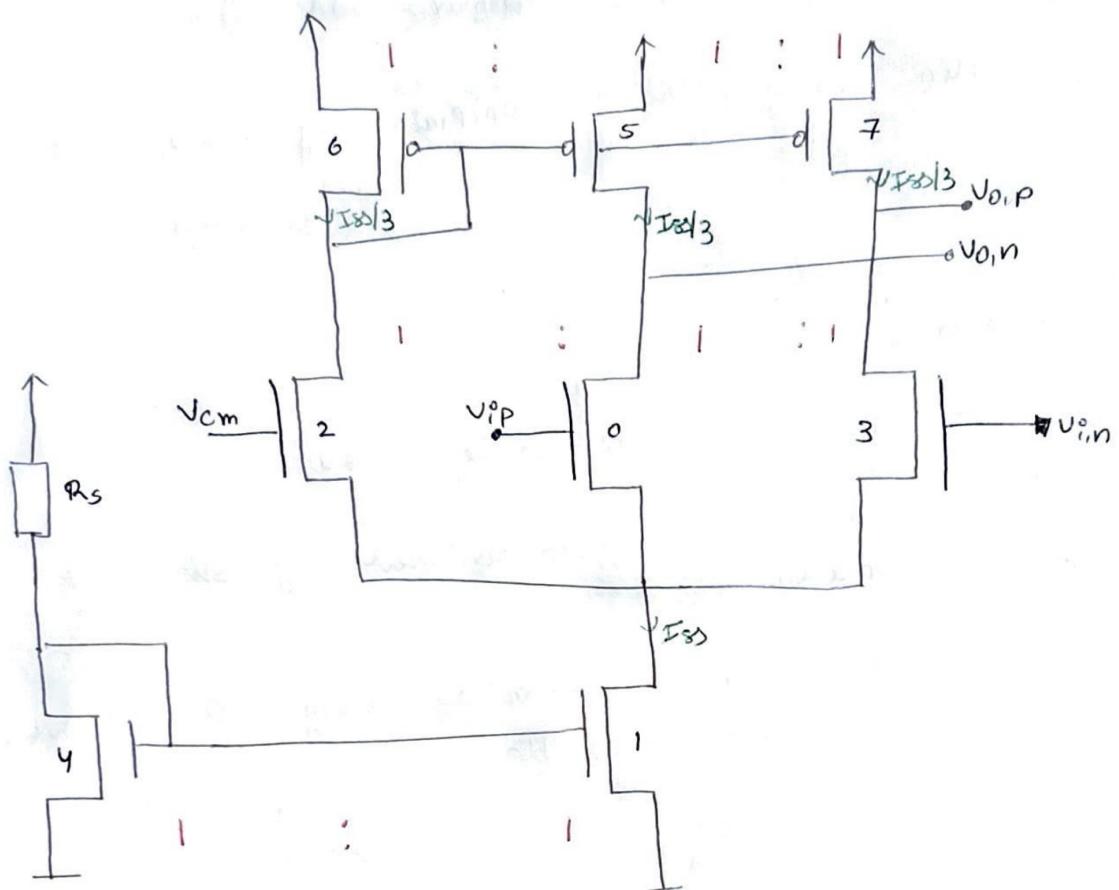
$$I_d = \frac{V_{dd} - V_{ds, 1,4}}{R_s}$$

$$\boxed{R_s = \frac{V_{dd} - V_{ds, 1,4}}{I_d}}$$

$$[V_{ds, 1,4} = V_{gs, 1,4}]$$

- The resistor value to be chosen based on to maintain minimum  $V_{eff, 4}$ .  $[V_{ds, 4} = V_{gs, 4}]$ .

## \* Amplifier Circuit analysis & sizing



- Matching the currents between the NMOS transistors [073] & PMOS transistor [577] in the differential pair is the key task.
- If there is any mismatch between this two differential pairs, then common mode voltage can go up or down depending on the current flowing through the transistors.

\* MOS Sizing.

\* To satisfy the current requirements for all the transistors & to maintain all the transistors are in saturation. Below sizing can be chosen for the analysis.

NMOS :-

$$\left(\frac{w}{L}\right)_{2,0,3} = 10 \rightarrow \left(\frac{w}{L}\right)_{4,1} = \text{---} 10$$

PMOS :-

$$\left(\frac{w}{L}\right)_{6,5,7} = 10$$

$\left(\frac{w}{L}\right)$  of transistors 2,0,3 & 6,5,7 are maintained same for good matching [to have same currents]

## 2.2 Integrator Initial Setup:-

The circuit configuration was initially established through analysis, employing a W/L ratio of 10. To ensure effective feedback within the circuit, substantial values were assigned to both the Inductor and capacitor components.

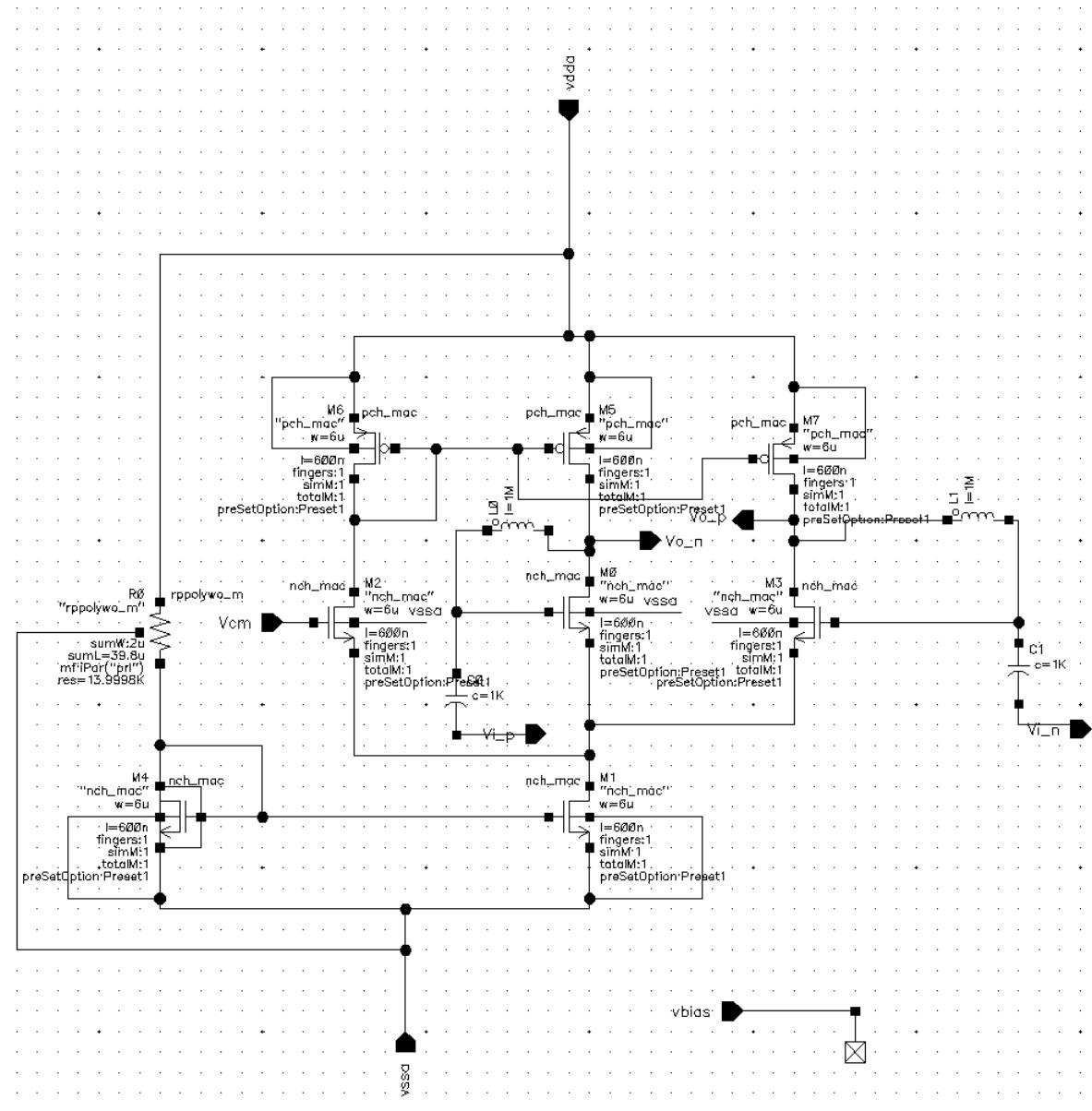


Figure 1: Schematic Representation of the Integrator Circuit with Hand-Estimated W/L Ratios

### 2.2.1 DC simulation to find region of operation:-

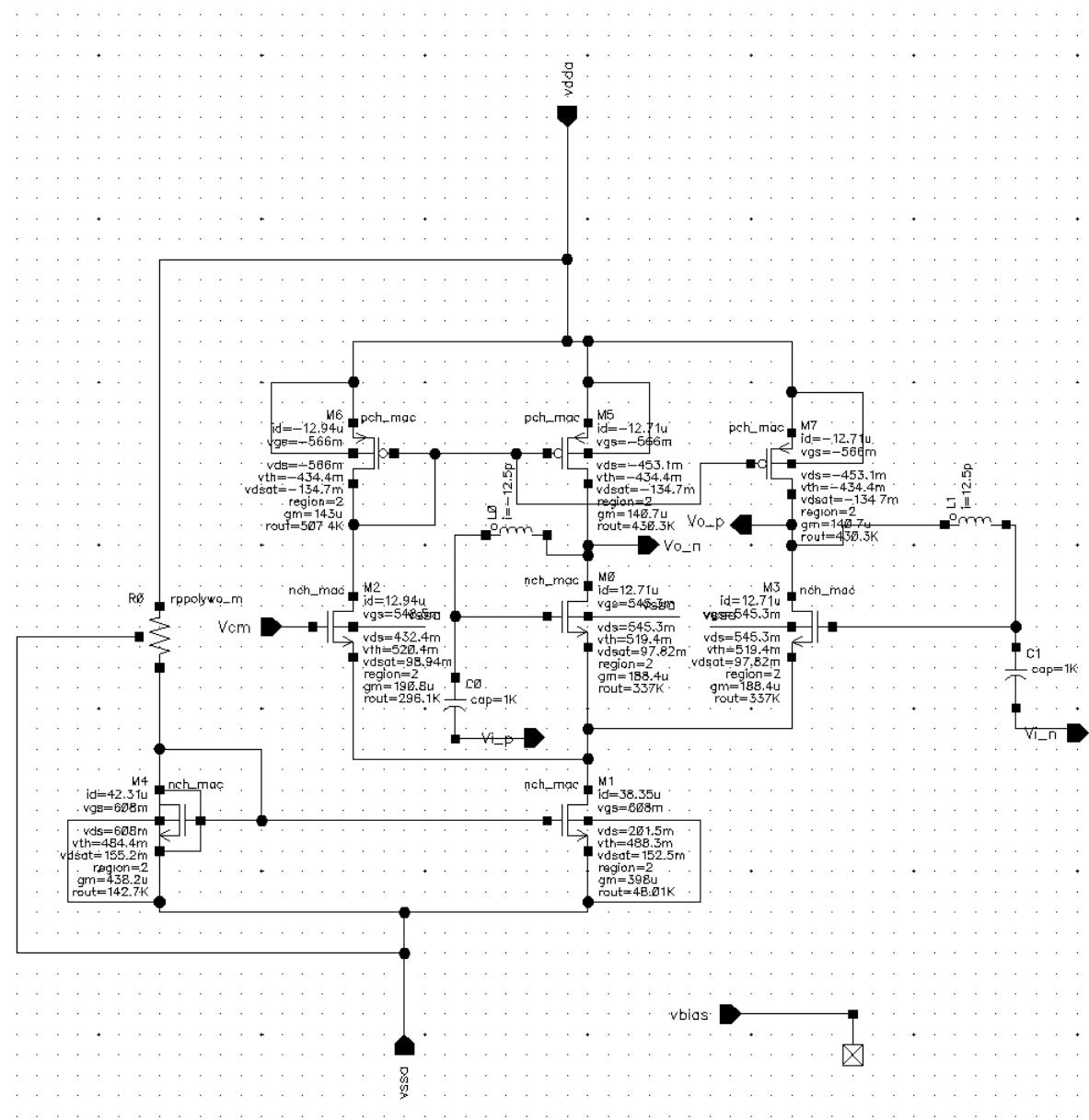


Figure 2: DC Operating Point Analysis of the Integrator Circuit with Initial Configuration

### Observation:-

- All transistors are operating within the saturation region.
- The current flowing through the differential pair is identical, indicating a high degree of matching between the transistors.
- The amplifier's gain can be further enhanced by increasing the transconductance (gm) and output resistance (rout).

### 2.2.2 Transient Analysis:-

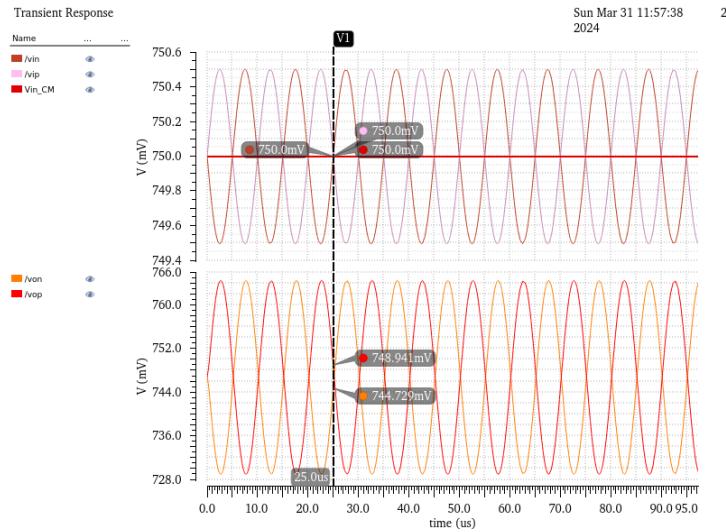


Figure 3: Transient Analysis of the Integrator Circuit with Initial Configuration

### Conclusion :

The circuit can be further optimized to achieve increased gain by augmenting the output resistance ( $r_{out}$ ), which can be accomplished through lengthening the transistors while maintaining the same current flow through both NMOS and PMOS. It is essential to meticulously refine the DC operating point for subsequent simulations.

### 2.3 Circuit Optimization:

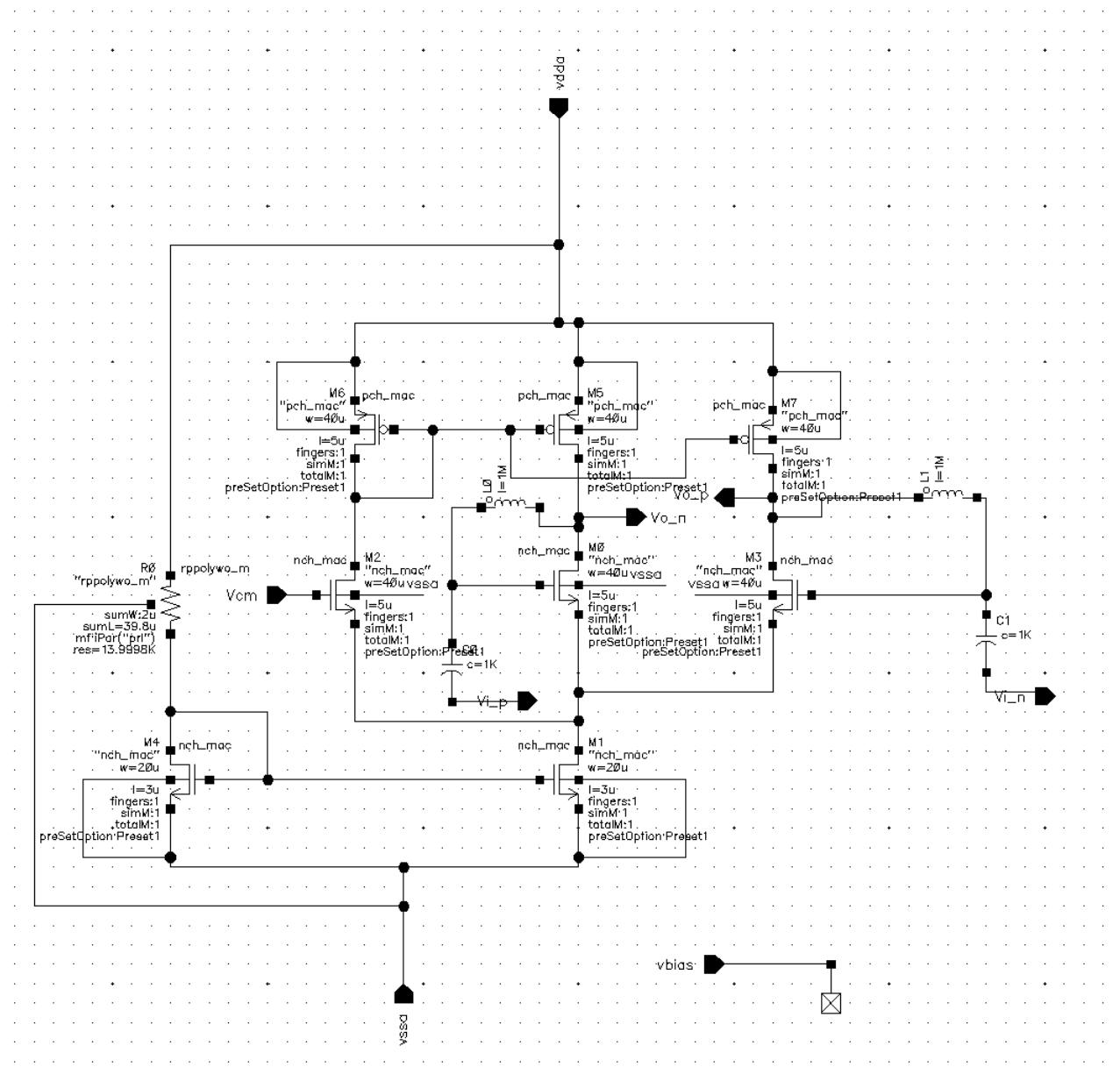


Figure 4: Integrator Circuit Schematic

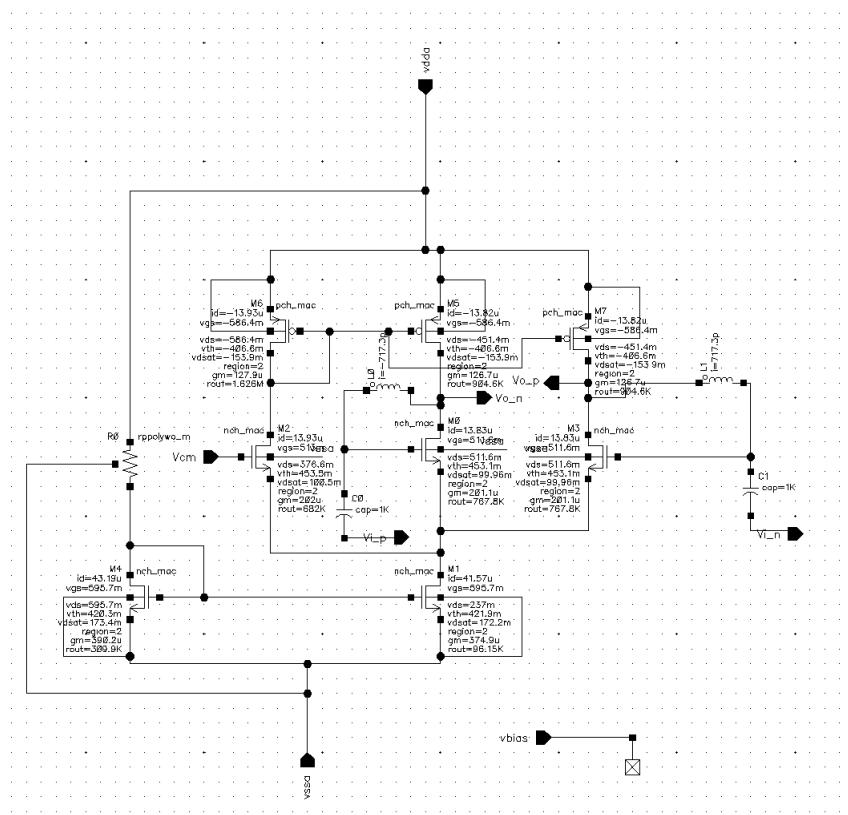


Figure 5: Integrator Circuit DC operating point

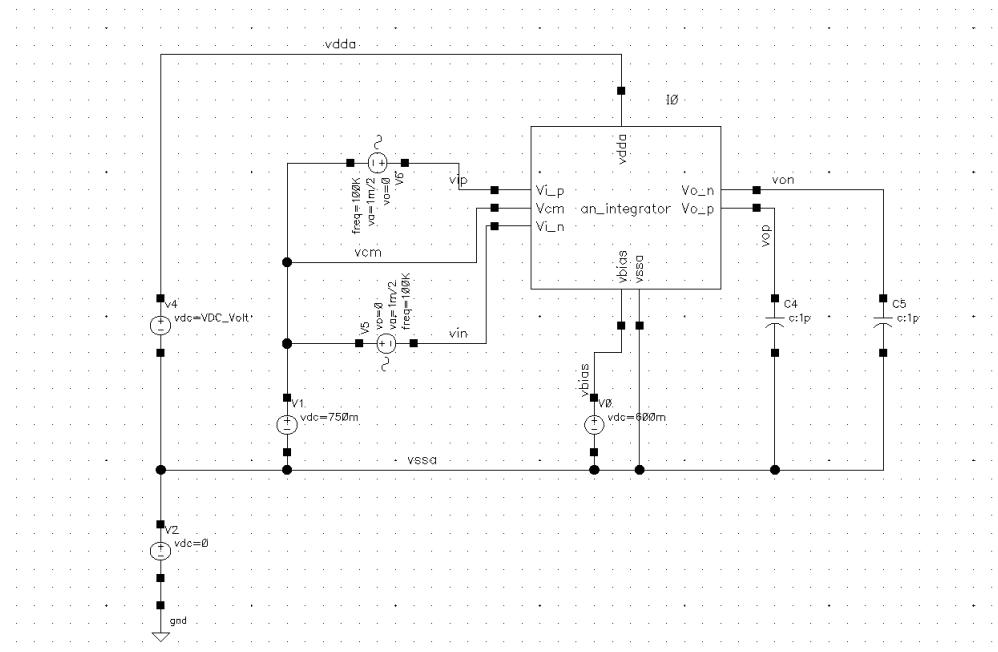


Figure 6: Test bench of the Integrator Circuit

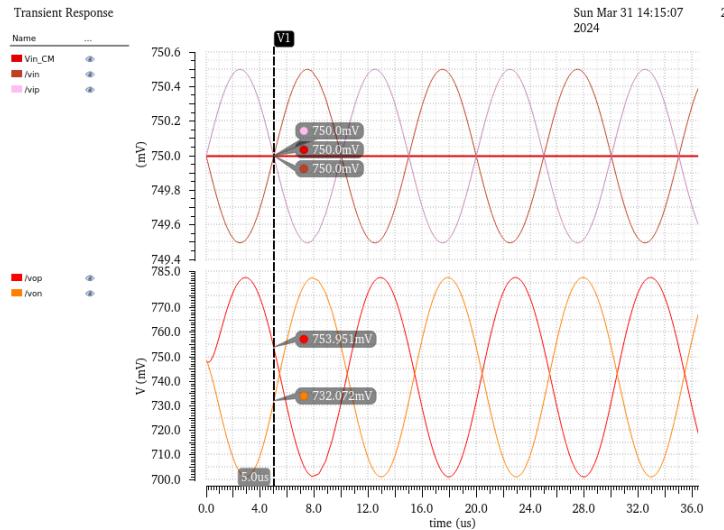


Figure 7: Transient analysis of the Integrator Circuit

### Observation:-

- Following circuit optimization, the output resistance ( $r_{out}$ ) has significantly increased along with the transconductance ( $gm$ ), resulting in a substantial boost in gain.
- The input common-mode voltage is 0.75V, while the output common-mode voltage is maintained at 748.6mV.
- The current through the differential pair has been kept constant.
- The small-signal differential gain is 38.43 dB.
- The large signal gain is 81.03.(The discussion regarding gain is provided in a subsequent section.)

## 2.4 Integrator AC and Transient Analysis:-

### Transient Analysis:-

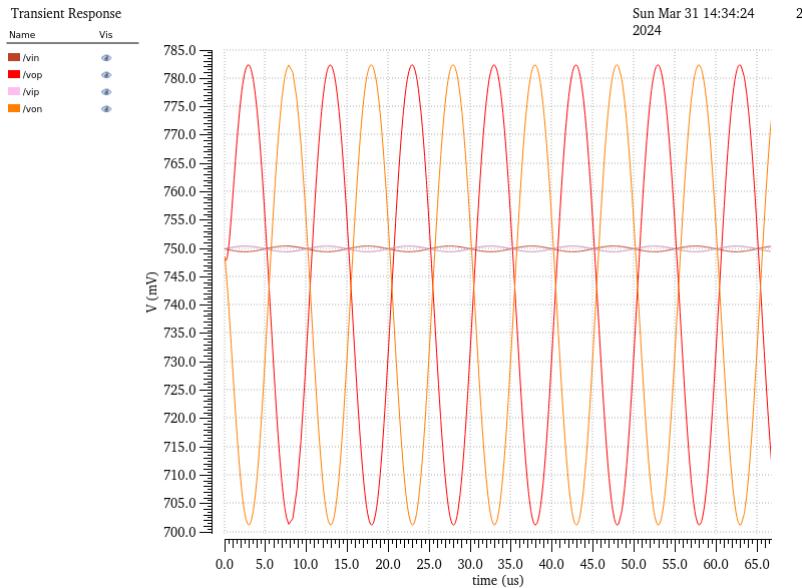


Figure 8: Transient analysis for Differential Gain

Large signal differential gain is given as ,**Add** = ((peakToPeak(v("/vop" ?result "tran")) + peakToPeak(v("/von" ?result "tran")))) / (peakToPeak(v("/vip" ?result "tran")) + peakToPeak(v("/vin" ?result "tran")))) = **81.03**

### AC analysis:-

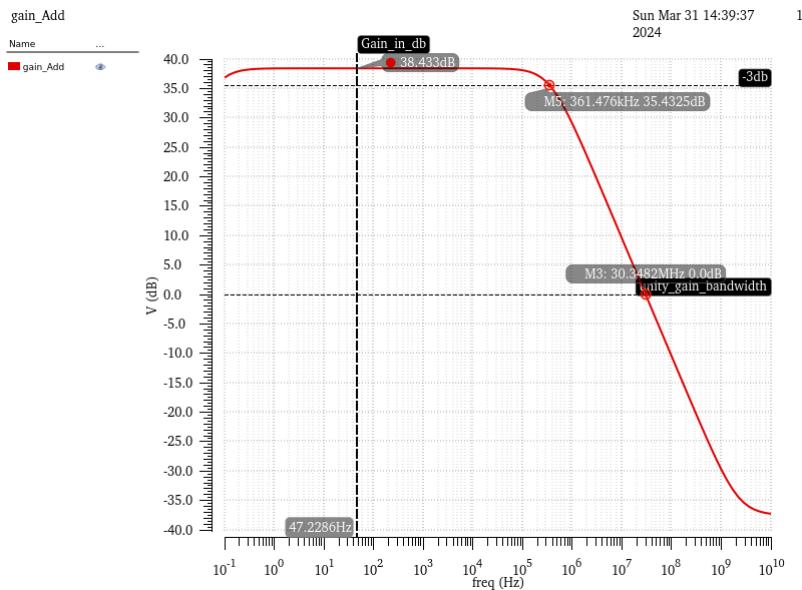


Figure 9: AC analysis for Differential Gain

Small Signal gain Add calculated by hand calculation :-

$$\text{Add} = g_{m0,3} \times (r_{out0,3} || r_{out5,7})$$

Given  $g_{m0,3} = 201.1\mu$  and  $r_{out0,3} || r_{out5,7} \approx 415.302\Omega$ :

$$\text{Add} = 201.1 \times 10^{-6} \times 415.302$$

$$\text{Add} \approx 83.517 \text{ V/A}$$

Therefore, the calculated value of **Add** is approximately **83.517 V/A**.

$$\text{Add(dB)} = 20 \times \log(83.517)$$

$$\text{Add(dB)} \approx 38.43 \text{ dB}$$

Therefore, the calculated value of Add in dB is approximately **38.43 dB**.

### Observation:-

- The small-signal gain observed is 38.433 dB as depicted in the figure above.
- The unity gain bandwidth observed is 30.3482 MHz at 0 dB gain.
- The -3 dB bandwidth of the integrator is 361.476 kHz

### 2.5 DC Offset Voltage:

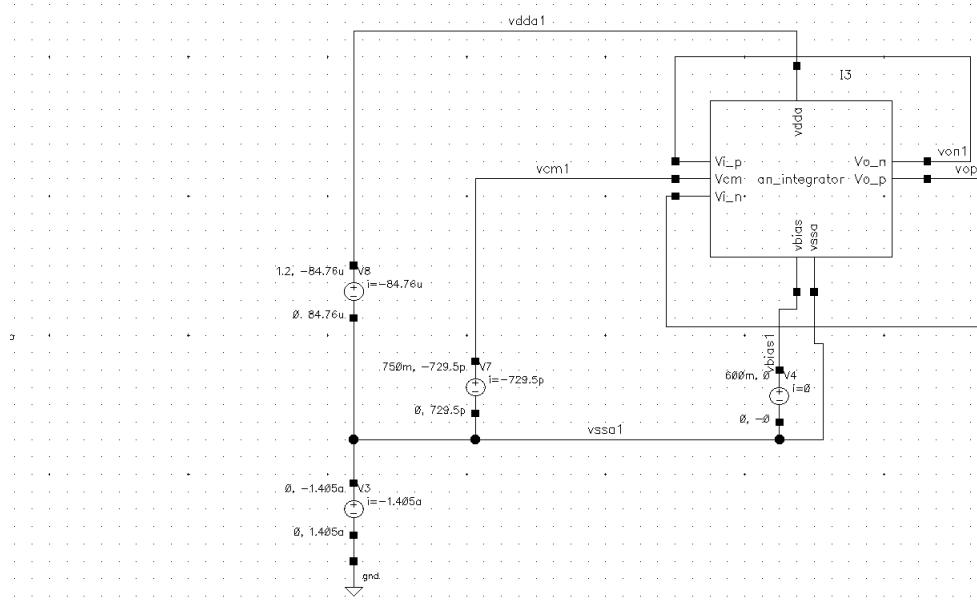


Figure 10: Test bench set up to measure offset voltage

DC simulation was conducted to measure the offset voltage by plotting the output difference. Any discrepancy between the transistors would be evident through the

observed offset voltage.

$$\text{Offset Voltage} = (\text{VDC}("/\text{vop1}") - \text{VDC}("/\text{von1}"))$$

The offset Voltage can be calculated by using the formula:-

$$(\text{V}_{os})^2 = (\Delta V_t)^2 + \frac{(\text{V}_{eff})^2}{4} \left( \frac{\Delta I_d}{I_d} \right)^2$$

$\Delta V_t$  is the difference in threshold voltage.

$V_{eff}$  is the effective overdrive voltage.

$\Delta I_d$  is the difference in drain current.

$I_d$  is the drain current.

According to this formula, the offset voltage is primarily determined by the threshold voltage mismatch and the effective overdrive voltage of the device. While the threshold voltage mismatch is inherent to device characteristics and beyond our control, the effective overdrive voltage can be managed. Therefore, to minimize the offset voltage, it is crucial to reduce the effective overdrive voltage.

By using the Pelgrom's law

$$\sigma(\Delta V_t) \propto \sqrt{\frac{W}{L}}$$

This relationship suggests that as the transistor's aspect ratio (width-to-length ratio) increases, the variability in threshold voltage mismatches decreases, assuming all other factors remain constant.

To measure offset mismatch, Monte Carlo simulation was conducted, and the histogram was plotted as depicted below. **The calculated  $3\sigma$  value of the offset is 1.10 mV**, which is less than 3 mV.

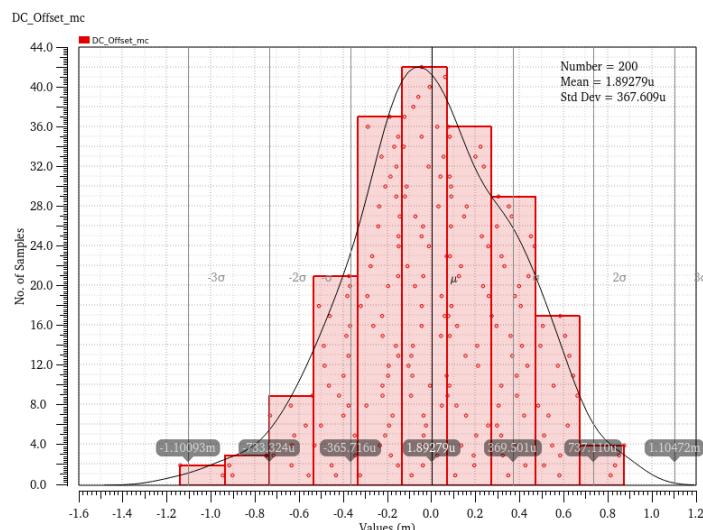


Figure 11: Monte Carlo Simulation to measure Offset

To quantify the **Threshold mismatch** between devices, the following expression was utilized:-

$$(\text{OP}(" / \text{I0/M0" } " \text{vth" }) - \text{OP}(" / \text{I0/M3" } " \text{vth" }))$$

The histogram plot of the threshold mismatch can be seen below. The  **$3\sigma$  voltage variation value** measured from the graph is **1.128 mV**.

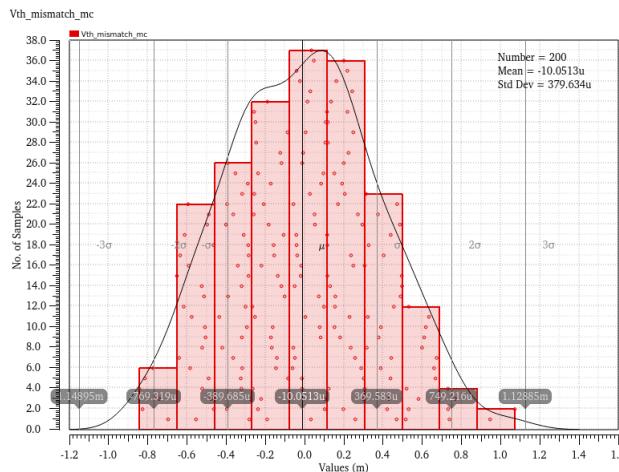


Figure 12: Monte Carlo Simulation to measure Threshold Voltage mismatch

## 2.6 Output Common mode and Transistor Region of operation:

The output common-mode voltage and transistor regions were evaluated through Monte Carlo simulation and worst-case corner analysis. These methodologies enabled the assessment of variations in the common-mode voltage and ensured coverage of extreme operating conditions across different transistor regions.

The expression used to measure output Common mode voltage is :-  
 $((\text{VDC}(" / \text{vop" }) + \text{VDC}(" / \text{von" })) / 2)$

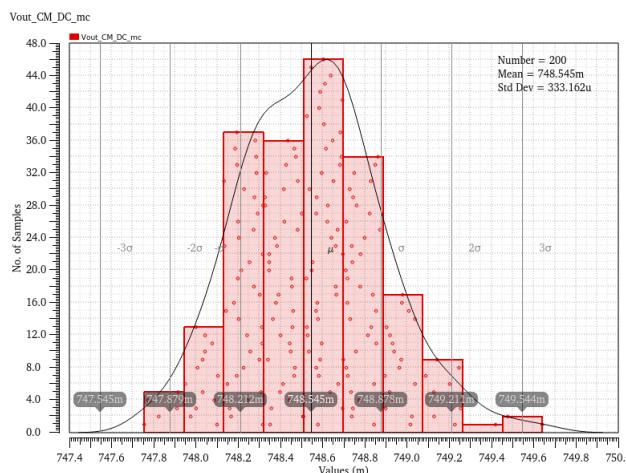


Figure 13: Monte Carlo Simulation for Output Common mode voltage

Parameter	Nominal				ff_0	ff_1	ff_2	ff_3	ff_4	ff_5	ff_6	ff_7	ff_8	fs_0	fs_1			
VDC_Volt	1.2				1.08	1.08	1.08	1.2	1.2	1.32	1.32	1.32	1.08	1.08				
temperature	27				-30	27	80	-30	27	80	-30	27	-30	27				
toplevel.scs	tt.lib				ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb	ff_llb			
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	ff_0	ff_1	ff_2	ff_3	ff_4	ff_5	ff_6	ff_7	ff_8	fs_0	fs_1
an_iadc_2023an_integrator_test1_M2		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M0		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M3		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M1		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M4		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M6		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M5		2				2	2	2	2	2	2	2	2	2	2	2	2	2
an_iadc_2023an_integrator_test1_M7		2				2	2	2	2	2	2	2	2	2	2	2	2	2

Figure 14: Worst Case corner simulation for Transistor region of operation.

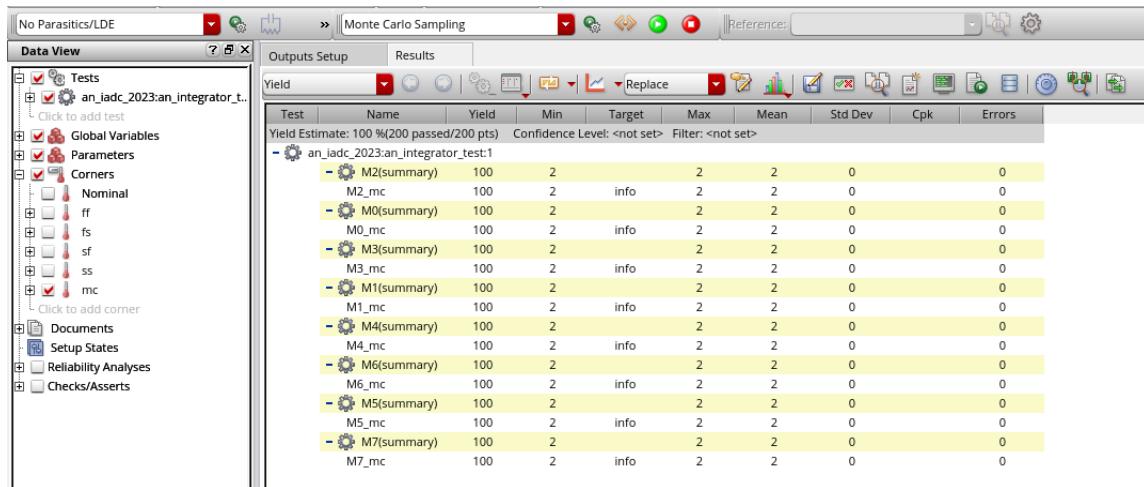


Figure 15: Monte Carlo Simulation for Transistor region of operation

Corner and Monte Carlo simulations were conducted, confirming that the transistors operate exclusively in the saturation region under all tested conditions. The results can be seen above.

## 2.7 Common Mode Gain (Acc):

When the inputs are shorted, it implies that the differential input voltage ( $V_{id}$ ) is zero. Additionally, a common-mode voltage with an AC magnitude of 1V is applied, and the resulting output common-mode voltage ( $V_{ocm}$ ) is measured as the average of the positive and negative output voltages ( $V_{op}$  and  $V_{on}$ ).

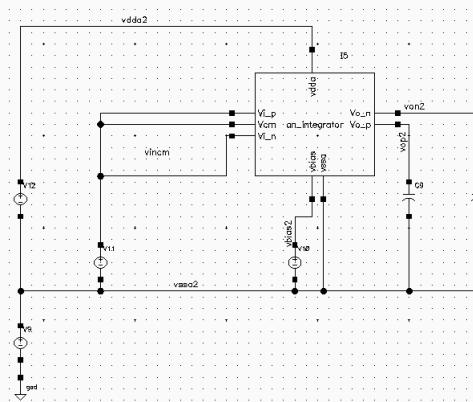


Figure 16: Test bench setup to measure Output common mode

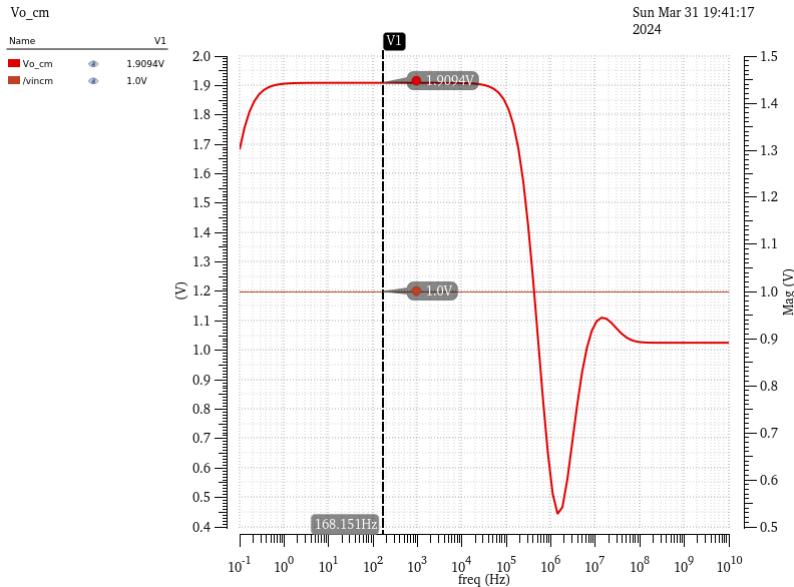


Figure 17: AC simulation of Output common mode gain

**Common Mode gain (ACC)** The common-mode gain (Acc) of an amplifier quantifies how much the output voltage changes in response to a common-mode input signal. In the provided testbench, a common-mode input of 1V (AC magnitude) is applied, resulting in an output common-mode voltage of 1.909V.

$$V_{ocm} = \frac{V_{op} + V_{on}}{2}$$

$$A_{cc} = \frac{V_{ocm}}{V_{icm}} = \frac{1.909}{1} = 1.909 = 5.616dB$$

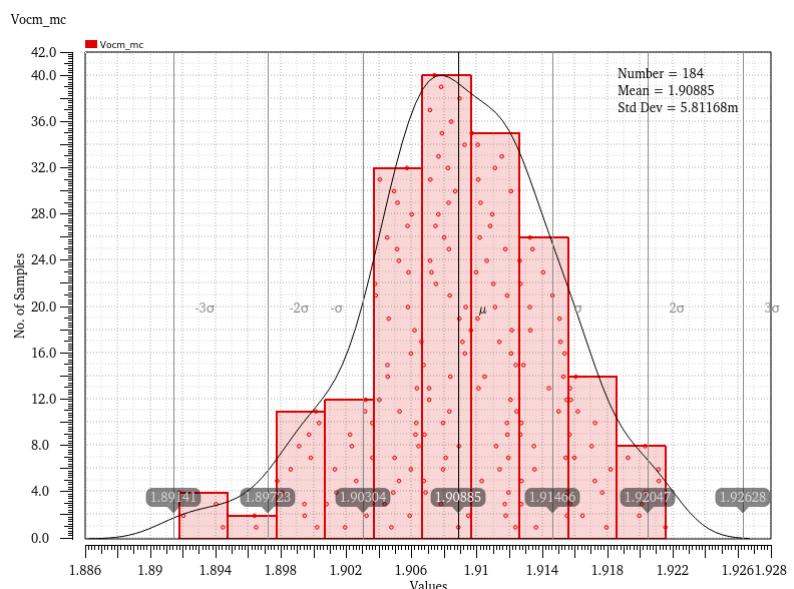


Figure 18: Monte Carlo simulation of Output common mode

A Monte Carlo simulation was conducted to analyze the output common-mode voltage,

with the observed 3-sigma voltage being 1.92 V.

## 2.8 Performance parameters:

**1. Output common mode variation:** The output common-mode variation, as discussed in section 2.6, can be calculated as follows:

$$dV_{out,cm} = 750 \text{ mV} - 749.6 \text{ mV} = 0.4 \text{ mV} \times (3\sigma) \text{ (approx)}$$

$$dV_{out,cm} = 0.133 \text{ mV} \times (1\sigma)$$

## 2. Common Mode Rejection Ratio (CMRR)

The Common Mode Rejection Ratio (CMRR) is a metric that quantifies the ability of a differential amplifier to reject common-mode signals. It's determined by comparing the differential gain (Add) to the common-mode gain (Acc).

$$\text{CMRR} = \text{ADD/ACC} = 38.43/5.616 = 6.842 \text{ dB}$$

## 3. Input impedance ( $Z_{in}$ ):

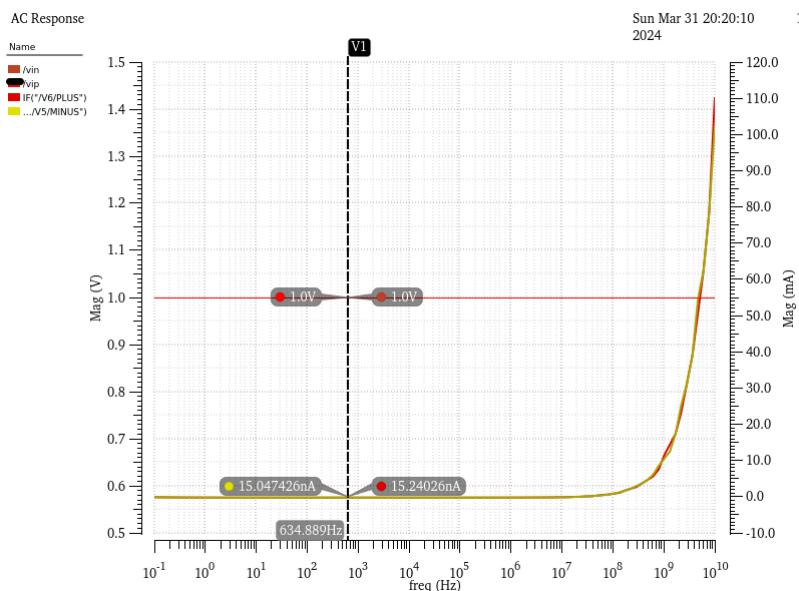


Figure 19: AC Analysis for input Impedance

$$Z_{in} = \frac{V_{ip} - V_{in}}{I_{ip} - I_{in}} = 66.45 \text{ M}\Omega$$

## 2.9 Top Model simulation :

The transient analysis for the top model simulation was conducted, wherein all the ideal building blocks of analog were replaced. The resulting output exhibited a 1 LSB error within the range of  $\pm \text{FSR}$  and a 2 LSB error within the range of  $\pm \text{FSR}/2$ .

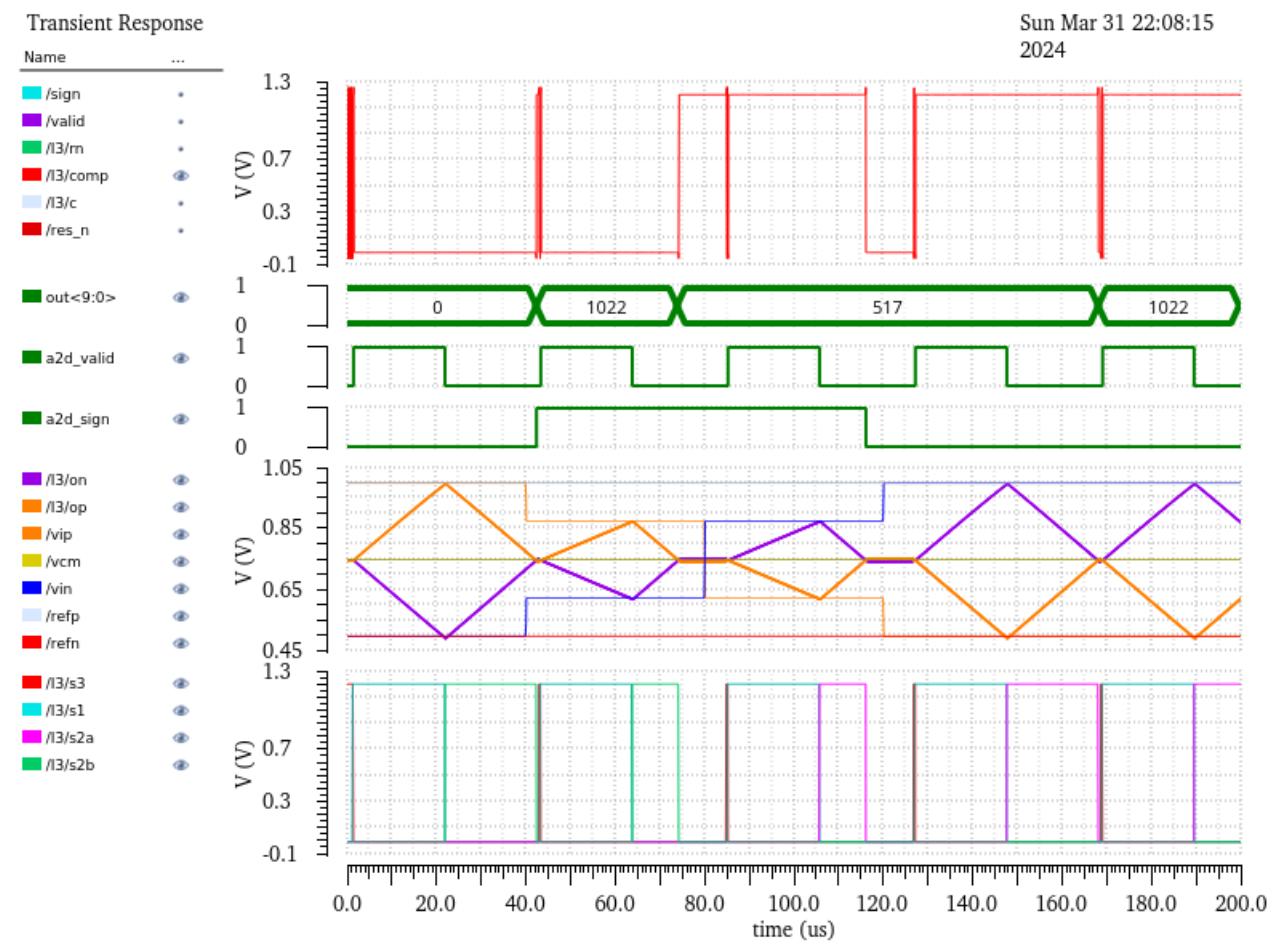


Figure 20: Transient Analysis of the Top Model

### 3 References

1. T. Chan Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed.
3. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed.
4. Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 4th ed.