Design and Implementation of Analog Circuits and Systems

Tapeout sign-off document

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1 Final Checks :

2.1 Final DRC and LVC clean check :-

Note: All top-level checks for the iADC have been completed in the `iadc_to_lib` library.

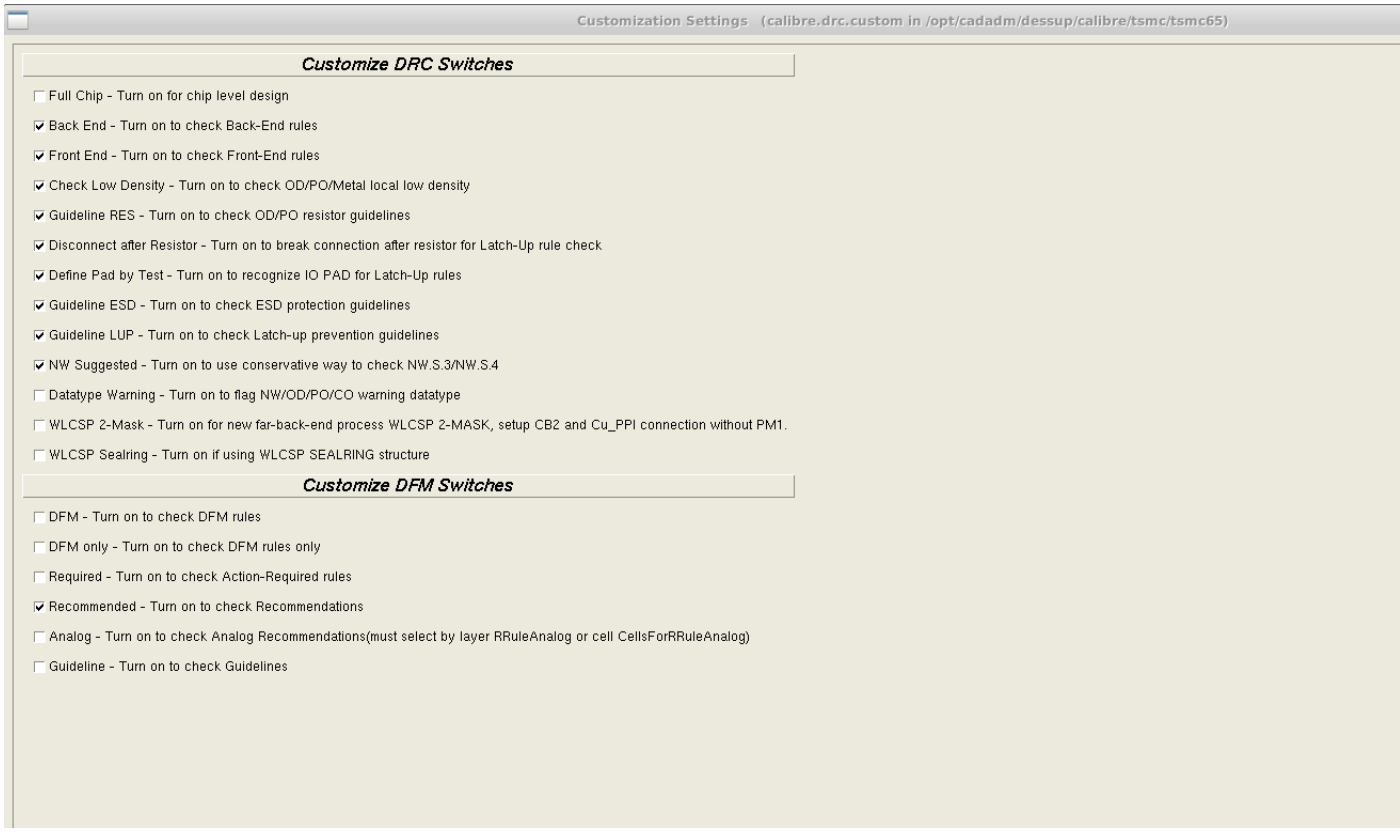

Figure 1: DRC calibre setting.

This were the Calibre DRC settings that were selected to perform the DRC for the top level iADC.

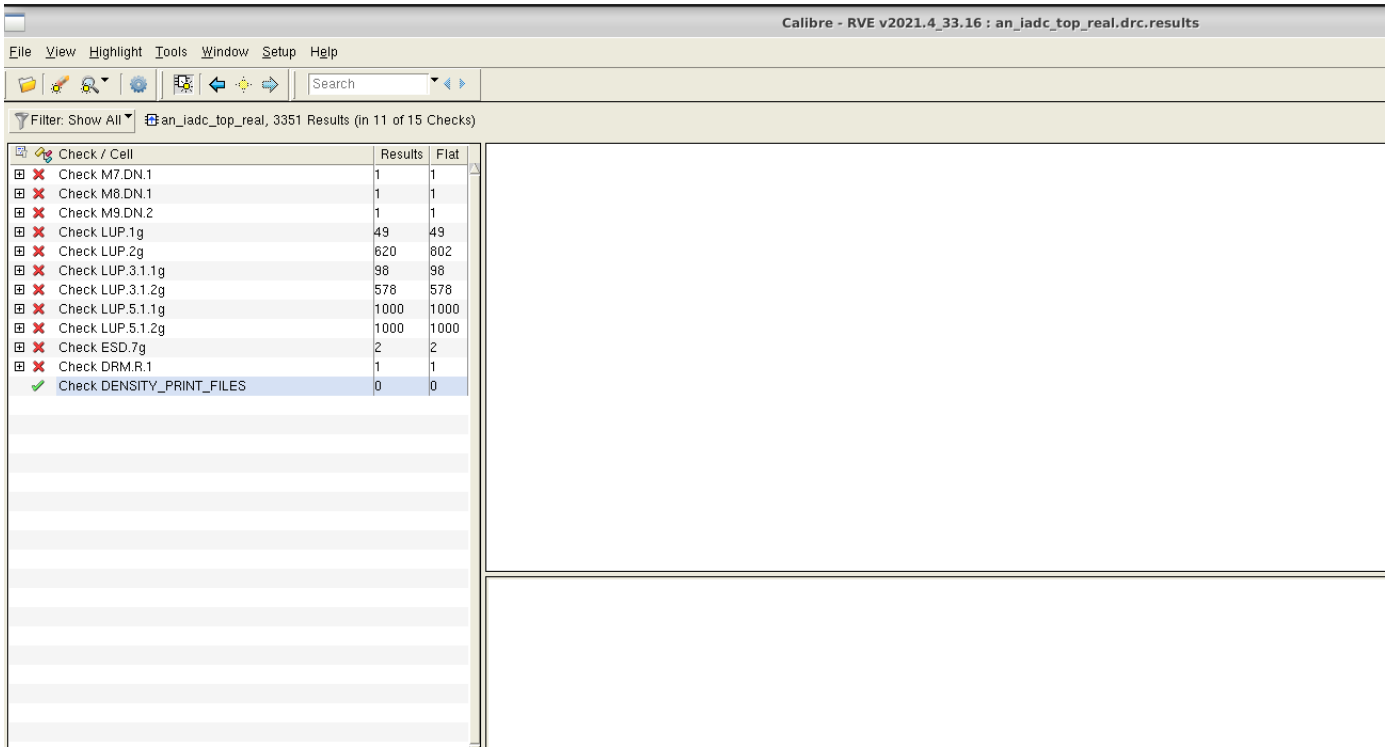

Figure 2: Above is the final DRC result that is obtained with the above DRC calibre settings.

The first three errors are related to the metal density of layers 7 to 9, which are not used in our top layout. Since we only utilize metal layers up to metal 6, we can waive these errors.

All the LUP errors are arising from both the digital and analog sections. Once the design is directly connected to an external pad, these errors will disappear. Therefore, I am waiving these errors as well.

I encountered two errors for ESD.7g, both related to the digital components.After reviewing them and finding nothing out of the ordinary, I decided to waive them.

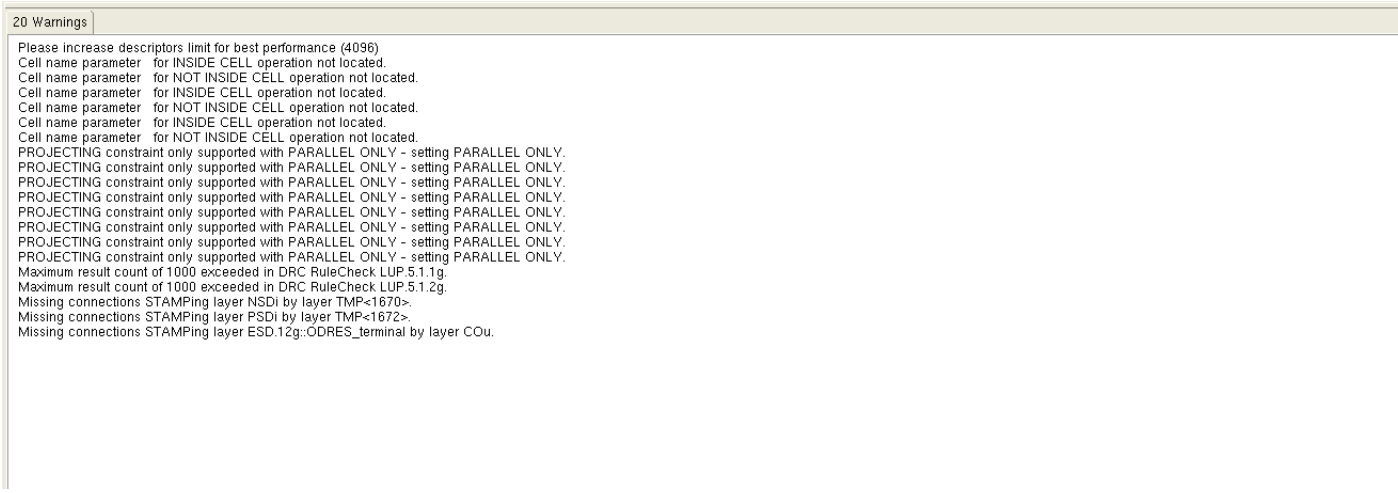

Figure 3: DRC Warnings.

The warnings mentioned above appear when we run DRC with the specified settings. Aside from these, I did not encounter any other errors.

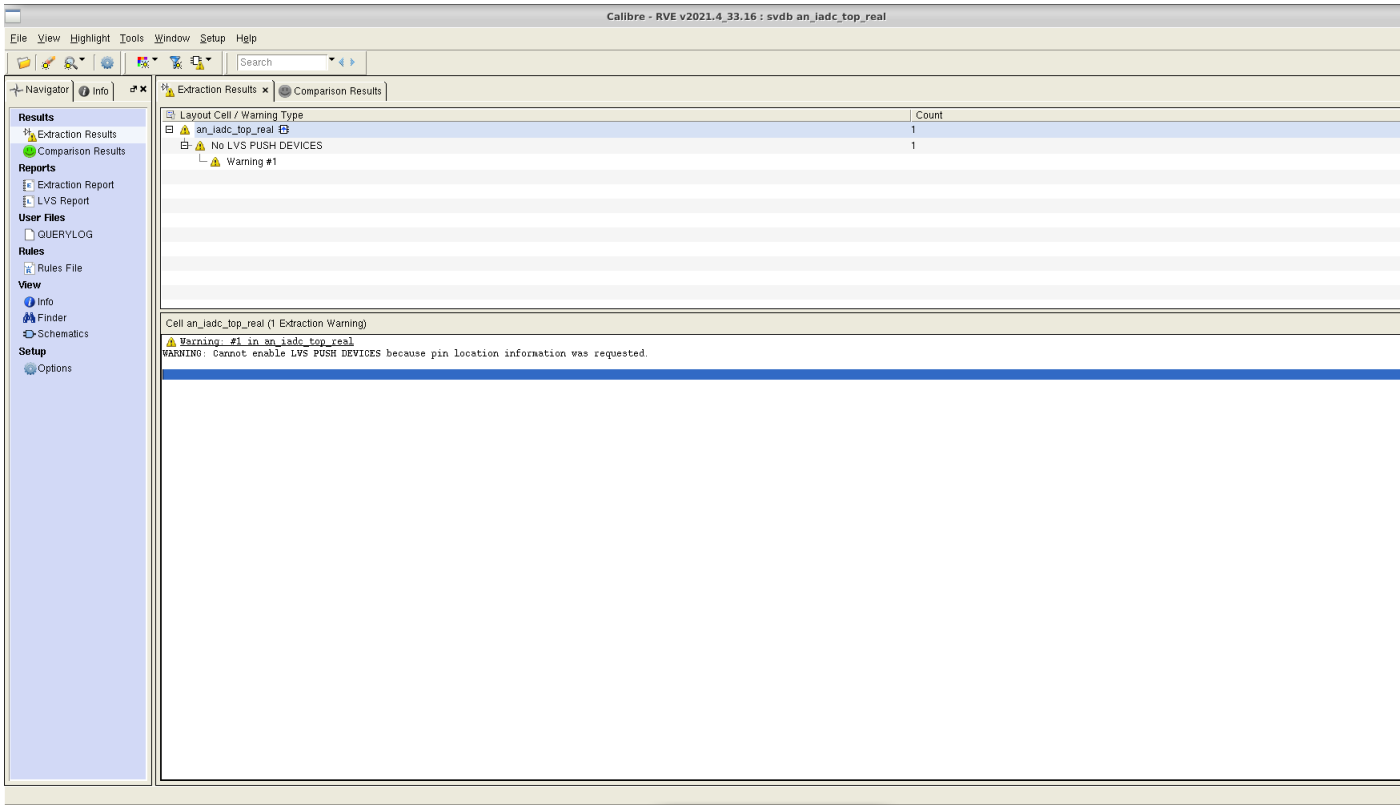

Figure 4: LVS result of iADC.

LVS should indicate "OK" (green), but I am receiving one warning. I am unsure whether this warning is critical, as there is no specific information provided about it. Therefore, I am disregarding it.

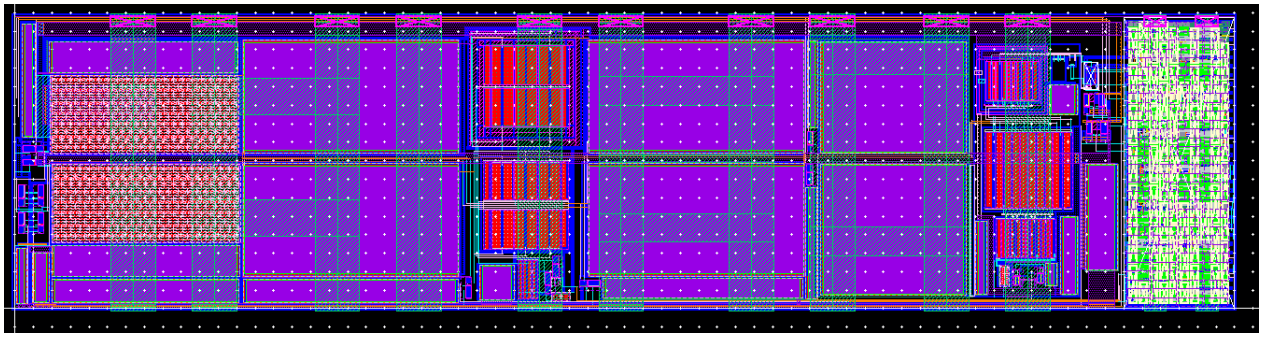

Figure 5: iADC top Layout after metal filling.

The layout filling has been completed, satisfying the metal density check and remaining within the specified PR boundary. All provided pin placements for both analog and digital sections have been adhered to.

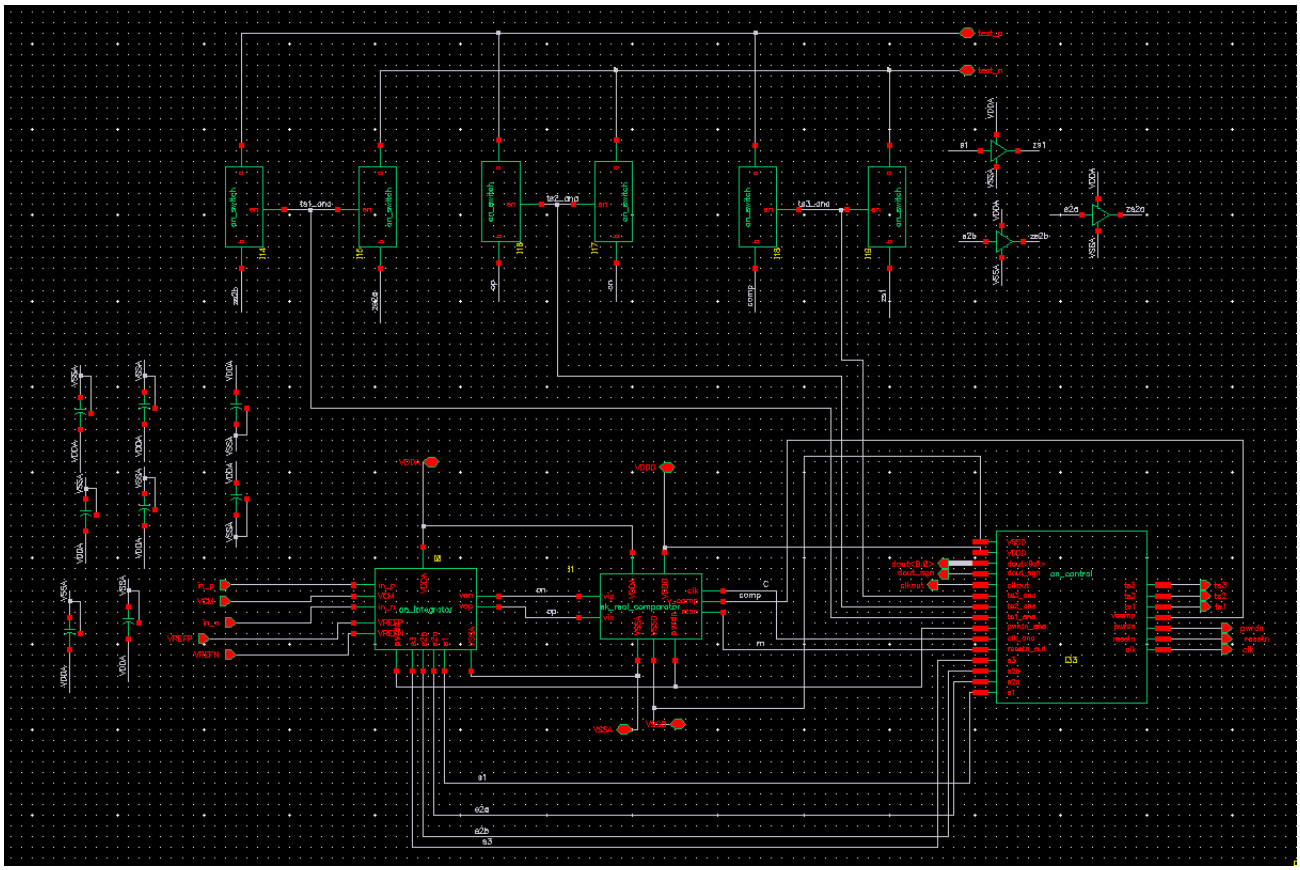

Figure 6: iADC top level Schematic.

The above is the iADC top-level schematic used to clear the LVS at the top level. All pins have been reused from the given project library, and all input/output pin names are matching.

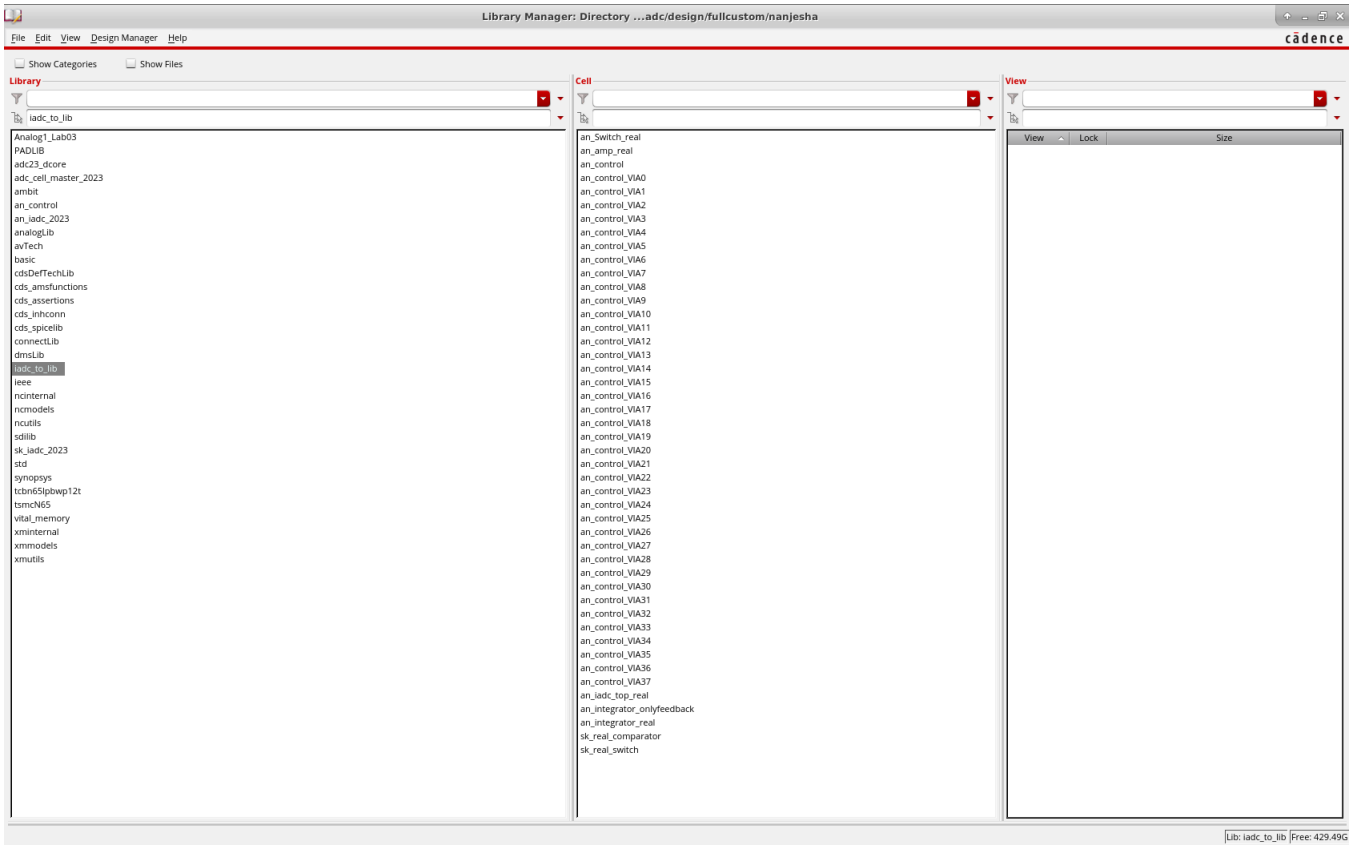

Figure 7: Cells of your IADC design.

The following cells, both digital and analog, are included in the given tapeout library "iadc_to_lib." All cells have been cross-checked and confirmed to be in the tapeout library.