EE 677 Foundation of VLSI CAD
Project Report

Team Members- Navnit Kumar *(16D070053)*
Amit Kumar *(16D070034)*

Objective : The aim of our project is to estimate the maximum delay for timing analysis in a combinational multi-level circuit assuming all gates have same delays. We have considered combinational circuit as Directed Acyclic Graph (DAG) where nodes represents all the operations and directed edges represent data.
So we have used Topological sorting algorithm for ordering the DAG and then calculated the longest distance on it according to the algorithm below. We have implemented it using C++ .

APPROACH:

Topological Sorting :

Topological sorting in Directed Acyclic Graph is a linear ordering of vertices such that there is no directed edge going from any vertex to an earlier vertex in the sequence. Depending on our DAG we may have more than one topological ordering of the same graph. If nodes in our graph represent certain computational task in the circuit and edges represent some constraint that one task must be completed before another, then Topological ordering is just a valid sequence of computational tasks to be performed in order to get correct output.

Longest path in a DAG

ALGORITHM :

- Let $i_1, i_2, \ldots, i_n$ be our topological ordering of our DAG representation of circuit.
- All neighbours of i_k appear before it in this topological list
- From left to right, we now compute longest path to(i_k) as below :

  $1 + \max\{ \text{longestpathto}(i_j) \}$

  among all incoming neighbours i_j (input to a particular gate) of i_k
- Combining this calculation with topological sort and iterating for each node gives us the longest path in our DAG representation of the circuit.

Conclusion :

The code gives the output of the the longest path of the Directed Acyclic graphical representation of our combinational circuit, by which we can determine the latency, which helps in Scheduling resources with time constraints .