Image Transfer and Software Defined Radio using USRP and GNU Radio

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Software Defined Radio

» It is a general term referring to any radio design that uses a computer and some controlling software to “define” that radio’s operation.

Why SDR ?

3

» Flexibility

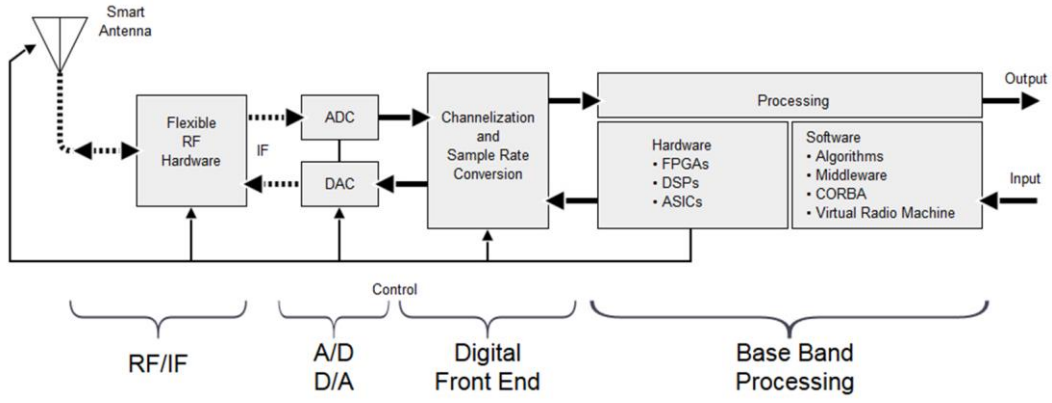
» Filtering - modify

» Modes of operation- can change

» Functions controlled in Software instead of Hardware

SDR Set-Up

4



GNU Radio

5

» A Development Toolkit That Provides Signal Processing Blocks To Implements (Define) Software Radios.

Why GNU Radio ?

6

» Free & Open Source Software

» Work on Both C++ & Python

» Offers Scalability

» Provides Library of standard algorithms

» Large set of example provided by Developer

Working of GNU Radio

7

» Generate a Python file for each processing block.

» Modified each file to fit the needs of the developer

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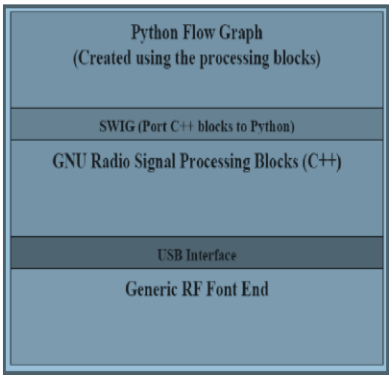
» Signal processing blocks are implemented in C++ classes.

» SWIG (Simplified Wrapper and Interface Generator) is a Linux package that converts the C++ classes to compatible Python classes.



USRP

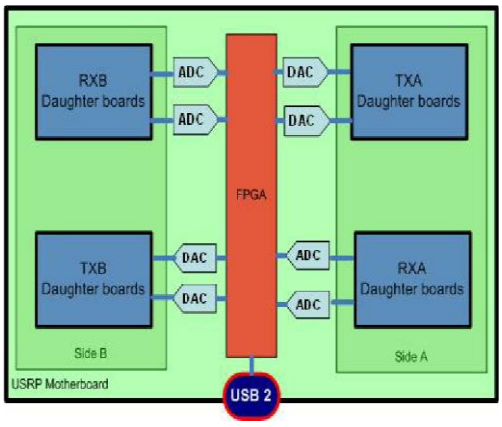
8

» FPGA, ADCs/DACs, and a USB controller

»All signal processing done on host CPU

»All high speed operations (decimation/interpolation) are done on the FPGA

»Daughter-boards perform transmit/receive operations

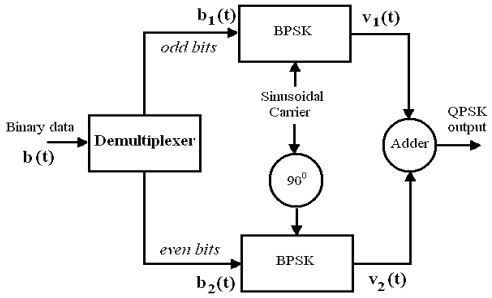


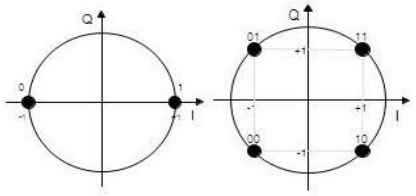
Modulation

9

1. Binary Phase Shift Keying

Phase-Reversal Keying
Phase shifts of ± 180°





2. Quaternary Phase Shift Keying

Phase shifts of 0, 90, 180, 270
or 45, 135, 225, 315

Forward Error Correction

10

Forward Error Correction (**FEC**) or **Channel Coding** is a technique used for controlling errors in data transmission over unreliable or noisy communication channels.

Solution : Hamming Code

Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors.

Methodology

11

STAGE 1 – Simulation

» Modulate/encode and demodulate/decode the image data all within GRC

STAGE 2 – Wireless(less)

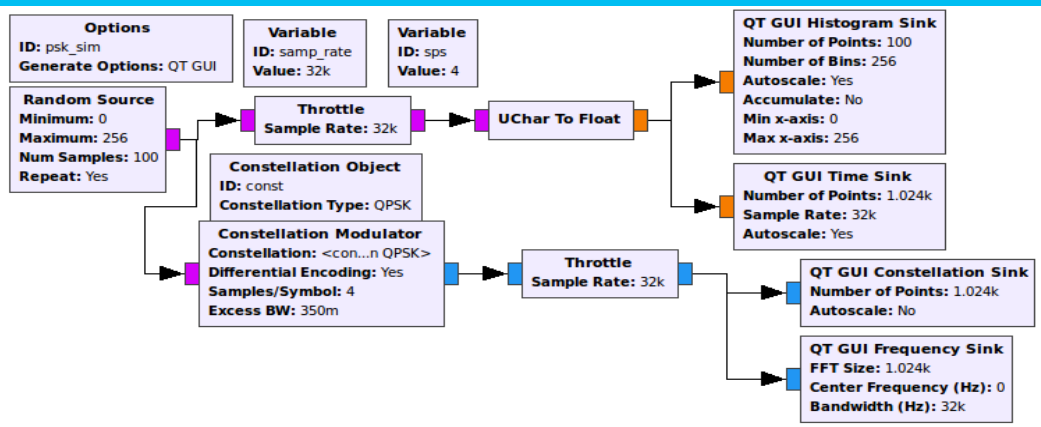
» File transfer between USRPs using a loop back cable

STAGE 3 – Wireless

» Comparison of modulation schemes, with and without FEC, and at different distances

Simulated Baseband Modulation

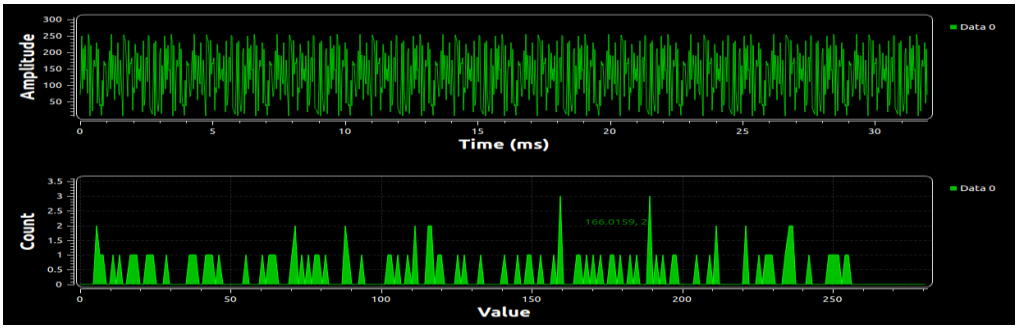
12



Input Signal

13

»Oscilloscope
»Histogram

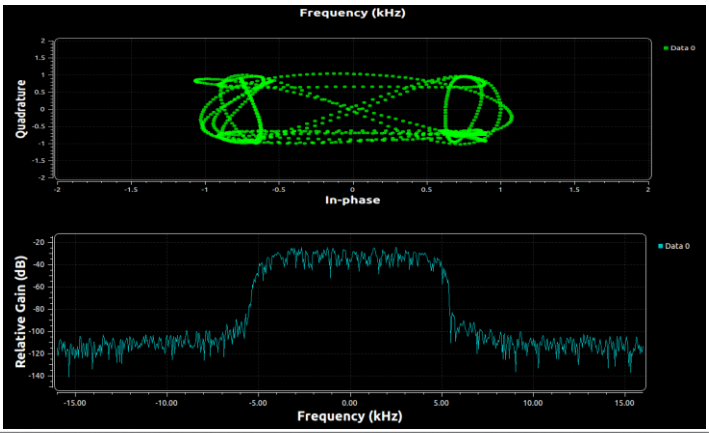


Modulated signal

14

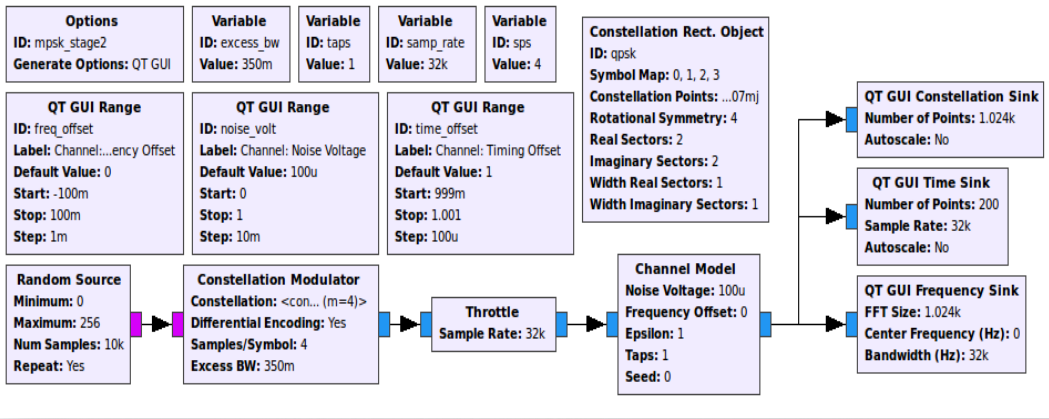
Constellation

Frequency Spectrum



Simulation with Transmission Channel

15



Channel effects

16

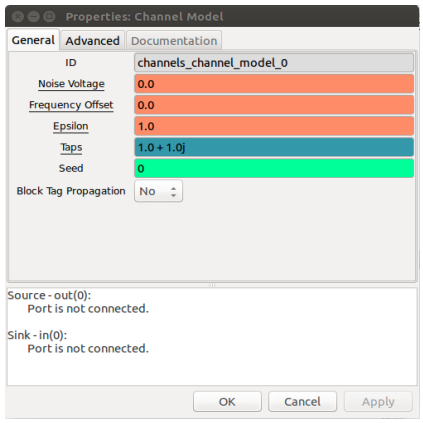
1. ~~Amplitude Attenuation~~

2. ~~Timing~~

3. Frequency Drift

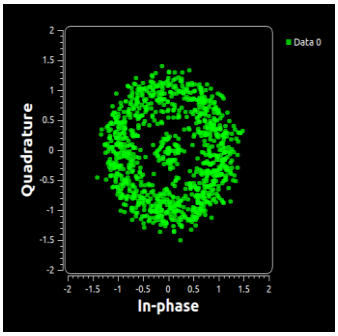
4. Additive White Gaussian Noise(AWGN)

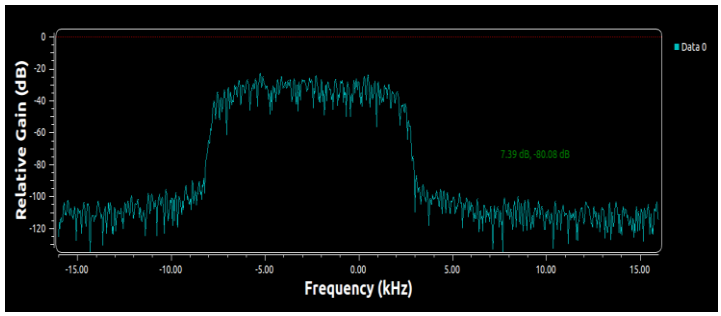
5. Inter Symbol Interference (ISI)



Frequency Distortion

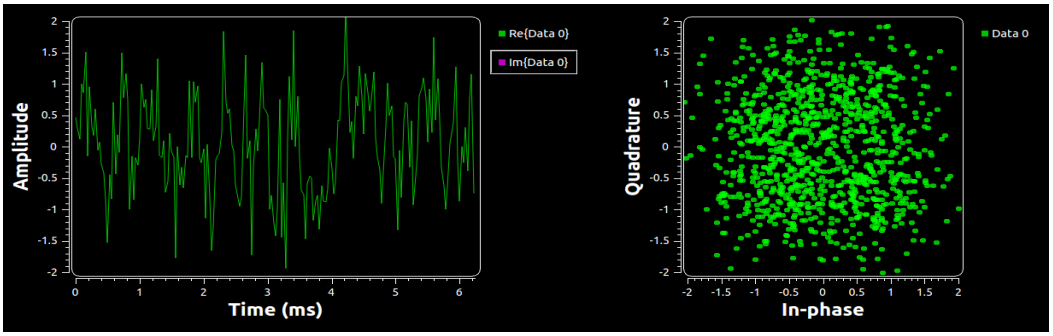
17





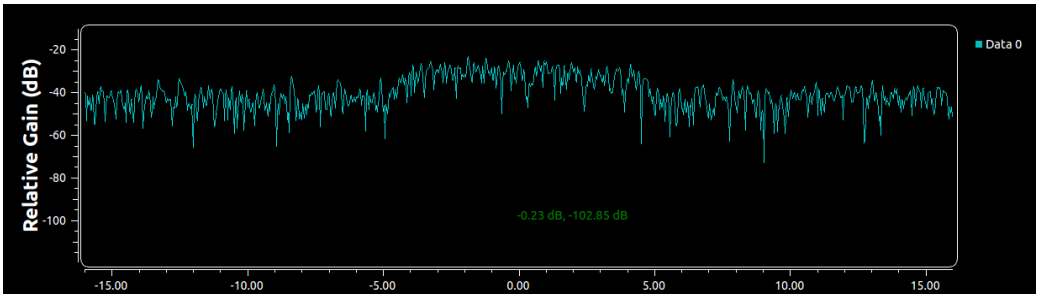
Noise distortion

18



Noise distortion

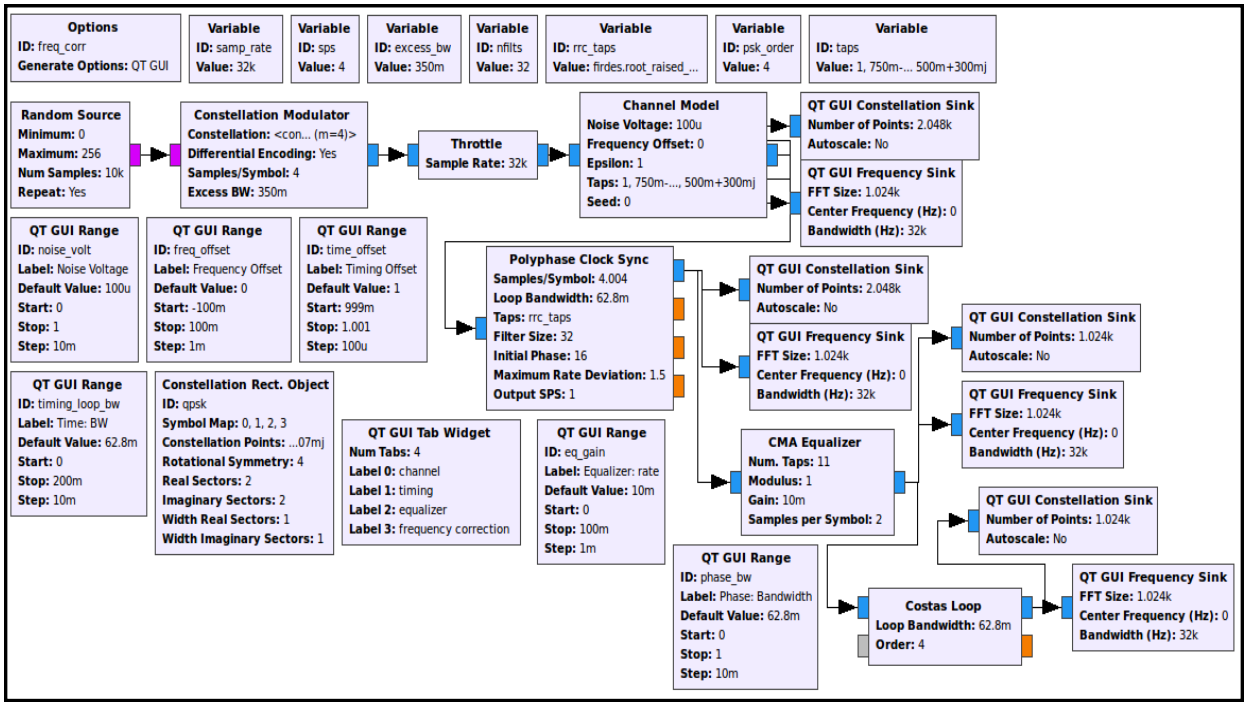
19



20

1.

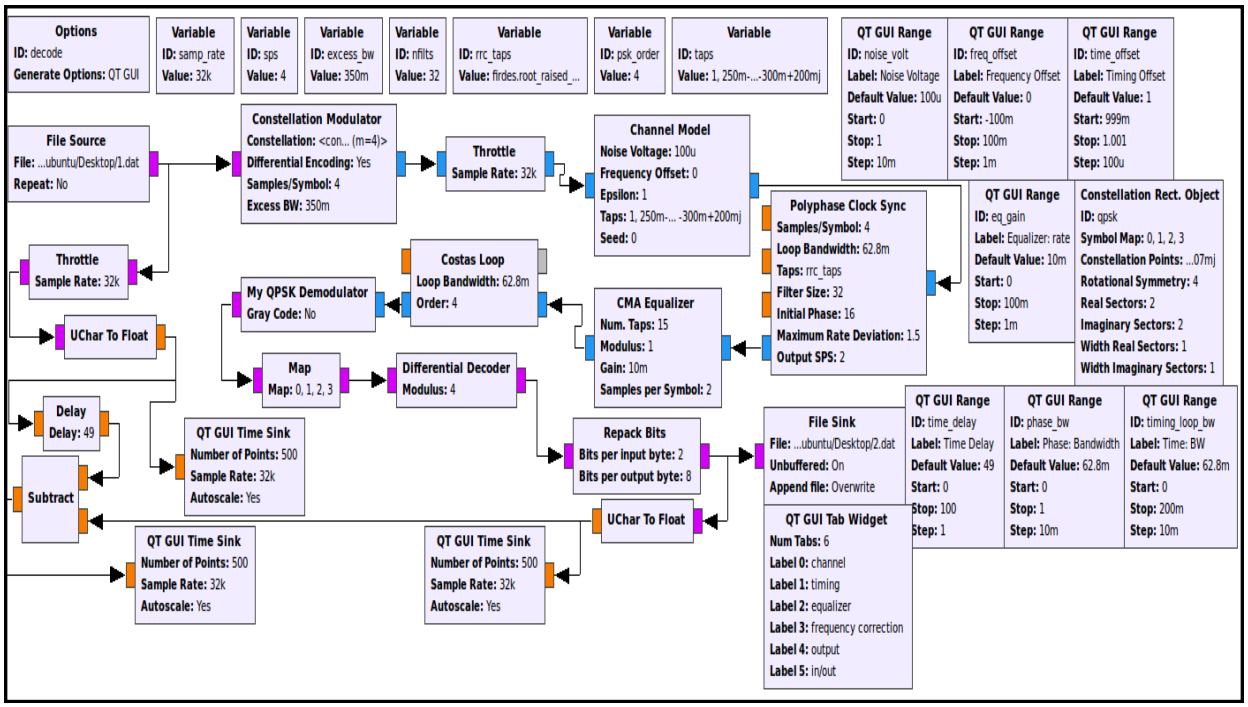
Simulation with Demodulation

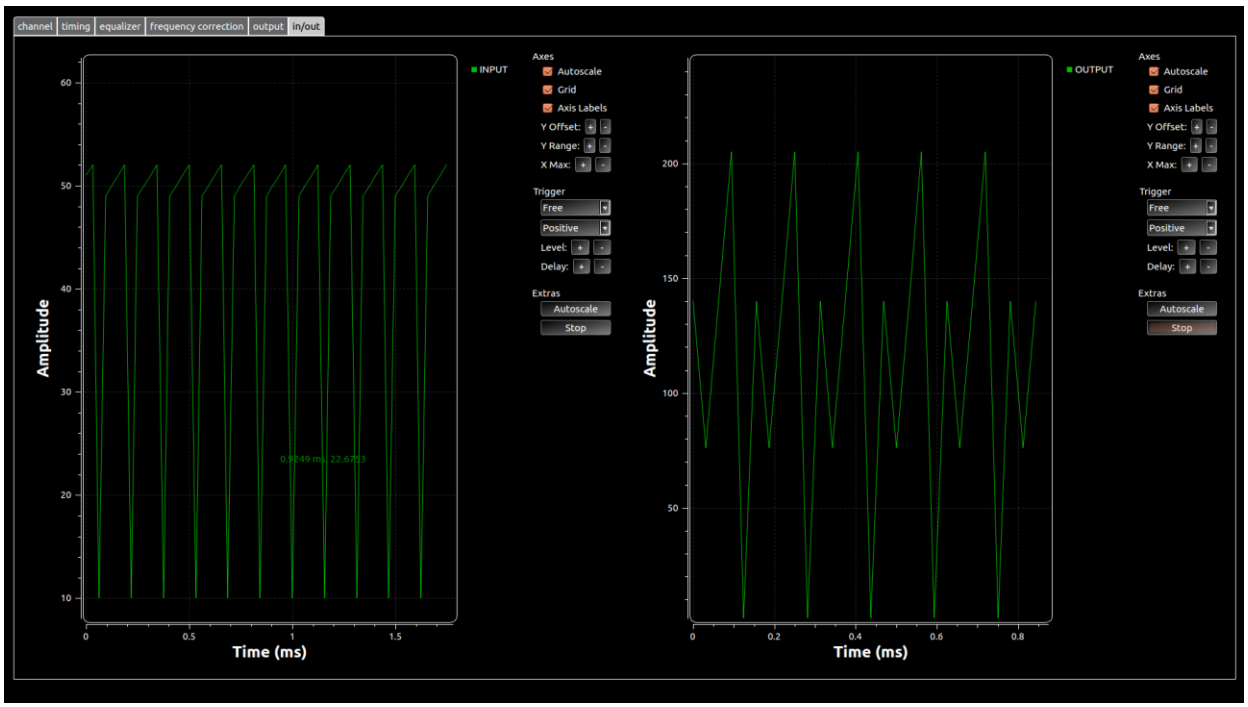


22

2.

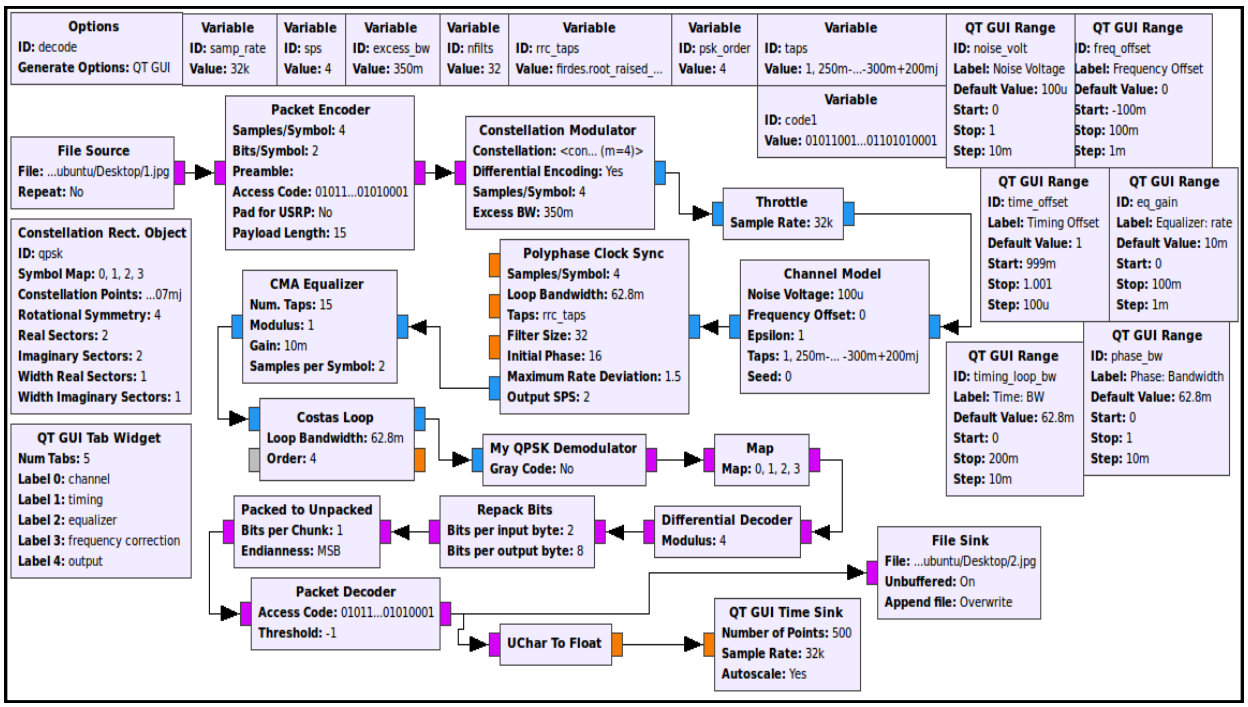
Simulation with Decoding

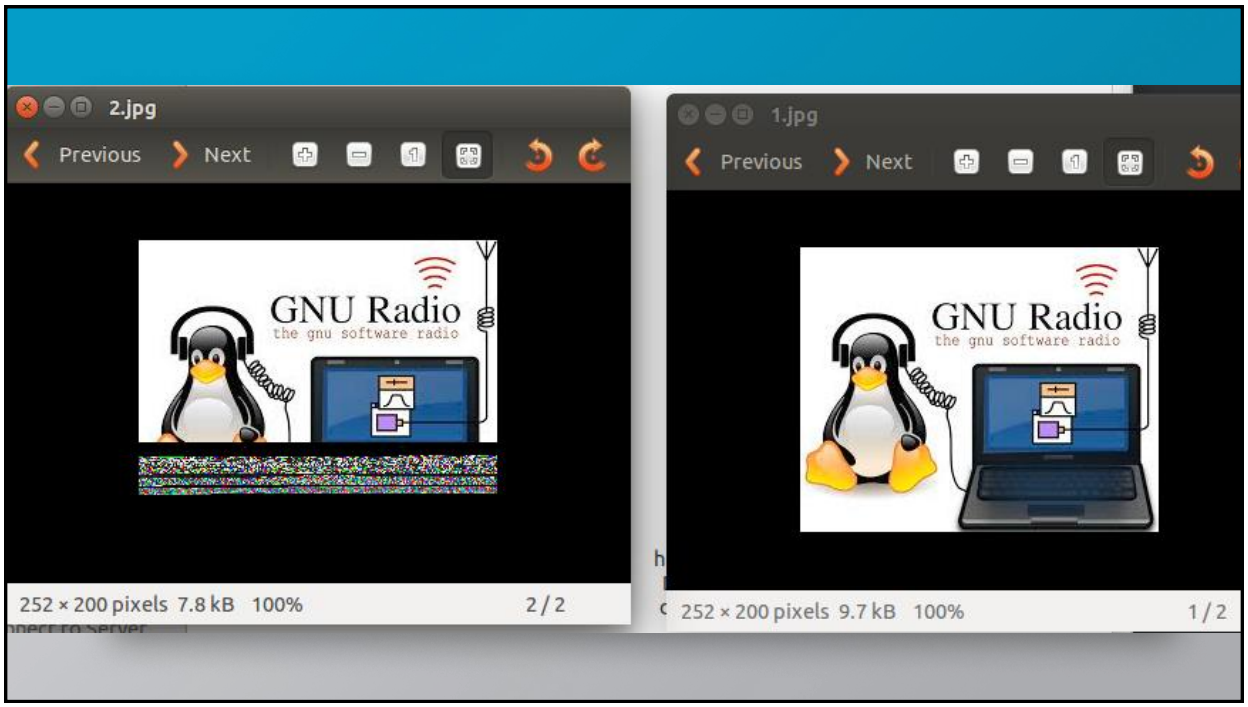

Options
ID: decode
Generate Options: QT GUI
Variable
ID: samp_rate
Value: 32k
Variable
ID: sps
Value: 4
Variable
ID: excess_bw
Value: 350m
Variable
ID: nfilts
Value: 32
Variable
ID: rrc_taps
Value: firdes.root_raised_...
Variable
ID: psk_order
Value: 4
Variable
ID: taps
Value: 1, 250m-...-300m+200mj
QT GUI Range
ID: noise_volt
Label: Noise Voltage
Default Value: 100u
Start: 0
Stop: 1
Step: 10m
QT GUI Range
ID: freq_offset
Label: Frequency Offset
Default Value: 0
Start: -100m
Stop: 100m
Step: 1m
QT GUI Range
ID: time_offset
Label: Timing Offset
Default Value: 1
Start: 999m
Stop: 1.001
Step: 100u
File Source
File: ...ubuntu/Desktop/1.dat
Repeat: No
Constellation Modulator
Constellation: <con... (m=4)>
Differential Encoding: Yes
Samples/Symbol: 4
Excess BW: 350m
Throttle
Sample Rate: 32k
Channel Model
Noise Voltage: 100u
Frequency Offset: 0
Epsilon: 1
Taps: 1, 250m-... -300m+200mj
Seed: 0
Polyphase Clock Sync
Samples/Symbol: 4
Loop Bandwidth: 62.8m
Taps: rrc_taps
Filter Size: 32
Initial Phase: 16
Maximum Rate Deviation: 1.5
Output SPS: 2
QT GUI Range
ID: eq_gain
Label: Equalizer: rate
Default Value: 10m
Start: 0
Stop: 100m
Step: 1m
Constellation Rect. Object
ID: qpsk
Symbol Map: 0, 1, 2, 3
Constellation Points: ...07mj
Rotational Symmetry: 4
Real Sectors: 2
Imaginary Sectors: 2
Width Real Sectors: 1
Width Imaginary Sectors: 1
Throttle
Sample Rate: 32k
UChar To Float
Costas Loop
Loop Bandwidth: 62.8m
Order: 4
My QPSK Demodulator
Gray Code: No
CMA Equalizer
Num. Taps: 15
Modulus: 1
Gain: 10m
Samples per Symbol: 2
Map
Map: 0, 1, 2, 3
Differential Decoder
Modulus: 4
Delay
Delay: 49
Subtract
QT GUI Time Sink
Number of Points: 500
Sample Rate: 32k
Autoscale: Yes
Repack Bits
Bits per input byte: 2
Bits per output byte: 8
File Sink
File: ...ubuntu/Desktop/2.dat
Unbuffered: On
Append file: Overwrite
QT GUI Range
ID: time_delay
Label: Time Delay
Default Value: 49
Start: 0
Stop: 100
Step: 1
QT GUI Range
ID: phase_bw
Label: Phase: Bandwidth
Default Value: 62.8m
Start: 0
Stop: 1
Step: 10m
QT GUI Range
ID: timing_loop_bw
Label: Time: BW
Default Value: 62.8m
Start: 0
Stop: 200m
Step: 10m
QT GUI Time Sink
Number of Points: 500
Sample Rate: 32k
Autoscale: Yes
UChar To Float
QT GUI Time Sink
Number of Points: 500
Sample Rate: 32k
Autoscale: Yes
QT GUI Time Sink
Number of Points: 500
Sample Rate: 32k
Autoscale: Yes
QT GUI Tab Widget
Num Tabs: 6
Label 0: channel
Label 1: timing
Label 2: equalizer
Label 3: frequency correction
Label 4: output
Label 5: in/out


channel
timing
equalizer
frequency correction
output
in/out
INPUT
OUTPUT
Axes
Autoscale
Grid
Axis Labels
Y Offset:
Y Range:
X Max:
Trigger
Free
Positive
Level:
Delay:
Extras
Autoscale
Stop
Amplitude
Time (ms)

3.

Completed Simulation

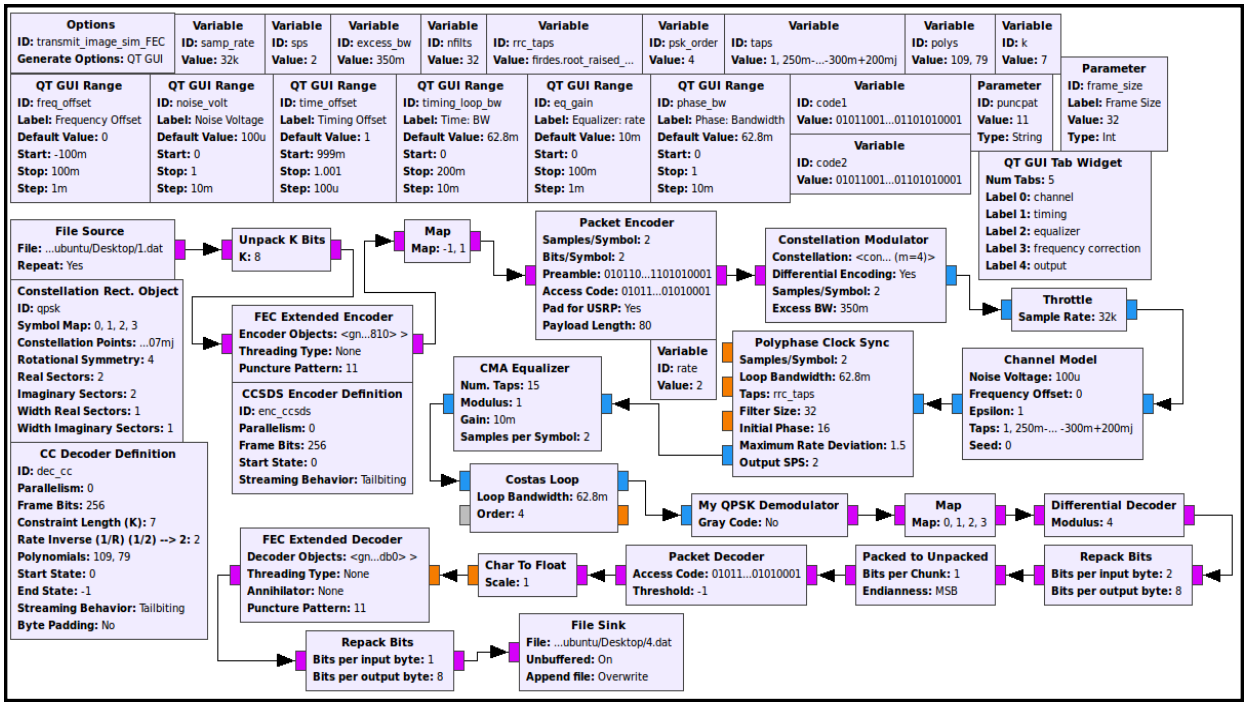




28

4.

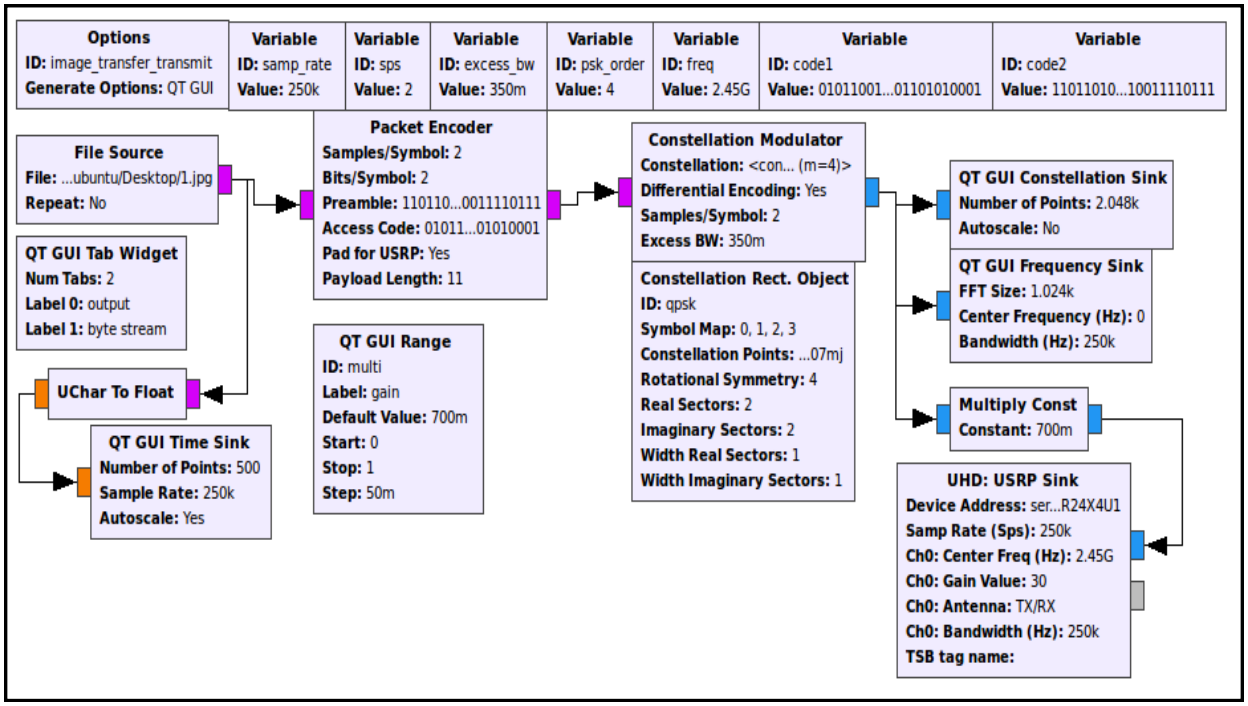
Simulation with Error Correction



30

5.

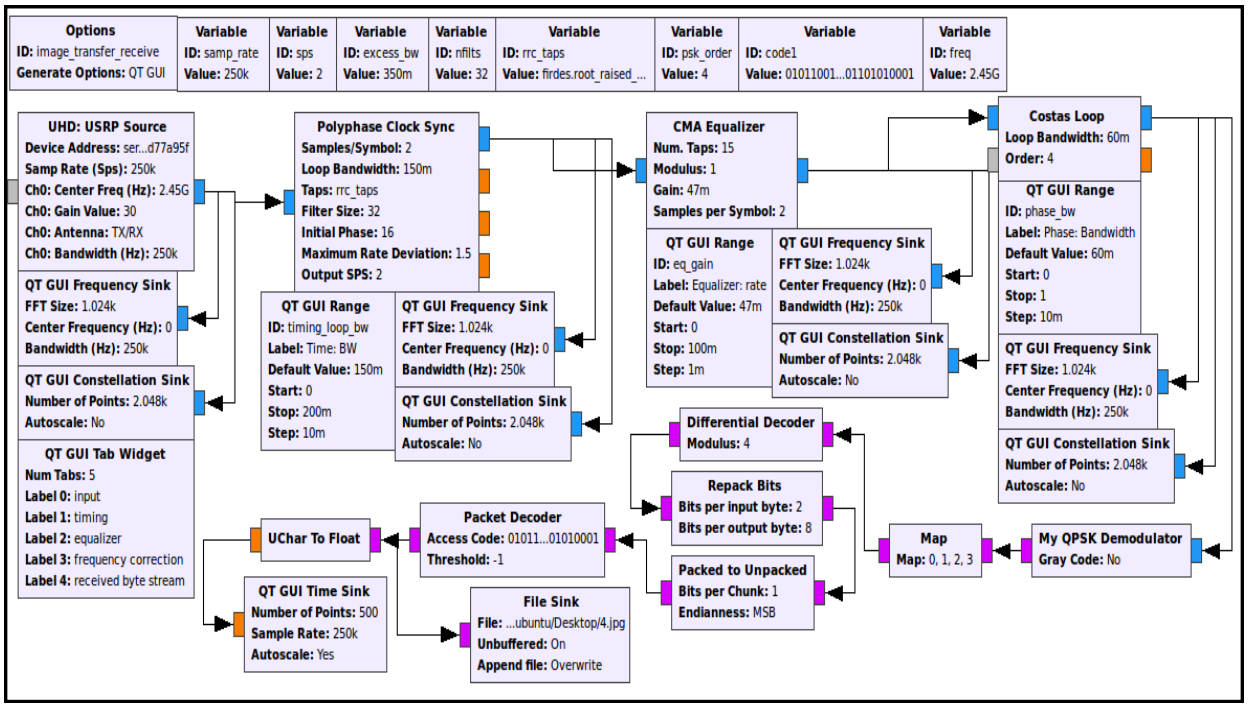
Transmitter with hardware



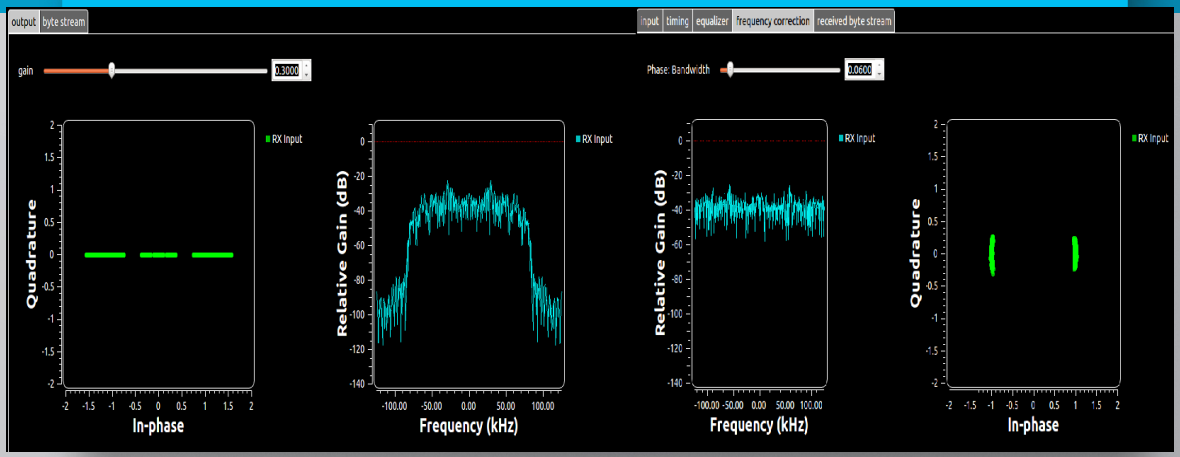
32

6.

Receiver with Hardware

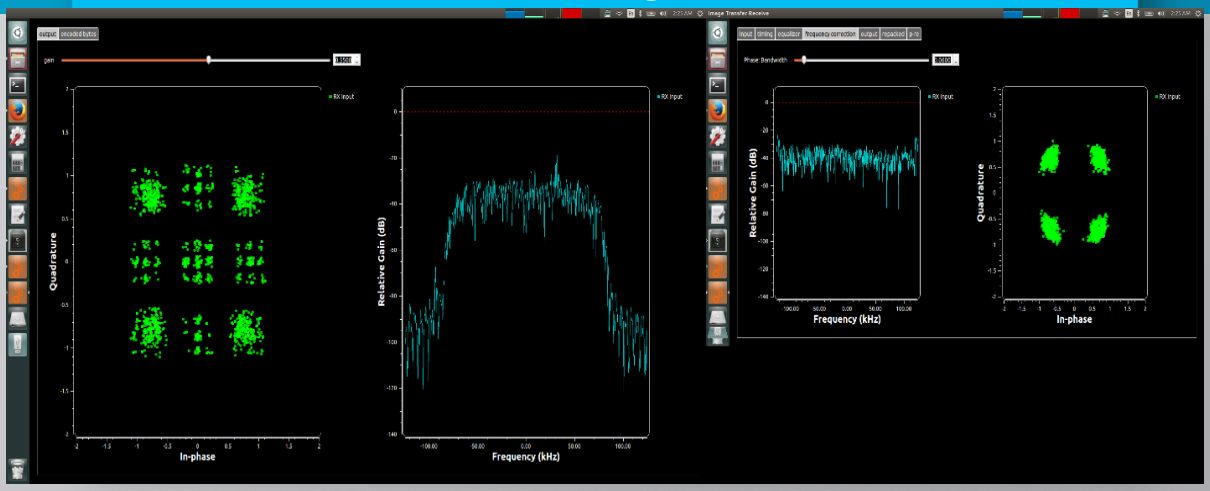


Transmit/Receive with BPSK



Transmit/Receive with QPSK

35



Results and Conclusions

36

1. Simulation - Image transfer was error free

2. With Hardware – roughly 75% success rate using very large pre-amble

3. FEC was ineffective due to burst errors

4. Interleaving was a more appropriate solution

37

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Thank You..!!!

Questions ??