AMIT LAKNAUR

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Professional Summary

A successful track record from **inception** to the **deployment** for many test solutions and measurement tools with **captivating UX** which reached **200% of target** users.
Good at evangelizing product ideas and garnering leadership support and approvals.
Proven success in leading cross-functional teams to deliver exciting software products and achieve key operational goals. And have helped by saving several $100K.
Pre-sales customer (CM/OEM) facing product and support demos resulting in **design wins**.
More info @ **https://amitlaknaur.github.io/**
Talented product manager with demonstrated record of success in marketing management and campaign development. Successful at overseeing all stages of initiatives, building positive relationships and promoting products with innovative and forward-thinking approaches. Well-versed in tracking institutional needs and working for them.

Skills

- Efficient and systematic product development
- Data collection and analysis
- Budgeting and Allocation
- Client communication
- Research and trend analysis
- Matlab, Perl
- Processes building and Optimization
- Methodology and plan development
- Leadership

Work History

Principal Engineer

Nov 2016 - May 2019

Broadcom Ltd — San Jose, CA

- Defined and analyzed metrics to measure product robustness performance and helped push data sheet entries within critical timeframes
- Designed, developed elaborate automation tools from scoping, planning, resource management and intuitive reporting with sorted charts and plots. This work resulted in high-efficiency tools
- Supported Agile product development and iterative UX design for a web-based data analysis tool
- Developed detailed product requirements and user stories based upon user research, led prioritization
- Test and Measurement Equipment evaluation and putting together an optimal configuration suiting over validation needs and constraints. Presenting the same to upper management with ROI analysis
- Developing debug and validation test plans: Test execution on different functions, their co-ex stress and dependency analysis over PCIe PHY/link

Principal & Lead Engineer

Sep 2015 - Nov 2016

Spectra7 Microsystems Inc. Palo Alto, CA

- Pre-sales customer (CM/OEM) facing product and support demos resulting in design wins
- Managed a technical team for all validation and debug efforts at module, functional and system level: Develop test methodologies, automate and delegate tasks & priorities
- Documenting product development guides for each step of our chip integration into end products for the CM to build stronger confidence in our IP, progress, support, and value
- Provide customer support (CM) from IP to End User product development with overseas teams

Senior Mixed Signal Design Validation Engineer May 2011 - Sep 2015

NVIDIA Corp Santa Clara, CA

- Characterization of the PCIE Gen1/2/3, Display Port, HDMI IO PHY and lead such validation efforts for different two GPU chip programs
- Represented NVIDIA in MIPI CTS workgroups in its SPEC development efforts to keep us proactive in our design/test efforts
- Scouting, evaluating, tailoring and purchasing of simulation and testing tools from different Vendors improving the design workflow. Also includes the ROI discussion for funds for such purchase
- Developed an in-house tool for clock characterization and power-noise measurement at ATE for DFT/PI testing, which sped up the flow by 50 times

Mixed Signal Design Validation Engineer Apr 2008 - Apr 2011

NVIDIA Corp Santa Clara, CA

- Developed DSP tool (Matlab and Perl) to carry out the Electrical tests of Display interfaces (Display port, DVI, HDMI) which is also a cross functional effort
- Represented NVIDIA in PCIE Gen3 test development with PCI-SIG in the test working group
- Matlab scripts for Isolating Jitter components in signals and root causing noise source issues at macro and system level
- Lead our group in a Chip bring-up (power-up) effort for Analog Validation
- Characterization of the PCIE Gen1/2, DVI, MLS analog PHY and give feedback to the design team with findings to better next-generation designs and their testability

Education

Ph.D.: **Electrical & Computer Engineering** 2010

Southern Illinois University Carbondale Carbondale, IL

Thesis titled: "Online and built-in self-testing techniques for Field Programmable Analog Array"

Master of Science: **Electrical & Computer Engineering**

Southern Illinois University Carbondale Carbondale, IL

Bachelor of Engineering: **Electrical, Electronics Engineering**

Chaitanya Bharati Institute of Technology (CBIT), Osmania University Hyderabad

Selected Publications

[1] Bonita BHASKARAN (NVIDIA), Amit SANGHANI (Nvidia), Kaushik NARAYANUN (NVIDIA), Ayub ABDOLLAHIAN (Nvidia), Amit LAKNAUR (NVIDIA) Test Method and Scheme for Low-Power Validation in Modern SOC Integrated Circuits. VLSI Testing Symposium 2016 (VTS16').
[2] A. Laknaur, R. Xiao, and H. Wang "Design of a Window Comparator with Adaptive Error Threshold for Online Testing Applications," International Symposium on Quality Electronic Design 2007(ISQED07'), has won Best Paper Award.
[3] A. Laknaur, R. Xiao, and H. Wang "A Programmable Window Comparator for Analog Online Testing," VLSI Testing Symposium 2007 (VTS07').
[4] A. Laknaur, R. Xiao, and H. Wang "An Analog Checker with Programmable Adaptive Error Thresholds," 2007 IEEE Instrumentation and Measurement Technology Conference IMTC07'