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Computer Science Engineering(CS)

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MULTIPLE SUBJECT : COMPUTER ORGANISATION AND ARCHITECTURE + OPERATING SYSTEM (GATE-2019) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(33) | CORRECT(0) | INCORRECT(0) | SKIPPED(33)

Q. 1

Consider a modified 8-bit floating point representation in which 1-bit for sign, 3-bit for exponent and 4-bit for significant.
What will be representation for decimal value –12?

Solution Video | Have any Doubt ?

A 11111000

B 11101000 — Correct Option

Solution :
(b)

Given decimal = –12

Number is negative, so sign bit = 1

Sign	Exponent	Significant
1-bit	3-bit	4-bit

- Now express 12 in binary form : 1100
  Normalized form = 1.100×2^3
- For 3-bit exponent field, a bias of $(2^{3-1} - 1 = 3)$ is used.
- Add the bias to the exponent = 3 + 3 = 6 = $(110)_2$

Hence result will be

1	110	1000
Sign	Exponent	Significant

Hence option (b) is correct.

C 11110000

D 11111100

QUESTION ANALYTICS +

Q. 2

Consider the following program segment:

```
    fork ( );
printf ("Hello");
    fork ( );
printf ("GATE2019");
    fork ( );
```

How many times Hello and GATE2019 will be printed?

Solution Video | Have any Doubt ?

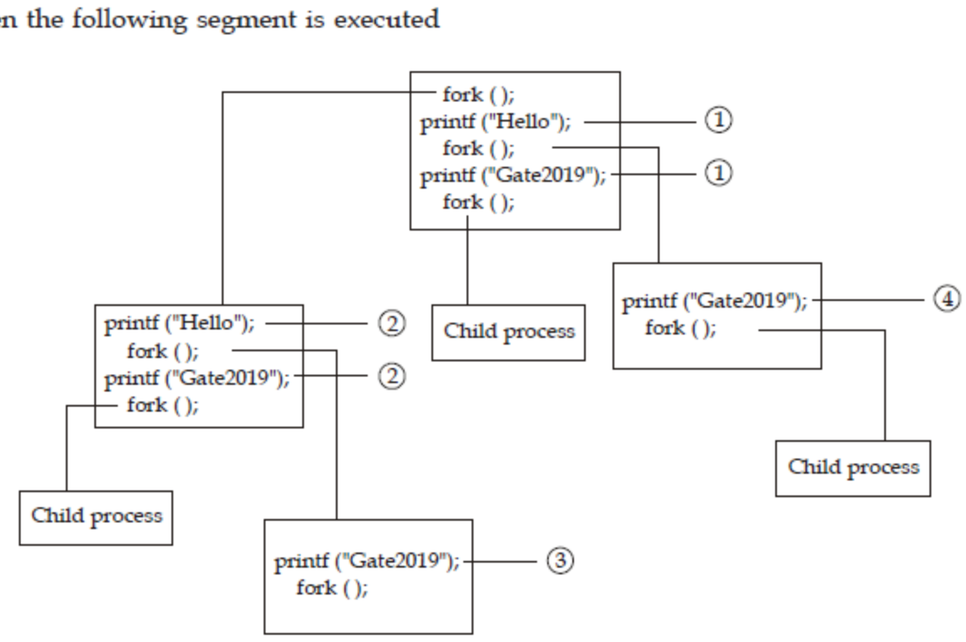
A 4, 2

B 2, 4 — Correct Option

Solution :
(b)

fork system call used for creating a new process, which is called a child process, after a new child process created, both processes (child and parent) will execute the next instruction following the fork ( ) system call.

When the following segment is executed



Hello is printed 2 time and GATE 2019 is printed 4 time.
Hence option (b) is the answer.

C 3, 2

D 2, 2

QUESTION ANALYTICS +

Q. 3

Assume a processor supports both conditional and un-conditional branch instructions. Below are given conditional and un-conditional statements. Which of the following satisfies unconditional target address?
(i) JMP
(ii) Do-while
(iii) Switch statement
(iv) Halt

Solution Video | Have any Doubt ?

A Only (i) and (ii)

B Only (ii) and (iii)

C Only (i) and (iv) Correct Option

Solution :
(c)
• JMP and Halt are unconditional instruction.
• Do-while and Switch statement are conditional.

D Only (iv)

QUESTION ANALYTICS +

Q. 4

Consider a 2-level L_1 and L_2 memory hierarchy system. The associativity of L_1 towards processor is more. L_1 (cache) has accessing time of 15 ns and L_2 (main memory) has an accessing time of 100 ns. Writing takes 30 ns for L_1 and 150 ns for L_2. Assume 30% read misses in L_1 memory. 50% of the program instructions are read only instructions. What is the average access time for the system if it uses write through protocol?

Solution Video | Have any Doubt ?

A 100.5 ns

B 102.75 ns

C 95.25 ns Correct Option

Solution :
(c)

In write through protocol CPU writes in both cache and main memory. Writing time of main memory is high so this is considered.

$$T_{read} = 0.7 \times 15\text{ ns} + 0.3 \times 100\text{ ns}$$
$$= 10.5\text{ ns} + 0.3 \times 100\text{ ns}$$
$$= 10.5\text{ ns} + 30\text{ ns}$$
$$= 40.5\text{ ns}$$
$$T_{write} = 150\text{ ns} \quad (H_w = 1, \text{Simultaneous organization})$$

Now,
$$T_{avg} = F_{read} \times T_{read} + F_{write} \times T_{write}$$
$$= 0.5 \times 40.5\text{ ns} + 0.5 \times 150\text{ ns}$$
$$= 20.25\text{ ns} + 75\text{ ns}$$
$$= 95.25\text{ ns}$$

D 105.67 ns

QUESTION ANALYTICS +

Q. 5

Consider a main memory with three page frames and the following sequence of page reference 1, 2, 3, 4, 2, 1, 5, 6, 1, 2, 3, 4, 1, 2 which of the following is true with respect to page replacement policies Least Recently Used (LRU) and optimal page replacement?

Solution Video | Have any Doubt ?

A Both incurs the same number of page faults.

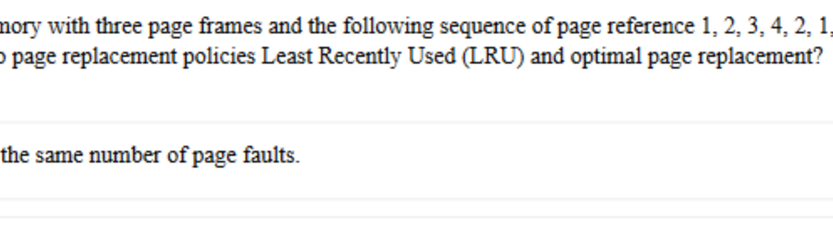
B LRU incurs 3 more page fault than optimal page replacement.

C LRU incurs 4 more page faults than optimal page replacement. Correct Option

Solution :
(c)

Page reference string 1, 2, 3, 4, 2, 1, 5, 6, 1, 2, 3, 4, 1, 2 LRU replace the page which is least recently used.

Total 12 page fault in LRU.
Optimal page replacement, replace the page which is not going to used in near future reference.



Total 8 page fault in optimal page replacement.
So LRU incurs 4 more page fault than optimal page replacement algorithm.
So option (c) is correct.

D LRU incurs 2 more page fault than optimal page replacement.

QUESTION ANALYTICS +

Q. 6

Consider the statement given below:
S_1 : Dirty bit in page table entry is used for reference count.
S_2 : Valid bit in the page table entry is used for page availability check.
Which of the following are correct?

Solution Video | Have any Doubt ?

A Both S_1 and S_2

B Only S_1

C Only S_2 Correct Option

Solution :
(c)
S_1 : Dirty bit is used to check for modified pages not for reference count.
S_2 : Valid bit used to check the availability of pages in the main memory. If it is valid it is directly used and if it is not valid a fresh page is loaded in memory.
So correct option is (c).

D Both statement are false

QUESTION ANALYTICS +

Q. 7

Assume a hypothetical processor uses a fixe 16-bit instruction length. The operand size are 6 bits. There are K 2-operand instructions and L 1-operand instructions. What is the maximum number of zero operand instructions that can be supported by this processor.

Solution Video | Have any Doubt ?

A $(((2^4 - K) \times 2^6) - L) \times 2^6$ Correct Option

Solution :
(a)
Number of 2-operand instructions = K
Number of 1-operand instructions = L
So, number of zero operand instructions $(((2^4 - K) \times 2^6) - L) \times 2^6$.

B $(2^{16} - (K \times 2^6 \times 2^6) - L)/2^6$

C $(2^{16} + K \times 2^6 \times 2^6 - L) \times 2^6$

D Not possible

QUESTION ANALYTICS +

Q. 8

Consider the following program segment, we want to synchronize two concurrent process P and Q using semaphore X = 1, Y = 0.

```
void Process P1                 void Process P2
{                               {
    while (1)                       while (1)
    {                               {
        P(X);                           P(X);
        print ("1");                    print ("0");
        P(Y);                           V(X);
    }                                   V(Y);
}                                   }
                                }
```

(While P and V are the usual semaphore operation) what will be the output of the following program segment?

Solution Video | Have any Doubt ?

A It will print 010101 .....

B It will print 001001 .....

C It will print 101010 .....

D None of the above Correct Option

Solution :
(d)
Value of the semaphore X = 1 and Y = 0
If Process P_1 execute first then after executing the P(X), X value become 0 and it will print 1. P(Y) is executed, value of semaphore Y is 0 so Process P_1 is blocked and if Process P_2 started executing, after executing P(X), X value is 0 so Process P_2 is also block this is a deadlock condition.
P_2 can run forever and in that case output will be 00000 .....
So option (d) is correct.

QUESTION ANALYTICS

Q. 9

Assume X and Y represents number of times a processor needs to refer to memory when it fetches and executes an indirect address mode instruction for single operand and for branch respectively. The value of (X – Y) is _____.

Solution Video | Have any Doubt ?

1 Correct Option

Solution :

1

- X represents number of times memory referred for single operand.

$$X = 3 \begin{bmatrix} 1. & \text{Fetch instruction} \\ 2. & \text{Fetch operand reference [EA]} \\ 3. & \text{Fetch operand} \end{bmatrix}$$

- Y represents for branch instruction.

$$Y = 2 \begin{bmatrix} 1. & \text{Fetch instruction} \\ 2. & \text{Fetch from memory and placed EA into PC.} \end{bmatrix}$$

So, $X - Y = 3 - 2 = 1$

QUESTION ANALYTICS

Q. 10

Assume a system has 3 control signals named as S_0, S_1 and S_2, 3 different instructions I_1, I_2 and I_3 and 3 micro-operations T_1, T_2 and T_3. The below table represents controls signals required at different micro-operations for the particular instruction.

μ-operation/instruction	I_1	I_2	I_3
T_1	S_0, S_1	S_0	S_0, S_1, S_2
T_2	S_2	S_2, S_1	S_2
T_3	S_0	S_1	S_2

(i) $S_0 = T_1 + T_3 I_1$
(ii) $S_0 = T_1 (I_1 + I_2) + T_3 I_1$
(iii) $S_1 = T_1 (I_1 + I_3) + T_2 I_2 + T_3 I_2$
(iv) $S_1 = T_1 I_1 + T_2 (I_2 + I_3)$
(v) $S_2 = T_1 I_3 + T_2$

The number of the above control signal equations correct for S_0, S_1 and S_2 are _____.

Solution Video | Have any Doubt ?

2 Correct Option

Solution :

2

Only equation (i) and (iii) for control signal S_0 and S_1 are correct.
Hence answer will be 2.

QUESTION ANALYTICS

Q. 11

Consider the following code:

```
int x = 0;
int y = 0;
f1( )
{
    x = 1;
    y = y + x;
}
f2( )
{
    y = 4
    x = x + 5
}
```

If f_1 and f_2 are executed concurrently by using concurrent program and if the number of different values, x can take is A and y can take is B what is the value of A + B _____. (Do not count $x = 0$ and y = 0)

Solution Video | Have any Doubt ?

5 Correct Option

Solution :

5

When $f_1( )$ is executed first followed by $f_2( )$

$x = 1$
$y = 1$
$y = 4$
$x = 6$

When $f_2( )$ is executed first followed by $f_1( )$

$y = 4$
$x = 5$
$x = 1$
$y = 5$

When $f_1( )$ and $f_2( )$ executing concurrently possible value of x and y.

$x = 1$	$y = 4$	$y = 4$	$y = 4$
$y = 4$	$x = 1$	$x = 1$	$x = 1$
$y = 5$	$x = 6$	$x = 6$	$y = 5$
$x = 6$	$y = 10$	$y = 10$	$x = 6$

x can takes value 1, 6
y can takes value 4, 5, 10
Total different value x can take is 3 and y can take is 4 so

$A + B = 2 + 3 = 5$

QUESTION ANALYTICS

Q. 12

Consider the arrival time and execution time for the following processes (all time in ms):

Process	Arrival time	Execution time
P_0	0	6
P_1	3	5
P_2	3	3
P_3	5	6
P_4	8	3

If processor uses Round Robin scheduling (Time quantum = 2) what is the average waiting time _____ (ms). (Upto 1 decimal place)

Solution Video | Have any Doubt ?

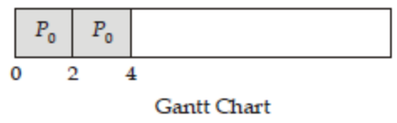
9.8 (9.7 - 9.9) — Correct Option

Solution :

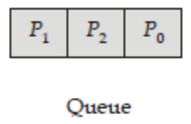
9.8 (9.7 - 9.9)

In Round Robin scheduling algorithm we also maintain a queue.

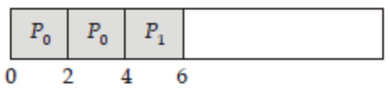
Time quantum = 2 unit



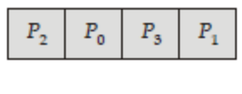
Gantt Chart



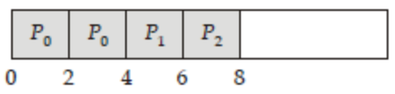
Queue



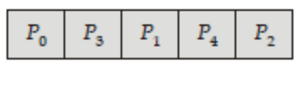
Gantt Chart



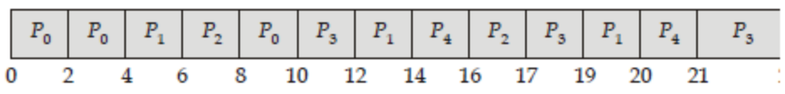
Queue



Gantt Chart



Queue



Waiting time = Turn around time – Execution time

Process	Waiting time
P_0	4
P_1	12
P_2	11
P_3	12
P_4	10

$$\text{Average waiting time} = \frac{\sum_{i=0}(\text{Waiting time of } P_i)}{\text{Number of process}}$$

$$= \frac{4+12+11+12+10}{5} = 9.8 \text{ ms}$$

QUESTION ANALYTICS

Q. 13

Consider the following statements:

S_1 : On per-thread basis, operating system maintain virtual memory state.

S_2: Related Kernel level threads can be scheduled on different processor in a multiprocessor system.

S_3: On pre-thread basis, operating system does not maintain CPU register state.

How many number of statements are true _____.

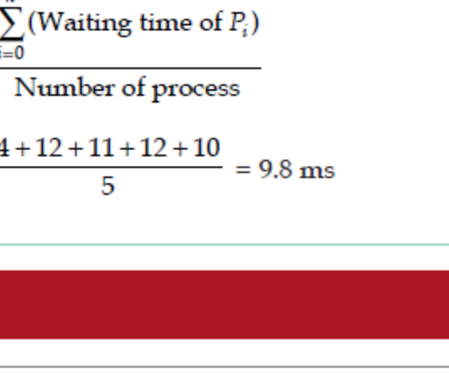
Solution Video | Have any Doubt ?

1 — Correct Option

Solution :

1

S_1: On pre-thread operating system does not maintain virtual memory state. It maintain address space for the process not for threads S_1 is false.



S_2: Kernel level thread schedule by the operating system independently so related Kernel level thread can be scheduled on a different processor in a multiprocessing system. S_2 is true.

S_3: On per thread basis operating system maintain CPU register state and stack. S_3 is false.

QUESTION ANALYTICS

Q. 14

A non-pipelined processor has a clock rate of 2.5 GHz and an average cycle per instruction of 5. An upgrade to the processor produces a five stage pipeline. The clock rate of upgraded processor has been reduced to 2 GHz due to internal pipeline delays. The time saved for executing 1000 instructions on pipelined processor compared to non-pipelined processor in nanoseconds (ns) is _____.

Solution Video | Have any Doubt ?

1498 — Correct Option

Solution :
1498

Cycle time of non-pipelined processor = $\frac{1}{2.5}$ ns = 0.4 ns

To execute 1000 instruction each requiring 5 cycles

Execution time = 1000 × 5 × 0.4 ns
= 2000 ns

Cycle time of upgraded pipeline processor = $\frac{1}{2}$ ns = 0.5 ns

Execution time for n instruction on K-stage pipeline with cycle time t = $(K + n - 1) \times t$
So, time to execute 1000 instruction on 5-stage pipeline will be

= (5 + 1000 – 1) × 0.5 ns
= (5 + 999) × 0.5 ns
= 10004 × 0.5 ns = 502 ns
Time saved = (2000 – 502) ns
= 1498 ns

QUESTION ANALYTICS

Q. 15

A machine has a 32 bit virtual and 32 bit physical address space and a 8 KB page. Assume that the table is entirely in hardware with one 32-bit word per entry. When a process starts, the page table is copied to the hardware from memory, at one word in 100 nsec. If each process runs for 200 msec (including the time to load the page table); what fraction of CPU time is devoted to loading the page table (in percentage) _____. (Only integer part)

Solution Video | Have any Doubt ?

26 — Correct Option

Solution :
26

Number of entries in the page table is $\frac{2^{32}}{2^{13}}$ = 524288

100 ns is needed to load one word from hardware to main memory for 524288 entries it takes
524288 × 100 × 10^{-9} sec = 52.428 ms
If a process gets 200 ms, this consist of 52.428 ms for loading the page table and (200 – 52.428) for executing the process.
CPU devoted time for page table loading is

$$= \frac{52.428}{200} \times 100 = 26.214\% = 26$$

QUESTION ANALYTICS

Q. 16

A processor supports 256 kW of memory and uses memory mapped I/O for I/O PORT. Address to the I/O PORT is assigned when 3 MSB bits of address is high. The number of memory address available for I/O port is _____.

Solution Video | Have any Doubt ?

32768 — Correct Option

Solution :
32768

Given that 256 kW of memory used.

256 kW = $2^8 \times 2^{10}$ W
= 2^{18} W

Whenever 3 MSB bit is high, that is used for I/O port.

$\underbrace{A_{17}A_{16}A_{15}}_{\text{3 MSB bit}}$ $\underbrace{A_{14} \ldots\ldots A_3A_2A_1A_0}_{\text{15 LSB bit}}$

1 1 1 → 2^{15}

When $A_{17}\,A_{16}\,A_{15}$ is high then remaining 2^{15} combinations of memory reserved for I/O PORT.
So, 2^{15} = 32768

QUESTION ANALYTICS

Q. 17

Consider 2^y lines of cache memory uses direct mapping function to map the data. Memory system is organized into 2^z byte blocks. Main memory size is 2^x bytes. What is the tag directory size in the cahce controller (consider the cost of tags only)?

Solution Video | Have any Doubt ?

A $2^y(x - (y + z))$ — Correct Option

Solution :
(a)

	x bit	
TAG	LO	WO
$(x - (y + z))$	y bit	z bit

∴ Tag directory size = $2^y(x - (y + z))$

B $2^x - (y + z)$

C $2^y(x + z)$

QUESTION ANALYTICS

D $2^y(z - (x + y))$

QUESTION ANALYTICS +

Q. 18

Consider the statements given below:
S_1 : FCFS suffers from starvation.
S_2 : Thrashing decreases the degree of multi-programming.
S_3 : The best fit technique for memory allocation ensures the memory will never be fragmented.
Which of the above statements are incorrect?

Solution Video | Have any Doubt ?

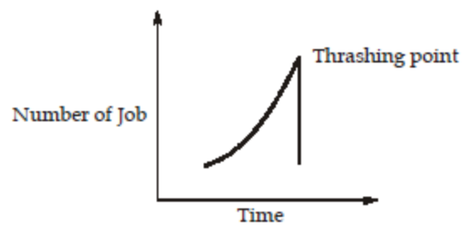
A S_1 and S_3 only

B S_2 and S_3 only

C S_1 and S_2 only

D All S_1, S_2 and S_3 Correct Option

Solution :
(d)
S_1 : FCFS does not suffers from starvation. S_1 is incorrect.
S_2 : In thrashing CPU is spending more time is paging rather than running. CPU efficiency drastically decrease in this situation.



Thrashing implies excessive page I/O not decrease the degree of multiprogramming so S_2 is incorrect.
S_3 : Best fit also suffer from fragmentation so S_3 is incorrect.
All statement is incorrect so option (d) is answer.

QUESTION ANALYTICS +

Q. 19

Consider the following program:

```
boolean block [2];
    int turn;
void entry (int process)
{
    block [process] = true;
    while (turn ! = process) {
        while (block [1-process]);
            turn = process;
    }
    /* critical section */
    block [process] = false;
        /* remainder */
    }
    void main ( )
    {
        block [0] = false;
        block [1] = false;
            turn = 0;
        parbegin (p(0), p(1));
    }
```

Which of the following option is correct?

Solution Video | Have any Doubt ?

A It achieved mutual exclusion and progress.

B It achieved mutual exclusion but not progress.

C It does not achieve mutual exclusion. Correct Option

Solution :
(c)
When we execute the procedure given below:

```
void entry (int process)
{
    block [process] = true;
    while (turn ! = process) {
        while (block [1-process]);
            turn = process;
    }
    /* critical section */
    block [process] = true;
```

Let assume p(1) first executes the entry( ), then it make

```
        block [1] = true;
    while (turn! = process)
```

condition is satisfied turn = 0 and process = 1 it go to second while loop
While (block [1-process]) which is block [1 – 1] = block[0]
Which is FALSE so condition is not satisfied it go to next line but before executing, process is preempted and P(0) get CPU and start executing it make block [0] = true, turn value is 0 and process value is 0 so condition in while loop become false and P(0) go to critical section and

process is preempted.
Then again P(1) get executed from turn = process it make turn = 1 and next time while condition is not satisfied so P(1) also go to critical section.
So mutual exclusion is not satisfied.
So correct option is (c).

D It achieved mutual exclusion but can not prevent deadlock.

QUESTION ANALYTICS +

Q. 20

A processor overflow flag is represented as 0V (a, b, c) where arguments a is MSB of operand 1, b is MSB of operand 2 and c is the MSB of the result after computing a and b. The 0V(a, b, c) of PSW becomes 1 after

Solution Video | Have any Doubt ?

A $a'b'c + a'bc'$

B $a'b'c + abc'$ Correct Option

Solution :
(b)
Overflow flag is active when there is a carry into the MSB and No carry out of MSB or vice-versa.

MSB of operand 1 (a)	MSB of operand 2 (b)	MSB of result (c)	Overflow
0	0	0	0
0	0	1	(1)
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	(1)
1	1	1	0

So, whenever $a'b'c + abc'$, overflow flag is active.
Hence, option (b) is correct.

C $ab'c' + ab'c$

D $a'b'c + abc$

QUESTION ANALYTICS +

Q. 21

Which of the following statements about IO modes are correct?

Solution Video | Have any Doubt ?

A CPU takes care of the IO operation in the programmed IO modes because the IO devices are directly connected to the system bus.

B DMA module has direct access to the main memory and control over the system bus for transfer of the data.

C DMA is efficient for transferring bulk amount of data and programmed IO of small amount of data transfer.

D All of the above Correct Option

Solution :
(d)
All of the above statements are correct.

QUESTION ANALYTICS +

Q. 22

Consider the following preemptive priority scheduling algorithm based on dynamically changing priorities, larger priority numbers imply higher priority. When a process is waiting for CPU its priority changes at a rate of a, when it is running, its priority changes at a rate b. All process are given a priority of 0 when they enter the ready queue. What is the algorithm that results from $a < b < 0$?

Solution Video | Have any Doubt ?

A FCFS (First Come First Serve)

B LIFO (Last In First Out) Correct Option

Solution :
(b)
All process have initial priority 0 when they enter into the ready queue.
When a process is waiting for CPU priority changes at a rate of a and when it is running it changes at rate b but $a < b < 0$ so when the process enter into the ready queue and assign a priority 0 has the highest priority, so a process enter into last in ready queue has processed first so it follow last in first out order.
So correct option is (b).

C SJF (Shortest Job Remaining First)

D None of these

QUESTION ANALYTICS +

Q. 23

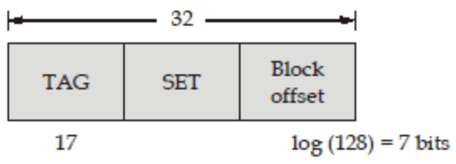
Consider m-way set associative cache with 32-bit addresses and having block size 128 Bytes. If cache memory has 1024 blocks and TAG bits are 17, then what is the number of sets and associativity of cache?

Have any Doubt ?

A 128 sets, 8-way set associativity

B 256 sets, 4-way set associativity — Correct Option

Solution :
(b)



$$\text{Number of sets bits} = 32 - (17 + 7)$$
$$= 32 - 24 = 8$$

i.e. 256 sets are present.
Since number of block in cache = 1024

$$\text{So, Associativity} = \frac{2^{10}}{m} = 2^8$$
$$m = 2^{10-8}$$
$$m = 4$$

So, 256 sets and 4-way set associative.

C 256 sets, 8-way set associativity

D Cannot be determined

QUESTION ANALYTICS

Q. 24

An operating system uses the Banker's algorithm for deadlock avoidance, when managing the allocation of three resource types A, B and C to processes P_0, P_1, P_2, P_3, P_4 the table below represent the current system state.

Process	Current allocation			Maximum need			Available		
	A	B	C	A	B	C	A	B	C
P_0	0	2	0	8	5	3	3	2	2
P_1	2	0	0	3	2	2			
P_2	3	0	2	9	0	2			
P_3	2	1	1	2	2	2			
P_4	0	0	2	4	3	3			

Solution Video | Have any Doubt ?

A System is not in the safe state.

B The system is in the safe state and process is executed in the sequence of P_3, P_1, P_0, P_4, P_2.

C The system is in the safe state and process is executed in the sequence of P_1, P_2, P_3, P_0, P_4.

D The system is in the safe state and process is executed in the sequence of P_1, P_3, P_2, P_0, P_4. — Correct Option

Solution :
(d)
Current need of all process and available resource is:

Process	Current need			Available		
	A	B	C	A	B	C
P_0	8	3	3	3	2	2
P_1	1	2	2			
P_2	6	0	0			
P_3	0	1	1			
P_4	4	3	1			

(a) System is in the safe state so option (a) is not correct.
(b) $P_3(0, 1, 1)$ it can be satisfied with available resources (3, 2, 2), P_1 need is (1, 2, 2) after executing the process P_3 available resources are (3 + 2, 2 + 1, 2 + 1) = (5, 3, 3) because P_3 currently hold (2, 1, 1) P_1 in also executed as available instance of resources (5, 3, 3) are greater than P_1 current need.
Now available instances of resources are (7, 3, 3) P_0 can not be executed as its current need of instance of resource A is 8 and available is 7 so this sequence is not possible.
(c) $P_1(1, 2, 2)$ is executed as available instances of resources is (3, 2, 2).
Now available resource are (5, 2, 2) because P_1 currently hold (2, 0, 0) instances of resources current need of $P_2(6, 0, 0)$ but available instances of resources are (5, 2, 2) so this can not be satisfied, so this sequence is also not possible.
(d) P_1 is executed (1, 2, 2) and now available resources are (5, 2, 2), P_3 current need is (0, 1, 1) so P_3 is also executed and now available resources are (7, 3, 3), P_2 current need is (6, 0, 0) P_2 is also executed as its current need is (6, 0, 0).
Now available resources are (10, 3, 5) because P_2 are currently holds (3, 0, 2), P_0 is also executed because it current need is (8, 3, 3) and P_4 is also executed, sequence for executing is P_1, P_3, P_2, P_0, P_4.

So correct option is (d).

QUESTION ANALYTICS

Q. 25

Consider a machine with 26-bit virtual address space. If the size of the page table entry is 4B what is the page size (in KB) if the machine uses single level page table _____? (Assume that page table will fit in one page in a single level paging)

Solution Video | Have any Doubt ?

16 — Correct Option

Solution :
16

Page table size = Number of pages × e (where e is page table entry size)

Virtual address contain 26 bit assume that number of bit in page size is P so page size is 2^P as given in the question that page table will fit in one page so the size of page table is 2^P.

$$2^P = \frac{2^{26}}{2^P} \times 4B$$

$$2^P = \frac{2^{26}}{2^P} \times 2^2 B$$

$$2^{2P} = 2^{28}$$

$$2P = 28$$

$$P = 14$$

$$\text{Page size} = 2^P = 16 \text{ KB}$$

So answer is 16.

QUESTION ANALYTICS

Q. 26

Consider the organization of a UNIX file as represented by the I-node. Assume that there are 12 direct block pointer and one singly, one doubly, one triply indirect pointer in each I-node. Assume that the system block size and disk sector size are both 8K. If the disk block pointer is 32 bits with 8 bits to identify the physical disk and 24 bits to identify the physical block. Assuming no information other than that the file i-node is already in main memory, how many disk access are required to access the byte in position 13,423,956 _____.

Solution Video | Have any Doubt ?

2 — Correct Option

Solution :
2

Number of disk block pointer in one block

$$= \frac{\text{Block size}}{\text{Pointer size}}$$

$$= \frac{8K}{4} = 2K \text{ pointer per block}$$

The maximum file size supported by the I-node is

$$= (12 + 2K + 2K \times 2K + 2K \times 2K \times 2K) \times \text{Block size}$$

Direct block; Single indirect block; Doubly indirect block; Trtiply indirect block; (8K)

$$= (96 \text{ KB} + 16 \text{ MB} + 32 \text{ GB} + 64 \text{ TB})$$

Direct block covers the first 96 KB, while first indirect block covers the next 16 MB, requested file position is in 13 MB which is clearly with in 16 MB so two disk access is required, one for the first indirect block and one for the block containing the required data.
So answer is 2.

QUESTION ANALYTICS

Q. 27

A hypothetical processor can execute a maximum of 103 instructions per second. System is word addressable and I/O device is connected through shared bus. An average instruction requires 5 machine cycles. Processor executes 90% of its instruction that does not require any I/O instructions. If programmed I/O is used and each one-word I/O transfer requires the processor to execute 2 instructions. The data transfer rate between I/O and processor in words per second
are _____.

Solution Video | Have any Doubt ?

50 — Correct Option

Solution :
50

Given, that 90% of instruction does not requires I/O. So, only 10% instructions will be required I/O.
Thus, maximum I/O instruction execution rate

$$= 10^3 \times 0.10$$

$$= 100 \text{ instructions/second}$$

Now, for 1-word transfer requires processor to execute 2 instructions.

1 word ..... 2 instructions
?.....100 instructions

So, data transfer rate in words per second

$$= \frac{100}{2} = 50 \text{ words/sec}$$

QUESTION ANALYTICS

Q. 28

Consider a 2GHz processor which consumes 10 cycles for LOAD and STORE instruction, 7 cycles for ALU operation and 5 cycle for branch instruction. The frequencies of these instructions are 60%, 30% and 10% for LOAD and STORE, ALU and branch instruction respectively. The processor is enhanced to make cycle per instruction 1 but cycle time increased by 25%. The performance gain in the enhanced processor is _____.

Solution Video | Have any Doubt ?

6.88 — Correct Option

Solution :
6.88

$$\text{Performance gain (S)} = \frac{\text{Execution time of old processor } (ET_{old})}{\text{Execution time of new processor } (ET_{new})}$$

$$\text{Cycle time} = \frac{1}{2\text{ GHz}} = 0.5\text{ ns}$$

$$\begin{aligned} ET_{old} &= \sum(I_i \times CPI_i) \times \text{Cycle time} \\ &= (0.6 \times 10 + 0.3 \times 7 + 0.1 \times 5) \times 0.5\text{ ns} \\ &= 8.6 \times 0.5\text{ ns} \\ &= 4.3\text{ ns} \end{aligned}$$

$$\begin{aligned} ET_{new} &= (0.6 \times 1 + 0.3 \times 1 + 0.1 \times 1) \times (0.5\text{ ns} + (0.25 \times 0.5\text{ ns})) \\ &= 1 \times 0.625\text{ ns} \\ &= 0.625\text{ ns} \end{aligned}$$

Now, $$S = \frac{ET_{old}}{ET_{new}}$$

$$= \frac{4.3\text{ ns}}{0.625\text{ ns}} = 6.88$$

Hence the performance gain is 6.88.

QUESTION ANALYTICS

Q. 29

The arrival time, priority and durations of the CPU and I/O bursts for each of four process P_0, P_1, P_2, P_3 are given in table below. Each process has a CPU burst followed by an I/O burst followed by another CPU burst (Assume that each process has its own I/O resources and all time in millisecond).

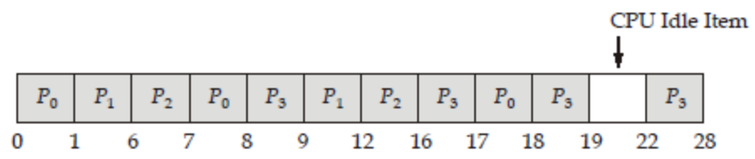
Process	Arrival time	Priority	Burst duration		
			CPU	I/O	CPU
P_0	0	2	2	9	1
P_1	1	0 (highest)	5	3	3
P_2	4	1	1	2	4
P_3	3	3 (lowest)	3	3	6

Operating system uses preemptive priority scheduling if the finish time of P_3 is A and CPU idle time (in percentage) is B, what is the value of A + B _____.
(Upto 1 decimal place)

Solution Video | Have any Doubt ?

38.7 (38.6 - 38.8) — Correct Option

Solution :
38.7 (38.6 - 38.8)



Gantt Chart

$$\text{Finish time of } P_3 = 28 = A$$

$$\text{CPU idle time} = \frac{3}{28} \times 100$$

$$\begin{aligned} A + B &= 28 + 10.71 \\ &= 38.71 \end{aligned}$$

QUESTION ANALYTICS

Q. 30

Consider a hard disk of a processor with a rotation speed of 6000 rpm and transfer rate of 5 MB/sec. Each sector of hard disk holds 64 bytes of data. Seek time of hard disk is 10 ms. Assume records are stored in contiguous sectors by combining 16 sectors. There is no overhead for the controllers time. The time required to access the single record is _____ (in ms). (Upto 2 decimal places)

Solution Video | Have any Doubt ?

15.2048 [15.20 - 15.21] — Correct Option

Solution :
15.2048 [15.20 - 15.21]

$$\begin{aligned} T_{avg} &= \text{Time required to access the single record} \\ &= \text{Seek time + Average rotational time + Transfer time + Overhead (controllers time)} \end{aligned}$$

$$\text{1-revolution time of hard disk} = \frac{60}{6000}\text{sec} = 10\text{ ms}$$

$$\text{Average rotational latency} = \frac{1}{2} \times \text{1 revolution time}$$

$$= \frac{1}{2} \times 10\text{ ms} = 5\text{ ms}$$

$$\text{Transfer time} = \text{Depends on the transfer rate}$$

$$1\text{ sec} \ldots\ldots 5 \times 10^6\text{ B}$$

$$? \ldots\ldots 16\text{ sectors} \times \text{each sectors of 64 bytes}$$

$$= \frac{16 \times 64\text{B}}{5 \times 10^6\text{ B}} = 0.2048\text{ ms}$$

Now, $$\begin{aligned} T_{avg} &= 10\text{ ms} + 5\text{ ms} + 0.2048\text{ ms} \\ &= 15.2048\text{ ms} \end{aligned}$$

QUESTION ANALYTICS

Q. 31

A 10 GHz hypothetical processor capable of moving data from one area of memory to another. Assume combined cost for fetching and decoding of the instruction takes 10 clock cycles. The cost for transferring each byte is 15 clock cycles. There are 2 cases X and Y for service of the interrupt. X represents interrupt can not be served before completing the current instruction but in Y interrupt can be served and current instruction interrupted. Consider an instruction which transfer 64 bytes data during its execution in both the cases and interrupt occurred. The total time (X + Y) in worst case for acknowledging an interrupt is _____ (in ns). (Upto 1 decimal places)

Solution Video | Have any Doubt ?

98.0 (98.0 - 98.5) Correct Option

Solution :
98.0 (98.0 - 98.5)

$$\text{Cycle time} = \frac{1}{10\ \text{GHz}} = 0.1\ \text{ns}$$

The execution length of 64 bytes instruction

$$= [10 + 15 \times 64] \times 0.1 = 97.0\ \text{ns}$$

- In first case X, interrupt can occur just after the start of the instruction. So waiting time for the interrupt to service will be 97.0 ns.
- In second case Y, interrupt is serviced just after it occurs.
  Here, interrupt can be occurred during the byte transfer which is the worst scenario.
  So, maximum waiting time will be = 10 × 0.1 ns = 1 ns
  So total waiting time in both X and Y situation
  = 97.0 ns + 1 ns
  = 98 ns

QUESTION ANALYTICS +

Q. 32

Consider a demand paging system with a paging disk that has an average access and transfer time of 20 milliseconds address are mapped through a page table in main memory, with an access time of 1 microsecond per memory access we have added a associative memory to reduce the access time if the page table entry is in the associative memory. Time to access the associative memory (TLB) is negligible. Assume that 70 percent of the accesses in the associative memory and that, of remaining 10 percent cause page fault what is the effective memory access time _____ (in ms). (Upto 2 decimal places)
(Assume page table access time is negligible)

Solution Video | Have any Doubt ?

0.60 (0.59 - 0.61) Correct Option

Solution :
0.60 (0.59 - 0.61)

Effective memory access time = TLB hit × (Memory Access Time) + TLB miss × (Page fault rate (P) × Page service time + (1 – P) × Memory Access Time)

= 0.7 × 1 µs + 0.3 (0.1 × 20000 µs + 0.9 × 1 µs)
= 0.7 µsec + 0.3 (2000 µs + 0.9 µs)
= 0.7 µsec + 600.27 µsec = 600.97 µsec
= 0.60 millisecond

QUESTION ANALYTICS +

Q. 33

Consider 5-stage RISC pipeline namely Instruction Fetch (IF), Instruction Decode (ID), Execute (EX) Memory Access (MA), Write Back (WB) in the same order instruction accomplishes the task. All the instruction are spending 1-cycle on all stages but load instruction takes 2 cycle on MA stage. The programs are given below:

	Meaning
I_1 : LOAD r_0, 8(r_1)	[load into r_0]
I_2 : MUL r_3, r_0, r_1	[$r_3 \leftarrow r_0 * r_1$]
I_3 : LOAD r_4, 3(r_2)	[load into r_4]
I_4 : ADD r_5, r_4, r_6	[$r_5 \leftarrow r_4 + r_6$]
I_5 : SUB r_6, r_5, r_0	[$r_6 \leftarrow r_5 - r_0$]

Assume operand forwarding is used and by considering the dependencies between instructions, the number of cycles required to complete the program are _____.

Solution Video | Have any Doubt ?

13 Correct Option

Solution :
13

Dependency table of instruction and cycles required by the instruction.

	IF	ID	EX	MA	WB
I_1	1	1	1	2	1
I_2	1	1	1	1	1
I_3	1	1	1	2	1
I_4	1	1	1	1	1
I_5	1	1	1	1	1

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
I_1	IF	ID	EX	MA	MA	WB							
I_2		IF	ID	ID	ID	EX	MA	WB					
I_3			IF	IF	IF	ID	EX	MA	MA	WB			
I_4						IF	ID	ID	ID	EX	MA	WB	
I_5							IF	IF	IF	ID	EX	MA	WB

Hence, total 13 clock cycles are required.

QUESTION ANALYTICS +