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Course: GATE
Computer Science Engineering(CS)

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SINGLE SUBJECT : COMPUTER ORGANIZATION AND ARCHITECTURE (GATE - 2019) - REPORTS

OVERALL ANALYSIS | COMPARISON REPORT | SOLUTION REPORT

ALL(33) | CORRECT(0) | INCORRECT(0) | SKIPPED(33)

Q. 1

Which of the following statements are true?

Solution Video | Have any Doubt ?

A. Input output processor mode uses common bus for I/O and memory but different control signal.

B. Memory mapped I/O mode uses separate bus for I/O and memory.

C. Isolated I/O mode uses common bus with common control signal for both I/O and memory unit.

D. None of the above — Correct Option

Solution :
(d)

- Input output processor mode uses separate bus for memory and I/O unit.
- Memory mapped I/O mode uses common bus with common control signal for both I/O and memory unit.
- Isolated I/O mode uses common bus but different control signal for both I/O and memory unit.

QUESTION ANALYTICS +

Q. 2

Consider the following instruction sequence with there meaning given below:

Instruction	Meaning of Instruction
I_0 : MUL R_2, R_5, R_1	$R_2 \leftarrow R_5 \times R_1$
I_1 : DIV R_5, R_3, R_4	$R_5 \leftarrow R_3 / R_4$
I_2 : ADD R_2, R_5, R_2	$R_2 \leftarrow R_5 + R_2$
I_3 : SUB R_5, R_2, R_6	$R_5 \leftarrow R_2 - R_6$

What is the number of Write After Read (WAR) and Write After Write (WAW) hazards for the above instruction sequence?

Solution Video | Have any Doubt ?

A. 3, 2 — Correct Option

Solution :
(a)

$$\text{WAW} = I_0(R_2) \rightarrow I_2(R_2),\ I_1(R_5) \rightarrow I_3(R_5)$$
$$\text{WAR} = I_0(R_5) \rightarrow I_1(R_5),\ I_0(R_5) \rightarrow I_3(R_5),\ I_2(R_5) \rightarrow I_3(R_5)$$

B. 2, 1

C. 3, 1

D. 1, 2

QUESTION ANALYTICS +

Q. 3

A non-pipeline processor has a clock rate 4 MHz and an average CPI of 5. An upgrade to the processor introduce 5 stage pipeline. How ever due to internal delay the clock rate of the new processor has to be reduces to 3 MHz. What is the speed-up of pipeline over non-pipeline?

Solution Video | Have any Doubt ?

A. 3.1

B. 3.7 — Correct Option

Solution :
(b)

$$ET_{\text{non-pipe}} = \text{Average CPI} \times \text{Cycle time (non-pipe)}$$
$$= 5 \times 0.25\ \mu\text{sec}$$
$$= 1.25\ \mu\text{sec}$$
$$ET_{\text{pipe}} = \text{Average CPI}_{\text{pipe}} \times \text{Cycle time (pipe)}$$
$$= 1 \times 0.33\ \mu\text{sec}$$
$$= 0.33\ \mu\text{sec}$$
$$\text{Speed-up} = \frac{ET_{\text{non-pipe}}}{ET_{\text{pipe}}}$$
$$= \frac{1.25}{0.33} = 3.78 \approx 3.7$$

C. 3.5

D 4.1

QUESTION ANALYTICS +

Q. 4

Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I	List-II
A. To access constant value	1. Indirect addressing mode
B. Static variable	2. Direct addressing mode
C. Pointer	3. Based index addressing mode
D. Structure	4. Immediate addressing mode

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	2	3	4	1
(c)	4	2	1	3
(d)	2	3	1	4

Solution Video | Have any Doubt ?

A a

B b

C c Correct Option

Solution :
(c)
- To access constant value Immediate addressing mode is used.
- Static variable are using Direct addressing mode.
- Pointer are implemented using Indirect addressing mode.
- Array are implemented using Based index addressing mode.

D d

QUESTION ANALYTICS +

Q. 5

A 4-way set-associative cache memory unit with a capacity of 32 KB is built using a block size of 16 words. The word length is 32 bits. The size of the physical address space is 4 GB. What is the number of bits tag, set and word offset field are respectively?

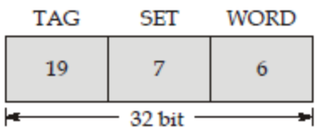
Solution Video | Have any Doubt ?

A 19, 8, 5

B 20, 7, 5

C 19, 7, 6 Correct Option

Solution :
(c)



$$\text{WORD offset} = \text{Number of word in a block} \times \text{word size}$$
$$16 \times 4 = 64$$
$$\text{WORD offset} = \log 64 = 6 \text{ bits}$$
$$\text{Number of blocks} = \frac{32\text{K}}{64} = 512 \text{ Blocks}$$
$$\text{Number of sets} = \frac{512}{4} = 128$$
$$\text{SET offset} = 7 \text{ bits}$$
$$\therefore \quad \text{Number of TAG bits} = 32 - (7 + 6)$$
$$= 19 \text{ bits}$$

D 18, 8, 6

QUESTION ANALYTICS +

Q. 6

Consider the following table:

Design change	Effect on miss rate
P. Increase cache size	(i) Decrease conflict misses
Q. Increase associativity	(ii) Decrease compulsory misses
R. Increase block size	(iii) Decrease capacity misses

Match the Design change in cache to Effect on miss rate:

Solution Video | Have any Doubt ?

A P-(i), Q-(ii), R-(iii)

B P-(ii), Q-(i), R-(iii)

C P-(i), Q-(iii), R-(ii)

D P-(iii), Q-(i), R-(ii) Correct Option

Solution :
(d)
1. Increasing cache size will decrease capacity miss.
2. Increasing associativity decreases conflict misses.
3. Increasing block size will decreases compulsory misses.

QUESTION ANALYTICS

Q. 7

Suppose 2-way set associative cache with 2^m lines 2^P bytes per cache lines. Memory is byte addressable of 2^n bytes. What is the space required for storing tags (in bits)?

Solution Video | Have any Doubt ?

A $2^{n-(m+p)}$

B $2^m \times (n-(m+p))$

C $2^m \times (n-((m-1)+p))$ Correct Option

Solution :
(c)

$$\text{Number of sets} = \frac{\text{Number of lines}}{\text{Set associativity}}$$

$$= \frac{2^m}{2} = 2^{m-1}$$

Set offset = $\log_2(2^{m-1}) = (m-1)$ bits
Word offset = $\log_2(2^p) = p$ bits
Address field size = $\log_2(2^n) = n$ bits
Tag bits per line = $n-((m-1)+p)$
Tag size = Number of cache lines × Number of tag bits per line
= $2^m \times (n-((m-1)+p))$

D $2^p \times (n-(m+p))$

QUESTION ANALYTICS

Q. 8

Consider a processor with 4 byte jump instruction is encountered at memory address 2056. If the jump instruction is in PC relative mode and instruction at memory address 2056 is JMP –15 (where –15 is signed byte) then what is the branch target address?

Solution Video | Have any Doubt ?

A 2060

B 2055

C 2050

D 2045 Correct Option

Solution :
(d)
Jump instruction is at address 2056 and is 4 bytes. Therefore PC will point to 2060 on execution of this instruction.
Branch target address = PC + (–15)
= 2060 – 15 = 2045

QUESTION ANALYTICS

Q. 9

Which of the following is true?

Solution Video | Have any Doubt ?

A Inside an Interrupt Service Routine, the values of the PC and CPU registers are pushed in the Stack.

B An Interrupt Vector is the starting address of an Interrupt Service Routine. Correct Option

Solution :
(b)
• The ISR does not push the value of PC and CPU register into stack but processor does this before the ISR is executed. So False.
• An Interrupt Vector is the starting address of an Interrupt Service Routine is true.
• The processor does not save these registers, as the Reset will initialize these values. So False.

C When servicing a Reset instruction, the values of the PC and CPU Registers are pushed in the Stack by processor.

D Both (b) and (c)

QUESTION ANALYTICS

Q. 10

Assume that for a certain processor, a read request takes 100 nanoseconds on a cache miss and 20 nanoseconds on a cache hit. Suppose while running a program, it was observed that 30% of the processor's read requests result in a cache miss. What is the average read access time?

Solution Video | Have any Doubt ?

A 55 nsec

B 44 nsec — Correct Option

Solution :
(b)

$$T_{readmiss} = 100 \text{ nsec}$$
$$T_{readhit} = 20 \text{ nsec}$$
$$(1 - h) = 0.30$$
$$T_{avgread} = h \times T_{readhit} + (1 - h) \times T_{readmiss}$$
$$= 0.70 \times 20 + 0.30 \times 100$$
$$= 14 + 30 = 44 \text{ nsec}$$

C 40 nsec

D 38 nsec

QUESTION ANALYTICS +

Q. 11

A microprocessor provides an instruction capable of moving a strings of bytes form one place to another place in memory. The fetching and initial decoding of instruction takes 8 clock cycles. After that, it takes 10 clock cycle to transfer each byte. If the clock rate of microprocessor is 10 GHz, then the time to transfer string of 80 bytes is _____. (in nsec) (Assume after each byte transfer interrupt is occurred)

Solution Video | Have any Doubt ?

144 — Correct Option

Solution :
(144)
Time to fetch and decode = 8 clock cycles
Since after every byte transfer interrupt is occur. So, number of clock cycles to transfer

$$1 \text{ byte} = 18 \text{ cycle}$$
$$\text{So, for 80 such bytes} = 80 \times (10 + 8)$$
$$= 1440 \text{ cycles}$$
$$\text{Time taken} = 1440 \times 0.1 \text{ nsec} = 144 \text{ nsec}$$

QUESTION ANALYTICS +

Q. 12

Consider 3 enhancements EA, EB, and EC with speedup 30, 20, 15 respectively are applied to old system to make a new system. If enhancements EA and EB are usable for 25% of the time, then the fraction (in %) of the time must EC be used to achieve an overall speed-up of 10 is _____. (in integer form)

Solution Video | Have any Doubt ?

45 — Correct Option

Solution :
45
By using Amdahl's Law:

$$10 = \left[1 - (0.25 + 0.25 + EC) + \left(\frac{0.25}{30}\right) + \left(\frac{0.25}{20}\right) + \left(\frac{EC}{15}\right)\right]^{-1}$$

$$10 = \frac{60}{[60 - 15 - 15 - 60\,EC + 0.5 + 0.75 + 4EC]}$$

$$-56\,EC + 31.25 = 6$$
$$56\,EC = 25.25$$
$$EC = 0.45089$$
$$\text{In \% EC} = 0.45089 \times 100 = 45\%$$

QUESTION ANALYTICS +

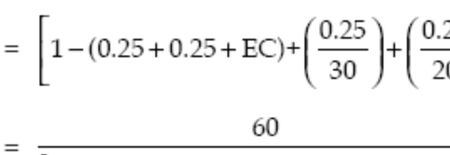
Q. 13

Consider a system with instruction set that uses a fixed 16 bits instruction length and length of address is 6 bits. There are 10 two address instructions and 8192 zero address instructions. The maximum number of one address instructions that can be supported are _____.

Solution Video | Have any Doubt ?

256 — Correct Option

Solution :
256



Total number of opcode = $2^4 = 16$
Remaining opcodes for one address instruction = (16 – 10) = 6
Possible 1 address instruction = $2^6 \times 6$
Consider there are 'n' one address instruction.
Remaining opcodes for zero address instruction
$= 2^6 \times 6 - n$
Possible zero address instruction
$(2^6 \times 6 - n) \times 2^6 = 8192$
By solving we get $n = 256$

QUESTION ANALYTICS +

Q. 14

Consider 5-stage pipeline with stage delays as 150, 120, 160, 180 and 140 ns respectively. Registers that are used between every two stages have a delay of 5 ns each. If clocking frequency is 1 MHz, then the total time taken to process 1000 data items on this pipeline will be _____ (in µsec up to 2 decimal places).

Solution Video | Have any Doubt ?

185.74 [185.50 - 185.90] — Correct Option

Solution :
185.74 [185.50 - 185.90]

$$\begin{aligned}\text{Pipeline Time} &= \max(150, 120, 160, 180 \text{ and } 140 \text{ ns}) + \text{Buffer delay}\\ &= 185 \text{ ns}\\ \text{Execution Time} &= [K + n - 1] \times \text{Pipeline time (where K is number of stages)}\\ &= [5 + 1000 - 1] \times 185 \text{ ns}\\ &= [1004] \times 185 \text{ ns}\\ &= 185740 \text{ ns} = 185.74 \text{ µsec}\end{aligned}$$

QUESTION ANALYTICS

Q. 15

Consider a single-level cache with an access time of 2.5 ns with block size of 64 bytes. Main memory uses a block transfer capability that has a first word (4 bytes) access time of 50 ns and an access time of 5 ns for each word thereafter. If hit ratio of cache memory is 95%, then average memory access time is _____.
[Upto 3 decimal places]

Solution Video | Have any Doubt ?

8.75 (8.70 - 8.80) — Correct Option

Solution :
8.75 (8.70 - 8.80)

$$\begin{aligned}\text{Average Access Time} &= (0.95 \times 2.5) + (1 - 0.95)\,((50 + 15 \times 5) + 2.5)\\ T_{avg} &= 8.75 \text{ ns}\end{aligned}$$

QUESTION ANALYTICS

Q. 16

A device with data transfer rate 40 KB/sec is connected to a CPU, where data transfer time between interfaces to memory or CPU is neglected. If the interrupt overhead is 2 µsec, then minimum performance gain of operating the device under interrupt mode over operating it under programcontrolled mode _____. (Assume data transferred Byte wise) [Upto 1 decimal place]

Solution Video | Have any Doubt ?

12.5 (12.2 - 12.8) — Correct Option

Solution :
12.5 (12.2 - 12.8)

$$S = \frac{ET_{Prog\text{-}IO}}{ET_{INT\text{-}IO}} = \frac{25}{2} = 12.5$$

QUESTION ANALYTICS

Q. 17

Consider a pipeline 'x' consist of 5 stages named as IF, ID, OF, EX and WB with the respective stage delays of 2 ns, 6 ns, 5 ns, 8 ns and 1 ns. The alternative pipeline 'y' contain the same number of stages but EX stage is divided into 2 sub stages, (EX1 and EX2) with equal delay i.e. (8 ns/2) and ID stage is divided into 3 substages (ID1, ID2 and ID3) with equal delays of (6 ns/3). In the pipeline x and y memory reference instructions are not overlapped so the penalty of memory
reference instructions in the pipeline 'x' is 4 cycles and in the pipeline 'y' is 8 cycles. If the program contain 20% of the instructions which are memory based instructions, what is the ratio of speedup of x to speedup of y?

Solution Video | Have any Doubt ?

A. 0.727

B. 1.2 — Correct Option

Solution :
(b)

$$S_x = \frac{t_n}{(1 + \#\text{ stalls/Instruction})\,\text{cycle time}}$$

$$S_x = \frac{22}{[1 + (0.2 \times 4)]6 \text{ ns}} = \frac{22}{10.8} = 2.037$$

$$S_y = \frac{t_n}{(1 + \#\text{ stalls/Instruction})\,\text{cycle time}}$$

$$S_y = \frac{22}{(1 + 1.6)5 \text{ ns}} = \frac{22}{13} = 1.692$$

$$\frac{S_x}{S_y} = \frac{2.037}{1.692} = 1.2$$

C. 0.665

D. 0.825

QUESTION ANALYTICS

Q. 18

Consider 5 stage pipelined processor has instruction fetch (IF), Instruction decode (ID), Operand fetch (OF), Perform operation (PO) and Write operand

(WB) stages. The IF, ID, OF and WB stages takes 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction, 4 clock cycles for MUL instruction and 3 clock cycles for DIV instructions respectively.

Instruction	Meaning of Instruction
I_0: ADD R_2, R_0, R_1;	$R_2 \leftarrow R_0 + R_1$
I_1: MUL R_5, R_3, R_4;	$R_5 \leftarrow R_3 \times R_4$
I_2: SUB R_2, R_5, R_2;	$R_2 \leftarrow R_5 - R_2$
I_3: DIV R_5, R_2, R_6;	$R_5 \leftarrow R_2 / R_6$

How many clock cycles needed to execute the above sequence of instruction where operand forwarding from PO to PO?

Solution Video | Have any Doubt ?

A 8

B 10

C 13 Correct Option

Solution :
(c)

	IF	ID	OF	PO	WB
ADD	1	1	1	1	1
MUL	1	1	1	4	1
SUB	1	1	1	1	1
DIV	1	1	1	3	1

	1	2	3	4	5	6	7	8	9	10	11	12	13
I_0	IF	ID	OF	PO	WB								
I_1		IF	ID	OF	PO	PO	PO	PO	WB				
I_2			IF	ID	OF	OF	OF	OF	PO	WB			
I_3				IF	ID	ID	ID	ID	OF	PO	PO	PO	WB

D 15

QUESTION ANALYTICS +

Q. 19

Consider the following bit pattern represents the floating point number in IEEE 754 single precision format:
1 10000111 11100000000000000000000
Which of the following represents the decimal value of above floating point number?

Solution Video | Have any Doubt ?

A –192

B –320

C –384

D –480 Correct Option

Solution :
(d)

1 bit	8 bits	23 bits
1	10000111	11100 ... 0
Sign	Exponent	Mantissa

$$\begin{aligned}
\text{Bias exponent value} &= 10000111 \\
\text{Actual exponent} &= 10000111 - 127 \quad [\because 127 \text{ is bias}] \\
&= 135 - 127 = 8 \\
\text{Normalized mantissa bits} &= 11100000000000000000000 \\
\text{Actual value} &= 1.11100000000000000000000 \\
\text{Decimal number} &= 1.11100 \times 2^8 \\
&= -(111100000)_2 \\
&= -(480)_{10}
\end{aligned}$$

QUESTION ANALYTICS +

Q. 20

Consider a system with 24 bit main memory. Data is transferred between main memory and cache in blocks of 4 bytes each. The cache can hold 64 KB. If the cache memory is 8-way set associative, then the main memory address B012EA is mapped into which set of cache? (Assume main memory is byte addressable)

Solution Video | Have any Doubt ?

A 10010111010 Correct Option

Solution :
(a)

TAG	Set	Block size
11	11	2

$$\text{Number of cache lines} = \frac{2^{16}}{2^2} = 2^{14}$$

$$\text{Number of sets} = \frac{2^{14}}{2^3} = 2^{11}$$

$$\text{Main memory address} = 101100000001\underbrace{00101110101}_{\text{Set}}0$$

B 10010111011

C 1100101110

D 1001100100

QUESTION ANALYTICS

Q. 21

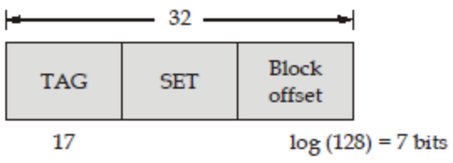
Consider m-way set associative cache with 32-bit addresses and having block size 128 Bytes. If cache memory has 1024 blocks and TAG bits are 17, then what is the number of sets and associativity of cache?

Solution Video | Have any Doubt ?

A 128 sets, 8-way set associativity

B 256 sets, 4-way set associativity — Correct Option

Solution :
(b)



$$\text{Number of sets bits} = 32 - (17 + 7)$$
$$= 32 - 24 = 8$$

i.e. 256 sets are present.
Since number of block in cache = 1024

$$\text{So,} \quad \text{Associativity} = \frac{2^{10}}{m} = 2^8$$
$$m = 2^{10-8}$$
$$m = 4$$

So, 256 sets and 4-way set associative.

C 256 sets, 8-way set associativity

D Cannot be determined

QUESTION ANALYTICS

Q. 22

Consider the following Booth's multiplication:
Multiplicand : 1011 0111 1111
Multiplier : 0101 1100 1001

Which of the following represents the number of arithmetic operations are required in the multiplication?

Solution Video | Have any Doubt ?

A 5

B 6

C 7

D 8 — Correct Option

Solution :
(d)

Multiplier	Pair with $(q - 1)$	Recorder
1	0	−1
0	1	+1
0	0	0
1	0	−1
0	1	+1
0	0	0
1	0	−1
1	1	0
1	1	0
0	1	+1
1	0	−1
0	1	−1

Number of arithmetic operations are 8 (Recorder with sign '−' and '+').

QUESTION ANALYTICS

Q. 23

A hard disk with a transfer rate of 1 KBps is constantly transferring data to memory using DMA cycle stealing mode. The size of the data transfer is 16 bytes. The processor runs at 400 kHz clock frequency. The DMA controller requires 10 cycles for initialization of operation and transfer takes 2 cycles to transfer one byte of data from the device to the memory. What is the percentage of processor time blocked during this DMA operation?

Solution Video | Have any Doubt ?

A 0.70 %

B 0.65 % — Correct Option

Solution :
(b)

$$\% \text{ Time CPU is blocked} = \frac{\text{Transfer Time}}{\text{Transfer Time + Preparation Time}}$$

Preparation Time:

10^5 bytes → 1 sec
1 bytes → 1 msec
So, 16 bytes → 16 msec

Transfer time = 10 cycles for initialization + (2 × 16) cycles for transfer
= 42 cycles

$$1 \text{ cycle time} = \frac{1}{400\,\text{kHz}} = 0.0025 \text{ msec}$$

So, 42 cycles = 42 × 0.0025 msec
= 0.105 msec

$$\% \text{ of time CPU blocked} = \frac{0.105}{16+0.105} = \frac{0.105}{16.105}$$
= 0.0065 × 100
= 0.65 %

C 0.50 %

D 0.55 %

QUESTION ANALYTICS +

Q. 24

Consider the following statements:
S_1 : Direct mapped caches do not need a cache block replacement policy, where as fully associative cache need.
S_2 : Direct mapped cache, may produce more misses if programs refers to memory words that occupy a same tag value.
Which of the following options is correct?

Solution Video | Have any Doubt ?

A Only S_1 is true — Correct Option

Solution :
(a)

• Since in direct mapped cache a block can mapped to only a particular block by using formula [MM block % cache blocks = cache block number]. Where as in fully associative cache a block can mapped to more than one cache block with in a set so only fully associative cache needs cache replacement policy. So, statement is true.
• Since in direct mapped cache, mapping is based on line offset not on TAG and those memory addresses having same line offset are mapped to same cache line. Therefore, if a program refers to memory access with same TAG value does not ensure more misses. Hence this statement is false.

B Only S_2 is true

C Both S_1 and S_2 are true

D Neither of S_1 nor S_2 is true

QUESTION ANALYTICS +

Q. 25

A Hypothetical control unit supports 5 groups of mutually exclusive signals

Group	G_1	G_2	G_3	G_4	G_5
Control Signal	2	1	4	33	25

What is the size of control memory (in bytes), if vertical programming is used, Assume control unit support 256 control word memory?

Solution Video | Have any Doubt ?

A 704 bytes

B 736 bytes — Correct Option

Solution :
(b)
Number of bits for control signals in vertical programming:

$$\log_2(2) + \log_2(1) + \log_2(4) + \log_2(33) + \log_2(25)$$
= 1 + 1 + 2 + 6 + 5
= 15 bits
256 CW = 8 bits

VCW:

Branch condition	Flag	Control field	Control memory address
		15	8

VCW size = 15 + 8 = 23 bits
Vertical control memory size = 256 × 23 bits

$$= \frac{256 \times 23}{8} \text{ bytes}$$
= 736 bytes

C 746 bytes

D 814 bytes

QUESTION ANALYTICS +

Q. 26

Consider a machine with byte addressable main memory of 30 bits, block size of 16 bytes and 4-way set associative cache of size 256 byte. For choosing the block to be replaced, use last recently used scheme. What is the number of cache misses for the following sequence of block addresses is 12, 28, 18, 15, 19, 31, 39, 15, 7, 15?

Solution Video | Have any Doubt ?

A 4

B 6

C 8 Correct Option

Solution :
(c)

$$\text{Number of cache line} = \frac{\text{Cache size}}{\text{Block size}}$$

$$= \frac{2^8}{2^4} = 2^4 = 16$$

$$\text{Number of sets} = \frac{2^4}{2^2} = 2^2 = 4$$

Set 0	12	28		
Set 1				
Set 2	18			
Set 3	15	19 7	31	39

There are 8 cache misses are possible.

D 9

QUESTION ANALYTICS +

Q. 27

Consider a two level memory hierarchy, L_1 (cache) has an accessing time of 5 ns and main memory has an accessing time of 100 ns. Writing or updating contents takes 20 ns and 200 ns for L_1 and main memory respectively. Assume L_1 gives misses 20% of the time with 60% of the instructions are read only instructions. What is the average access time for system (in ns) if it uses WRITETHROUGH technique?

Solution Video | Have any Doubt ?

A 80 ns

B 75 ns

C 94.4 ns Correct Option

Solution :
(c)

$$T_{(\text{read})} = \text{Hit} \times \text{Read Time of } L_1 + (1 - \text{hit}) \times \text{Read Time of Memory}$$
$$= 0.8 \times 5 \text{ ns} + 0.2 \times 100 \text{ ns}$$
$$= 4 \text{ ns} + 20 \text{ ns} = 24 \text{ ns}$$

H_w = 1 So, memory organization is simultaneous.

$T_{(\text{write})}$ = Write time to main memory = 200 ns

[Since, in WRITE-THROUGH CPU writes in both cache and main memory. Hence writing time of main memory is considered.]

$$T_{\text{avg}} = F_{\text{Read}} \times T_{(\text{read})} + F_{\text{write}} \times T_{(\text{write})}$$
$$= 0.6 \times 24 \text{ ns} + 0.4 \times 200 \text{ ns}$$
$$= 14.4 \text{ ns} + 80 \text{ ns}$$
$$= 94.4 \text{ ns}$$

D 85 ns

QUESTION ANALYTICS +

Q. 28

Consider the following piece of code:

```
int x = 0, y = 0;
int i;          //x, y, i are in register
int A[4096]; // A is in memory at address 0x 10000
for (i = 0; i < 1024; i++) {
    x+ = A[i];
}
for (i =0; i < 1024; i++) {
    y+ = A[i + 2048];
}
```

Assume that the system has a 2^{13} byte, direct-mapped data cache with 16-byte blocks. Assuming that the cache starts out empty, also Assume that an iteration of a loop in which the load hits takes 10 cycles but that an iteration of a loop in which the load misses takes 100 cycles. What is the execution time (cycles) of this snippet with the mentioned cache?
[Note: Assume integer size = 4 byte]

Solution Video | Have any Doubt ?

A 66556

B 66560 Correct Option

Solution :
(b)

Cache is a direct mapped one.

For the first loop: one in 4 elements causes a miss.

Sequence: M, H, H, H, M, H, H, H, M, ...

$$\text{Number of misses} = \frac{1024}{4} = 256$$

Number of hits = 768

For the second loop: 2048 × 4 = 8192 bytes which is the capacity of the direct mapped cache.
Therefore A[i+2048] is again mapped starting from 0 onwards.
So the sequence is same above: Miss, H, H, H, M, H, H, H, M, …

$$\text{Number of misses} = \frac{1024}{4} = 256$$

$$\begin{aligned}\text{Number of Hits} &= 768\\ \text{Total Number of misses} &= 512\\ \text{Number of hits} &= 1536\\ \text{Total Execution Time} &= 10 \times 1536 + 100 \times 512\\ &= 66560 \text{ cycles}\end{aligned}$$

C 66500

D 66548

QUESTION ANALYTICS +

Q. 29

Consider a RISC processor with an ideal CPI, where 25% of the total instructions are load and store instruction. Time to accessing main memory is 100 clock cycles and accessing of the cache memory required 2 clock cycles. If cache miss rate is 2%, then the effective CPI for the system with the cache is _____. [Upto 2 decimal placed]

Solution Video | Have any Doubt ?

5.00 [4.95 - 5.05] Correct Option

Solution :
5.00 [4.95 - 5.05]
LOAD and STORE take 2 memory access, 1 for IF and 1 for loading/storing.
So total memory access for 100 instruction

$$= 100 \text{ (IF)} + 1 \times 0.25 \times 100 \text{ (loading/storing)}$$
$$= 100 + 25 = 125 \text{ memory access}$$

Average memory access/instruction

$$= \frac{125}{100}$$
$$= 1.25 \text{ memory access/instruction}$$

Cycles per instruction for handling cache misses

$$= \text{Memory accesses per instruction} \times \text{Miss rate} \times \text{Cycles per miss}$$
$$= 1.25 \times 0.02 \times 102$$
$$= 2.55 \text{ Cycles per instruction}$$

Cycles per instruction for handling cache hits

$$= \text{Memory accesses per instruction} \times \text{Hit rate} \times \text{Cycles per hit}$$
$$= 1.25 \times 0.98 \times 2$$
$$= 2.45 \text{ Cycles per instruction}$$

$$\begin{aligned}\text{Effective CPI} &= \text{Cycles for hits} + \text{Cycles for misses}\\ &= 2.55 + 2.45 = 5\end{aligned}$$

QUESTION ANALYTICS +

Q. 30

Consider a hypothetical system used in web applications. Application program refers the IO operation and ALU operations. IO operational unit is enhanced then it runs 4 times faster. In the application program 40% of instructions are ALU instructions. The performance gain in the enhanced system is _____ (upto 2 decimal places).

Solution Video | Have any Doubt ?

1.80 (1.80-1.81) Correct Option

Solution :
1.80 (1.80-1.81)

$$S = \left[(1-F) + \frac{F}{S}\right]^{-1}$$

$$S = \left[(1-0.6) + \frac{0.6}{4}\right]^{-1}$$

$$S = [0.4 + 0.15]^{-1}$$

$$S = 1.8$$

QUESTION ANALYTICS +

Q. 31

Consider two level cache hierarchies with L_1 and L_2 cache. Programs refer memory 1000 times, out of which 40 misses are in L_1 cache and 10 misses are in L_2 cache. If the miss penalty of L_2 is 200 clock cycles, hit time of L_1 is 1 clock cycle, and hit time of L_2 is 15 clock cycles, the average memory access time is _____ clock cycles. (Upto 1 decimal place)

Solution Video | Have any Doubt ?

3.6 Correct Option

Solution :
3.6

$$L_1 \text{ miss rate} = \frac{40}{1000} = 4\%$$

$$L_2 \text{ miss rate (we need to take local miss rate)} = \frac{(10)}{40} = 25\%$$

$$\begin{aligned}\text{Average access time} &= \text{Hit time } (L_1) + \text{Miss rate } (L_1)[\text{Hit time } (L_2) + \text{Miss rate } (L_2) \times \text{Miss penalty}]\\ &= 1 + 4\% \text{ [15 cc} + 25\% \times 200 \text{ cc]}\\ &= 1 + 0.04 \text{ [15 cc} + 50 \text{ cc]}\end{aligned}$$

$= 3.6$ cc

QUESTION ANALYTICS

Q. 32

An instruction pipeline consists of following 5 stages:
IF = Instruction Fetch, ID = Instruction Decode, EX = Execute,
MA = Memory Access and WB = Register Write Back
Consider the following code:

1.	LOAD	R_1, [1000]	R_1 = Memory [1000]
2.	LOAD	R_3, 4(R_2)	R_3 = Memory [R_2 + 4]
3.	MUL	R_4, R_1, R_3	$R_4 = R_1 \times R_3$
4.	DIV	R_5, R_1, R_4	$R_5 = R_1 \div R_4$
5.	SUB	R_6, R_4, R_5	$R_6 = R_4 - R_5$

Assume that each stage takes 1 clock cycle for all the instructions. The number of cycles needed to execute the code, by using operand forwarding are _____.

Solution Video | Have any Doubt ?

10 — Correct Option

Solution :
10
With operand forwarding

	1	2	3	4	5	6	7	8	9	10
I_1	IF	ID	EX	MA	WB					
I_2		IF	ID	EX	MA	WB				
I_3			IF	ID	ID	EX	MA	WB		
I_4				IF	IF	ID	EX	MA	WB	
I_5						IF	ID	EX	MA	WB

10 cycles are required.

QUESTION ANALYTICS

Q. 33

Consider Prof. Vamshi's writes a program given below and run on system which has 2-way set associative 16 KB data cache with 32 bytes block where each word size is 32 bits and LRU replacement policy used. If base address of array 'a' is 0×0 and initially cache is empty then the number of data cache misses are there _____. (Assume integer takes 8 bytes)

```
int i, a[1024 * 1024], x = 0;
    for (i = 0; i < 1024; i++) {
        x + = a[i] + a[1024* i];
}
```

Solution Video | Have any Doubt ?

1279 — Correct Option

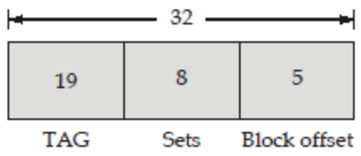
Solution :
1279

$$\text{Cache size} = 16 \text{ KB}$$
$$\text{Block size} = 32 \text{ B}$$

$$\text{Number of lines (Blocks)} = \frac{16 \text{ KB}}{32 \text{ B}} = \frac{2^{14}\text{B}}{2^5\text{B}} = 2^9$$

Since 2-way set associative,

$$\text{So, Number of sets} = \frac{2^9}{2} = 2^8$$



Set 0	0 – 31	0	1024 – 1055	1
Set 1	32 – 63	0	1056 – 1087	1
Set 2	64 – 95	0		1
Set 255		0		1

1. **First access:** $a^{\text{Miss}}[0] + a^{\text{Hit}}[0]$, since $a[0]$ is miss, $a[0]$, $a[1]$, $a[2]$ and $a[3]$ are fetched to mem. Since word size is 32 bits, so 4 integer are fetched on a miss.
2. **Second access:** $a^{\text{Hit}}[1] + a^{\text{Miss}}[1024]$
3. **Third access:** $a^{\text{Hit}}[2] + a^{\text{Miss}}[1048]$

$$\text{Line this, Total number of miss} = \frac{1024}{4} + (1024 - 1)$$
$$= 256 + 1023 = 1279$$

QUESTION ANALYTICS