Design and Verification of the full adder using system verilog testbench architecture approach

Tuesday, 17 June, 2025 11:04 PM

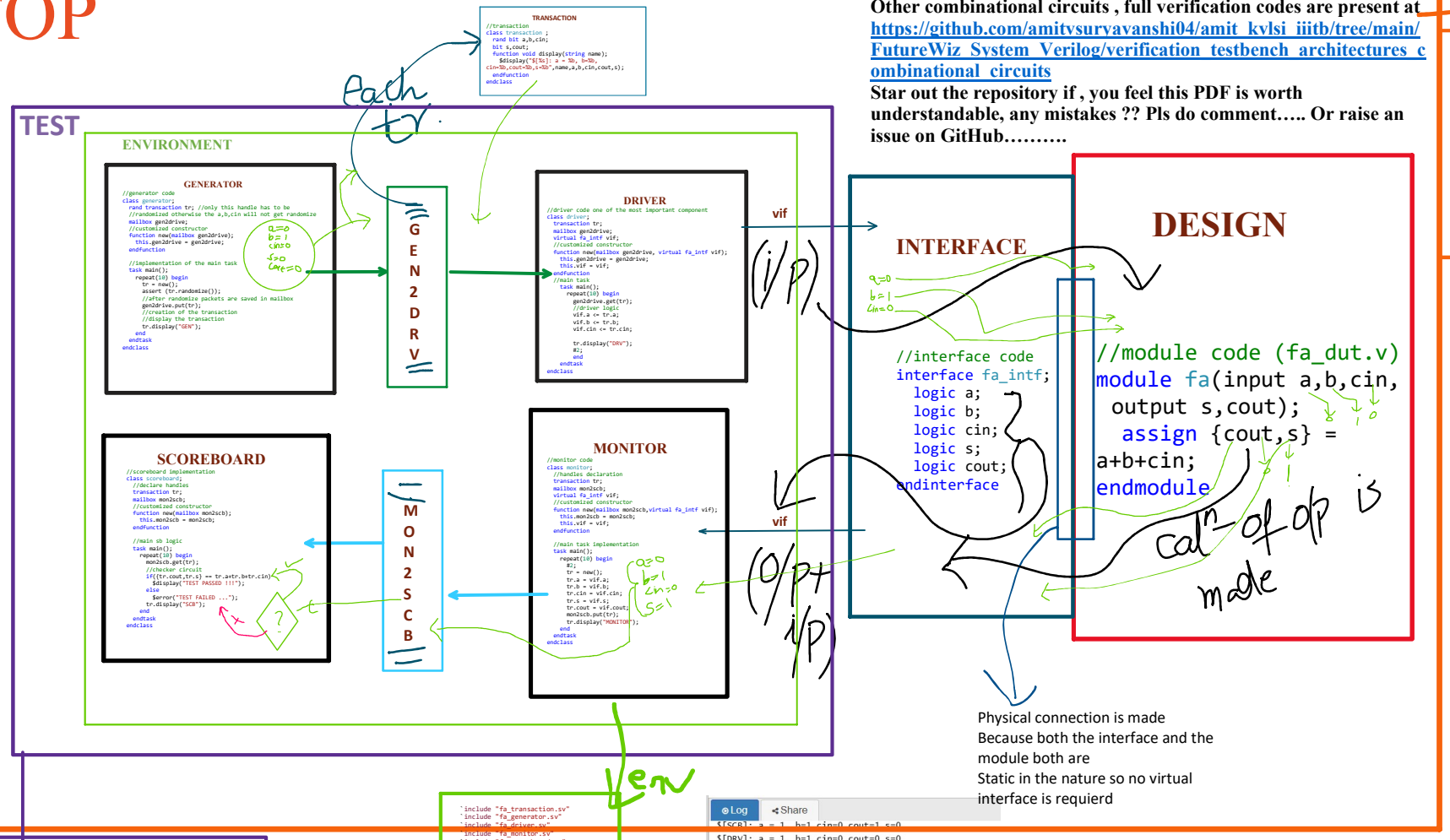
This note was created by "Amit Suryavanshi" in Microsoft OneNote...
LinkedIN: https://www.linkedin.com/in/amit-suryavanshi-668713241/

TOP

Other combinational circuits , full verification codes are present at https://github.com/amitvsuryavanshi04/amit_kvlsi_iiitb/tree/main/FutureWiz_System_Verilog/verification_testbench_architectures_combinational_circuits

Star out the repository if , you feel this PDF is worth understandable, any mistakes ?? Pls do comment….. Or raise an issue on GitHub…….

```
`include "fa_test.sv"
`include "fa_interface.sv"
// Top module
module top;
  fa_intf inf();
  fa
dut(.a(inf.a), .b(inf.b), .cin(inf
.cin), .s(inf.s), .cout(inf.cout))
;
  initial begin
    test t;
    t = new(inf);
    t.run();
    $finish;
  end
endmodule
```



Physical connection is made
Because both the interface and the module both are
Static in the nature so no virtual interface is requierd

```
`include "fa_environment.sv"
// Test
class test;
  env e;
  function new(virtual fa_intf vif);
    e = new(vif);
  endfunction
  task run();
    e.run();
  endtask
endclass
```

```
`include "fa_transaction.sv"
`include "fa_generator.sv"
`include "fa_driver.sv"
`include "fa_monitor.sv"
`include "fa_scoreboard.sv"
// Environment
class env;
  generator gen;
  driver drv;
  monitor mon;
  scoreboard scb;
  mailbox gen2drv;
  mailbox mon2scb;
  virtual fa_intf vif;
  function new(virtual fa_intf vif);
    this.vif = vif;
    gen2drv = new();
    mon2scb = new();
    gen = new(gen2drv);
    drv = new(gen2drv, vif);
    mon = new(mon2scb, vif);
    scb = new(mon2scb);
  endfunction
  task run();
    fork
      gen.main();
      drv.main();
      mon.main();
      scb.main();
    join
  endtask
endclass
```

OUTPUT

```
Log  Share
$[SCB]: a = 1, b=1,cin=0,cout=1,s=0
$[DRV]: a = 1, b=1,cin=0,cout=0,s=0
$[MONITOR]: a = 1, b=1,cin=0,cout=1,s=0
TEST PASSED !!!
$[SCB]: a = 1, b=1,cin=0,cout=1,s=0
$[DRV]: a = 1, b=0,cin=1,cout=0,s=0
$[MONITOR]: a = 1, b=1,cin=0,cout=1,s=0
TEST PASSED !!!
$[SCB]: a = 1, b=1,cin=0,cout=1,s=0
$[DRV]: a = 0, b=1,cin=0,cout=0,s=0
$[MONITOR]: a = 1, b=0,cin=1,cout=1,s=0
TEST PASSED !!!
$[SCB]: a = 1, b=0,cin=1,cout=1,s=0
$[DRV]: a = 0, b=1,cin=0,cout=0,s=0
$[MONITOR]: a = 0, b=1,cin=0,cout=0,s=1
TEST PASSED !!!
$[SCB]: a = 0, b=1,cin=0,cout=0,s=1
$[DRV]: a = 0, b=0,cin=0,cout=0,s=0
$[MONITOR]: a = 0, b=1,cin=0,cout=0,s=1
TEST PASSED !!!
$[SCB]: a = 0, b=1,cin=0,cout=0,s=1
```