Name: Anna Kurchenko

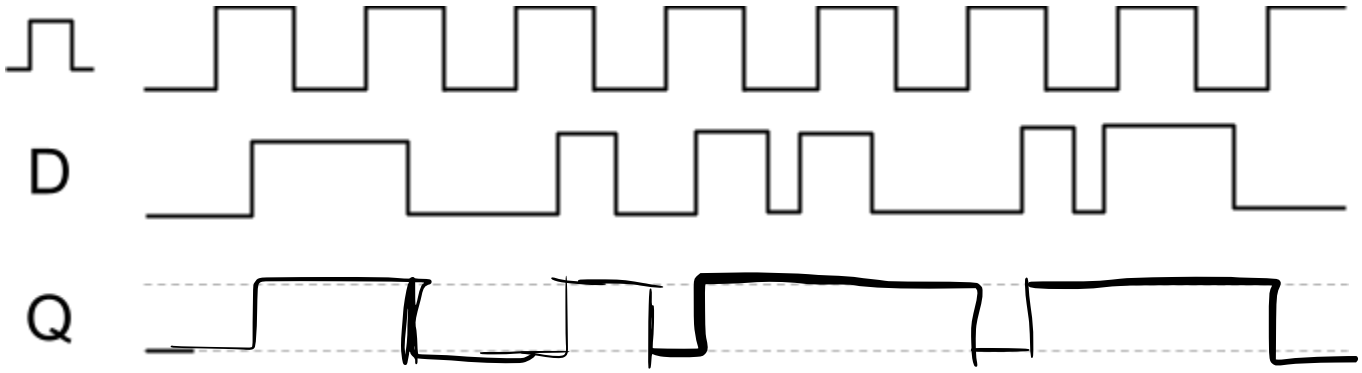
HW12: Sequential logic, clocks, triggers, flip-flops (CS220-04)

1) Complete the empty cells of the table below for an SR Latch. Use '?' in cells for which the correct answer could be 0 or 1. Assume the bit was a 1 just before this sequence starts.

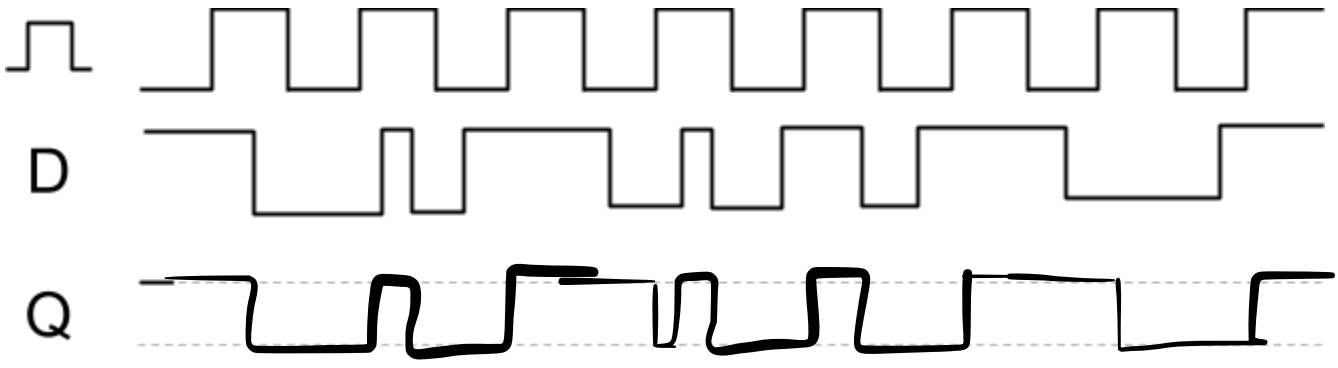
S	0	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	0
R	0	0	0	1	1	0	1	0	0	1	0	1	0	0	0	0	1	0	1	1	0
Q	1	1	1	0	0	0	0	?	?	0	0	0	0	0	1	1	0	1	0	0	0

*Assuming this is a sequence left-right, where Q and Qnot values remain in the circuit

2) Draw the curve of the bit Q given the D flip flop inputs below. Assume the bit Q starts with a value of 0.



3) Draw the curve of the bit Q given the D flip flop inputs below. ***This time***, assume the bit Q starts with a value of 1. Mwa-ha-ha-ha!



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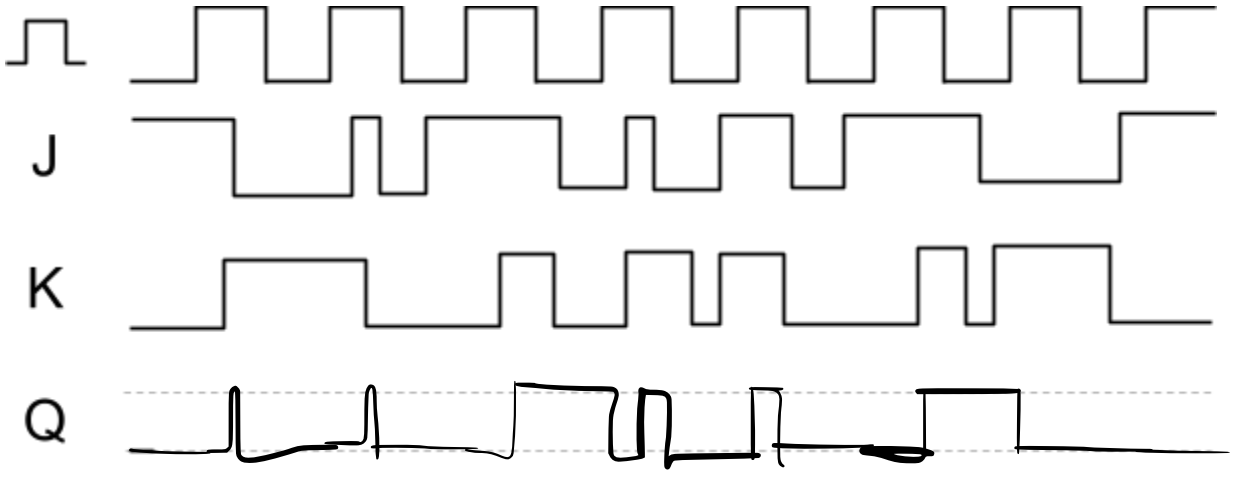
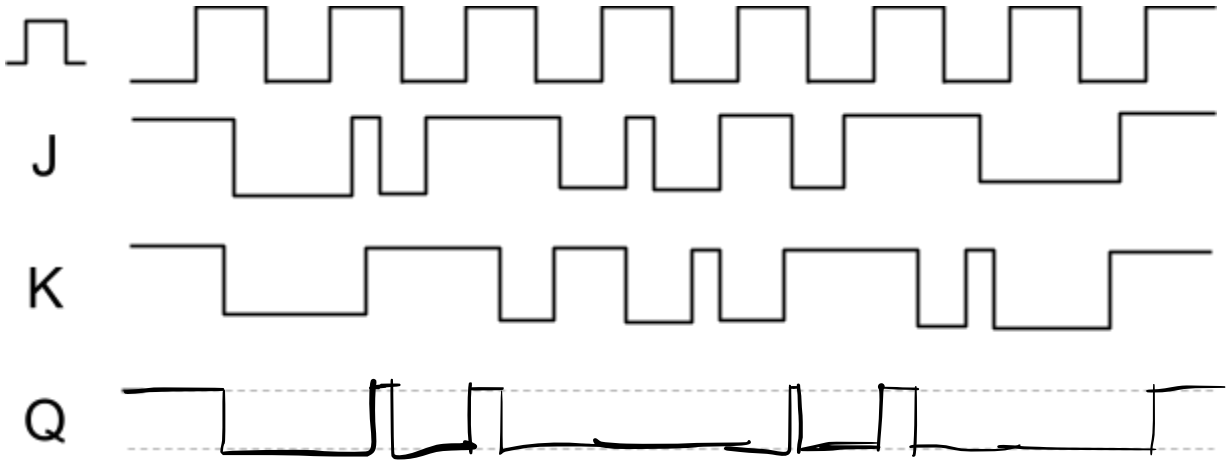
4) Draw the curve of the bit Q given the J-K flip flop inputs below. Assume the bit Q starts with a value of 0.



5) Draw the curve of the bit Q given the J-K flip flop inputs below. ***This time***, assume the bit Q starts with a value of 1. Mwa-ha-ha-ha!



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EXTRA CREDIT

6) The circuit below is NOT a clock circuit we've seen before. Show the alternate clock patterns at X and C. For X, remember a super tiny delay has been added by the inversions.