

Name: Ammaar Ahmad

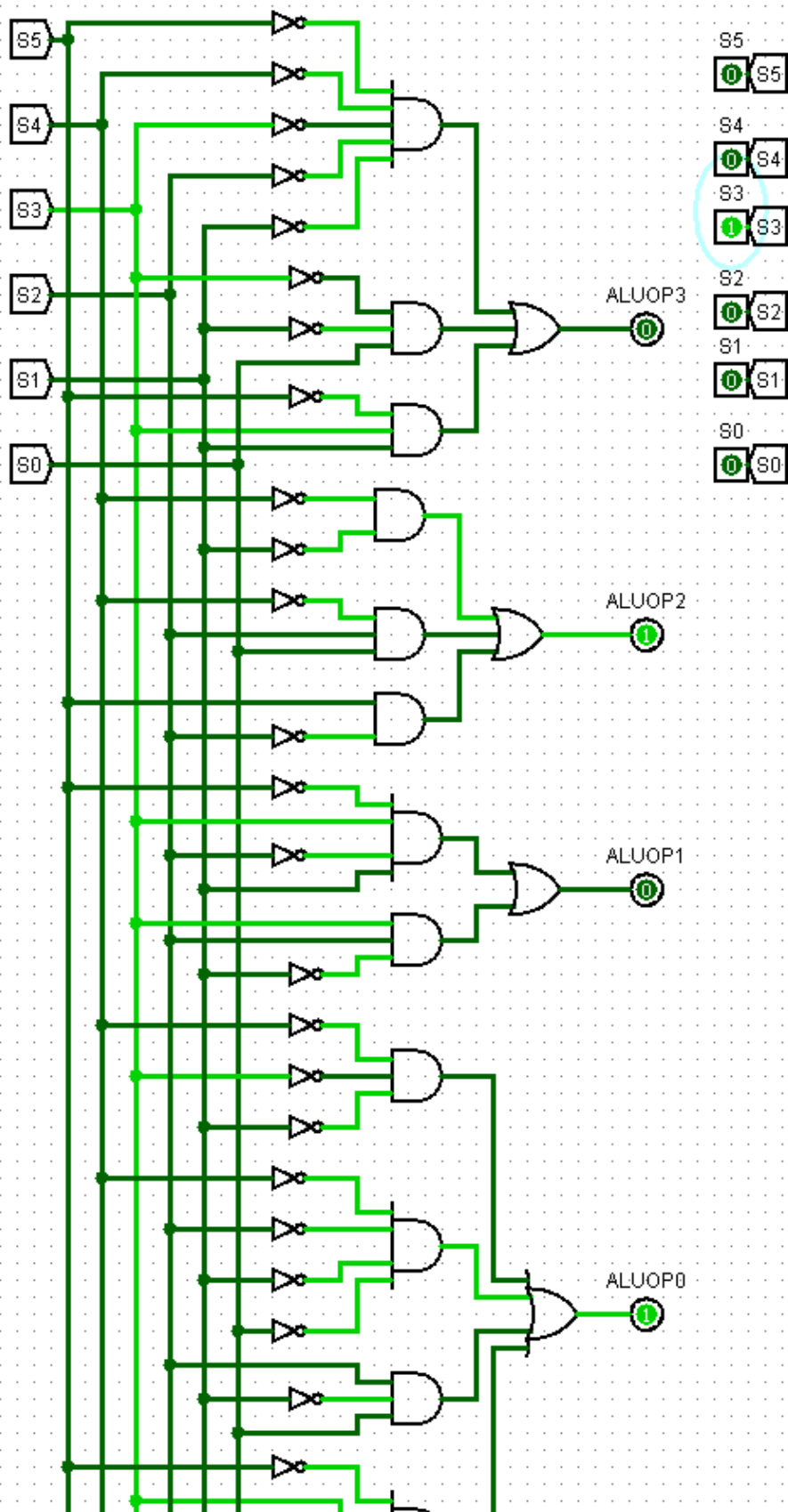
Roll No: 1801CS08

1. Instruction loaded at 0000 ROM

MIPS code	Machine Code
add \$s0, \$0, \$0	0x00008020
add \$s1, \$0, \$0	0x00008820
addi \$t0, \$0, 10	0x2008000A
loop:	
slt \$t1, \$s0, \$t0	0x0208482A
beq \$t1, \$0, done	0x11200003
add \$s1, \$s1, \$s0	0x02308820
addi \$s0, \$s0, 1	0x22100001
j loop	0x08000003
done:	

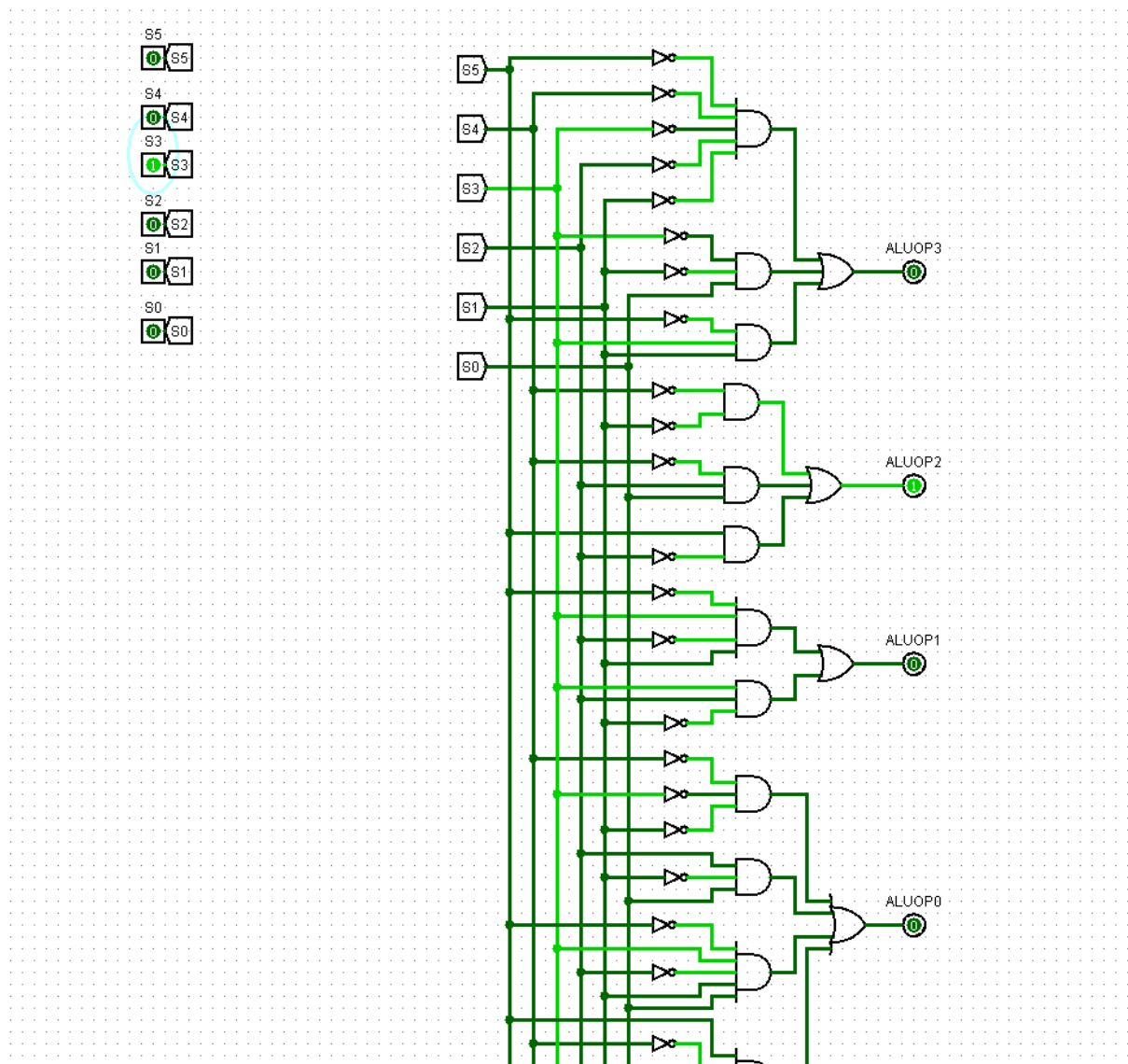
Initially there was an error in control decoder.

This instruction **addi** \$t0, \$0, 10 was doing subtraction instead of addition. Opcode: 001000, ALU: 0101



After rectification, it performs correctly Opcode: 001000

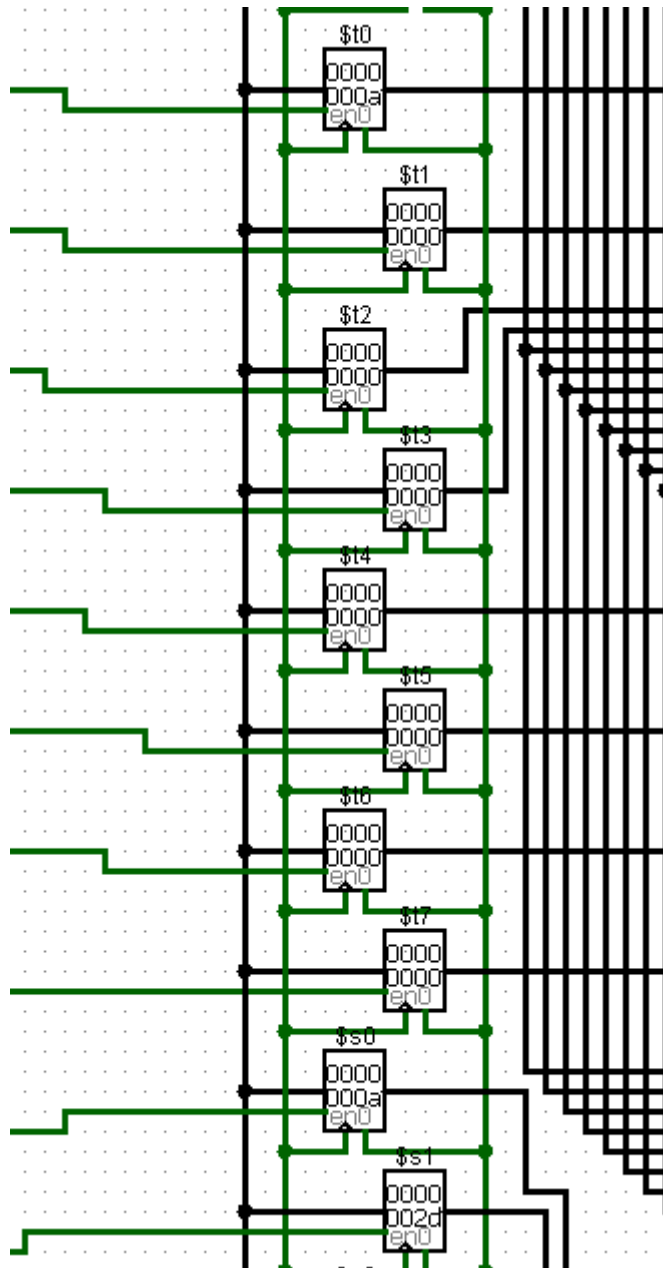
ALU: 0100



This program was adding whole numbers<10

Output \$t0=10(constant), \$t1=0(equality) \$s0=10

\$s1=45=2D(Hex) – Final Answer



2. Calculating Cycles in each type of processor

MIPS code	Machine Code	No. of cycles
add \$s0, \$0, \$0	0x00008020	1
add \$s1, \$0, \$0	0x00008820	1
addi \$t0, \$0, 10	0x2008000A	1
loop:		
slt \$t1, \$s0, \$t0	0x0208482A	11
beq \$t1, \$0, done	0x11200003	11
add \$s1, \$s1, \$s0	0x02308820	10
addi \$s0, \$s0, 1	0x22100001	10
j loop	0x08000003	10
done:		

No. of instructions: 55

No. of cycles in Single cycle processor: 55

CPI for Single cycle processor: 1

MIPS code	Machine Code	No. of cycles
add \$s0, \$0, \$0	0x00008020	1*4=4
add \$s1, \$0, \$0	0x00008820	1*4=4
addi \$t0, \$0, 10	0x2008000A	1*4=4
loop:		
slt \$t1, \$s0, \$t0	0x0208482A	11*4=44
beq \$t1, \$0, done	0x11200003	11*3=33
add \$s1, \$s1, \$s0	0x02308820	10*4=40
addi \$s0, \$s0, 1	0x22100001	10*4=40
j loop	0x08000003	10*3=30

No. of cycles in Multi cycle processor: 199

CPI for Multi cycle processor: $199/55=3.6$ (approx)

In Pipelined processor, beq instruction requires control hazard and is rectified by stalling until new PC is calculated (3 cycles)

MIPS code	Machine Code	No. of cycles
add \$s0, \$0, \$0	0x00008020	1*1=1
add \$s1, \$0, \$0	0x00008820	1*1=1
addi \$t0, \$0, 10	0x2008000A	1*1=1
loop:		
slt \$t1, \$s0, \$t0	0x0208482A	11*1=11
beq \$t1, \$0, done	0x11200003	11*4=44
add \$s1, \$s1, \$s0	0x02308820	10*1=10
addi \$s0, \$s0, 1	0x22100001	10*1=10
j loop	0x08000003	10*5=50

beq instruction stalls for 3 more cycle so 4 cycles per beq

j (jump) instruction waits for all instructions to complete that is stall for 4 cycles using total 5 cycles per jump instruction

Each instruction can take maximum 5 cycles for complete process but beq has no write back instructions to execute hence it completes in 4 cycles.

No. of cycles in Pipelined processor: 128

CPI for Multi cycle processor: $128/55=2.3$ (approx)

