J K Flipflop Truth Table after Stimulation

A	B	Q1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
1	1	0
1	1	1
0	1	1
0	1	0
0	0	0
1	0	0
1	0	1
0	0	1
0	1	1
0	1	0
1	1	0

1	1	1
1	1	0
1	1	1
0	1	1
0	1	0
0	0	0
1	0	0
1	0	1

SR Flipflop Truth Table after stimulation

C	D	Q2
0	0	0
1	0	0
1	0	1
1	1	1
0	1	1
0	1	0
0	0	0
0	1	0
1	1	0
1	0	0
0	0	0
0	1	0
1	1	0
1	0	0
1	0	1

0	0	1
0	1	1
0	1	0
1	1	0
0	1	0
0	0	0
1	0	0
1	0	1
0	0	1
1	0	1
1	1	1

D Flipflop Truth Table Stimulation

E	Q3
0	0
1	0
1	1
0	1
0	0
1	0
1	1
0	1
0	0
1	0
1	1
0	1
0	0

1	0
1	1
0	1
0	0
1	0
1	1
0	1
0	0
1	0
1	1
0	1
0	0
1	0
1	1

T Flipflop Truth Table after stimulation

F	Q4
0	0
1	0
1	1
1	0
1	1
1	0
0	0
1	0
1	1
1	0

1	1
1	0
0	0
1	0
1	1
0	1
1	1
1	0
1	1
1	0
1	1
1	0
1	1
1	0
1	1
0	1
1	1
1	0
0	0
1	0
1	1
1	0
1	1
1	0
1	1
1	0

1. 8 bit Shift Register Truth Table

A	O0	O1	O2	O3	O4	O5	O6	O7
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0
1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1
1	1	0	0	0	1	1	1	1
1	1	1	0	0	0	1	1	1
1	1	1	1	0	0	0	1	1
1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1

0	0	0	0	1	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0
0	0	0	1	1	0	0	0	0
1	0	0	1	1	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	1	0	0	1	1	0	0
1	1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1	1
1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1

2. 4 bit Parallel In Parallel Out Register

0 OR 1	RANDOM NUMBER	OUTPUT
1	1111	1111
1	1001	1111
1	1000	1001
1	0110	1000
1	1001	0110
1	0000	1001
1	1101	0000
1	1110	1101
0	1110	1101
0	1001	1101
0	1010	1101
1	1010	1101
1	1010	1010
1	0011	1010
1	1000	0011
1	1101	1000
1	1000	1101
1	0101	1000
1	1111	0101

1 0100 1111

1 0100 0100

1 1010 0100

Explanation: Due to clock it is retaining the any output for one cycle even if Input is changed in between. So output changes only after each clock cycle.

3. 6 bit counter using T flipflop Truth table

IN	S5	S4	S3	S2	S1	S0
1	1	1	1	1	1	1
1	1	1	1	1	1	0
1	1	1	1	1	0	1
1	1	1	1	1	0	0
1	1	1	1	0	1	1
1	1	1	1	0	1	0
1	1	1	1	0	0	1
1	1	1	1	0	0	0
1	1	1	0	1	1	1
1	1	1	0	1	1	0
1	1	1	0	1	0	1
1	1	1	0	1	0	0
1	1	1	0	0	1	1
1	1	1	0	0	1	0
1	1	1	0	0	0	1
1	1	1	0	0	0	0
1	1	0	1	1	1	1
1	1	0	1	1	1	0

1	1	0	1	1	0	1
1	1	0	1	1	0	0
1	1	0	1	0	1	1
1	1	0	1	0	1	0
1	1	0	1	0	0	1
1	1	0	1	0	0	0
1	1	0	0	1	1	1
1	1	0	0	1	1	0
1	1	0	0	1	0	1
1	1	0	0	1	0	0
1	1	0	0	0	1	1
1	1	0	0	0	1	0
1	1	0	0	0	0	1
1	1	0	0	0	0	0
1	0	1	1	1	1	1
1	0	1	1	1	1	0
1	0	1	1	1	0	1
1	0	1	1	1	0	0
1	0	1	1	0	1	1
1	0	1	1	0	1	0
1	0	1	1	0	0	1
1	0	1	1	0	0	0
1	0	1	0	1	1	1
1	0	1	0	1	1	0
1	0	1	0	1	0	1
1	0	1	0	1	0	0
1	0	1	0	0	1	1
1	0	1	0	0	1	0
1	0	1	0	0	0	1
1	0	1	0	0	0	0
1	0	0	1	1	1	1

1	0	0	1	1	1	0
1	0	0	1	1	0	1
1	0	0	1	1	0	0
1	0	0	1	0	1	1
1	0	0	1	0	1	0
1	0	0	1	0	0	1
1	0	0	1	0	0	0
1	0	0	0	1	1	1
1	0	0	0	1	1	0
1	0	0	0	1	0	1
1	0	0	0	1	0	0
1	0	0	0	0	1	1
1	0	0	0	0	1	0
1	0	0	0	0	0	1
1	0	0	0	0	0	0

EXPLANATION: COUNTING IS DONE IN REVERSE ORDER. WE CAN GET THE INCREASING BY USING INVERTORS. T FLIPFLOP TOGGLE THE INPUT WHEN IT IS 1 HENCE REVERSE ORDER IS OBTAINED. WHEN INPUT IS 0 PREVIOUS OUTPUT IS RETAINED.

5. 16 x 16 REGISTER USING 4X16 DECODER AND 16X1 MULTIPLEXER AND 16 BIT DATA INPUT. AFTER EACH CLOCK CYCLE DATA IS UPDATED ON THE SELECTED REGISTER USING DECODER TO CHOOSE THE REQUIRED REGISTER. AND FROM 16 REGISTERS DESIRED OUTPUT IS SELECTED USING MULTIPLEXER.