Q_D	Q_C	Q_B	Q_A	Q_D^+	Q_C^+	Q_B^+	Q_A^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

$Q_i \Rightarrow$ Current State

$Q_i^+ \Rightarrow$ Next State

4 Bit Synchronous Counter Basic Truth Table

S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	X	0	X	0	X	1	0
0	X	0	X	1	0	0	1
0	X	0	X	X	0	1	0
0	X	1	0	0	1	0	1
0	X	X	0	0	X	1	0
0	X	X	0	1	0	0	1
0	X	X	0	X	0	1	0
0	0	0	1	0	1	0	1
X	0	0	X	0	X	1	0
X	0	0	X	1	0	0	1
X	0	0	X	X	0	1	0
X	0	1	0	0	1	0	1
X	0	X	0	0	X	1	0
X	0	X	0	1	0	0	1
X	0	X	0	X	0	1	0
1	0	0	1	0	1	0	1

Truth Table for SR Flip Flop used in 4 Bit Synchronous Counter

SR Flip Flop Simplification

	00	01	11	10
00			1	
01			1	
11	X	X		X
10	X	X	X	X

$S_D = \overline{\varphi_D}\,\varphi_C\varphi_B\varphi_A$

	00	01	11	10
00			1	
01	X	X		X
11	X	X		X
10			1	

$S_C = \overline{\varphi_C}\,\varphi_B\,\varphi_A$

	00	01	11	10
00		1		X
01		1		X
11		1		X
10		1		X

$S_B = \overline{\varphi_B}\,\varphi_A$

	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

$R_A = \varphi_A$

$\varphi_D\varphi_C$ \ $\varphi_B\varphi_A$	00	01	11	10
00	X		1	
01	X		1	
11	X		1	
10	X		1	

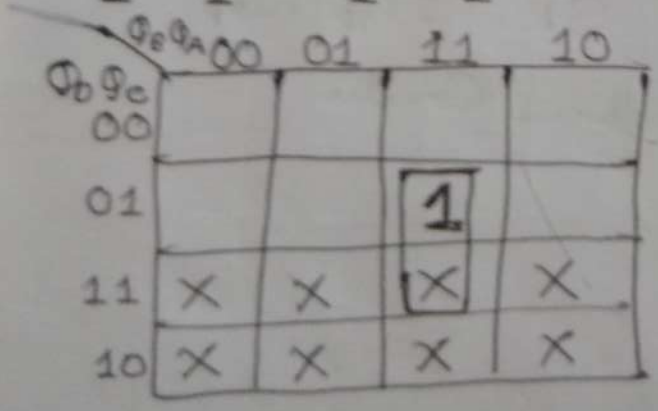
$R_B = \varphi_A\varphi_B$

	00	01	11	10
00	X	X		X
01			1	
11			1	
10	X	X		X

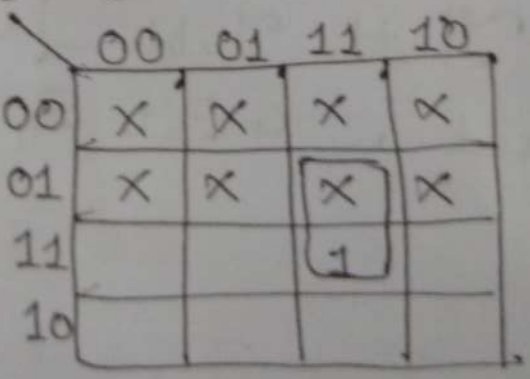
$R_C = \varphi_A\varphi_B\varphi_C$

	00	01	11	10
00	X	X	X	X
01	X	X		X
11			1	
10				

Q_D	Q_C	Q_B	Q_A	Q_D^+	Q_C^+	Q_B^+	Q_A^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

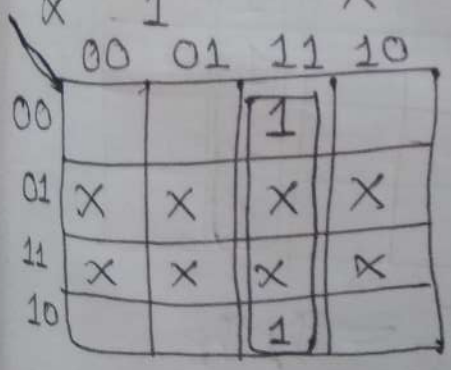


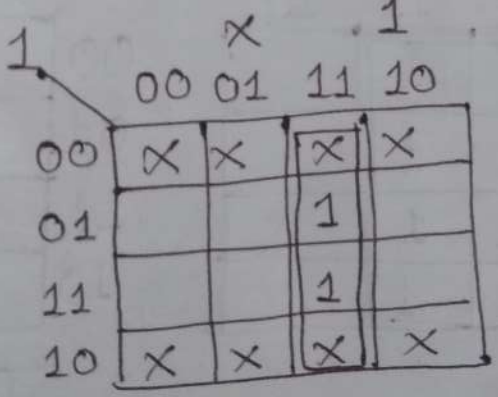
$J_D = Q_C Q_B Q_A$



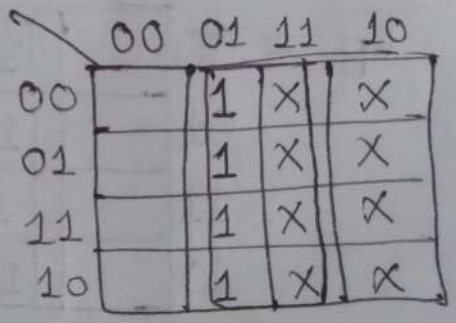
$K_D = Q_C Q_B Q_A$

J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	X	0	X	0	X	1	X
0	X	0	X	1	X	X	1
0	X	0	X	X	0	1	X
0	X	1	X	X	1	X	1
0	X	X	0	0	X	1	X
0	X	X	0	1	X	X	1
0	X	X	0	X	0	1	X
0	X	X	1	X	1	X	1
1	X	0	X	0	X	1	X
X	0	0	X	1	X	X	1
X	0	0	X	X	0	1	X
X	0	0	X	X	1	X	1
X	0	1	X	0	X	1	X
X	0	X	0	1	X	X	1
X	0	X	0	X	0	1	X
X	0	X	0	X	1	X	1
X	1	X	1	1	X		



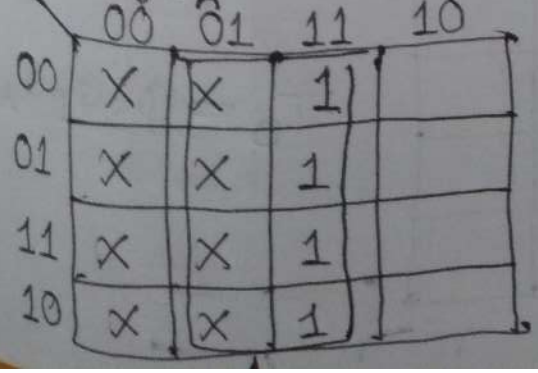


$K_C = Q_B Q_A$



$J_B = Q_A$

$J_C = Q_B Q_A$



$K_B = Q_A$

From Table it is clear that

$J_A = K_A = 1$ (Always)

Q_D	Q_C	Q_B	Q_A	Q_D^+	Q_C^+	Q_B^+	Q_A^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

$Q_i \Rightarrow$ Current State

$Q_i^+ \Rightarrow$ Next State

4 Bit Synchronous Counter Basic Truth Table

T_D	T_C	T_B	T_A	D_D	D_C	D_B	D_A
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	0	1	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	1	0	1	1	1
0	0	1	1	1	0	0	0
1	1	0	1	1	0	0	1
0	0	1	1	1	0	1	0
0	1	0	1	1	0	1	1
0	0	1	1	1	1	0	0
0	1	0	1	1	1	0	1
0	0	1	1	1	1	1	0
0	1	0	1	1	1	1	1
0	0	1	1	0	0	0	0
1	1	0	1				

T Flip Flop Simplification

$T_A = 1$ (Always)

$T_B =$

	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

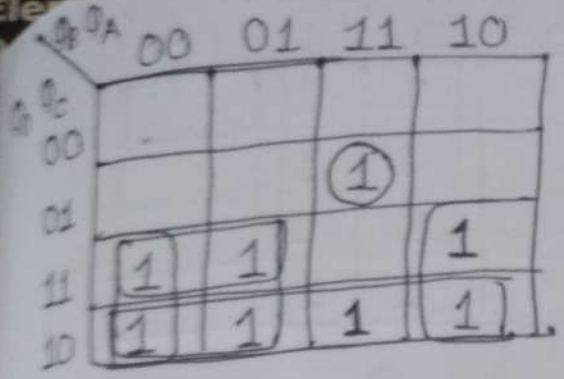
$T_C = Q_A Q_B$

	00	01	11	10
00			1	
01			1	
11			1	
10			1	

$T_B = Q_A$

	00	01	11	10
00				
01			1	
11			1	
10				

$T_D = Q_C Q_B Q_A$

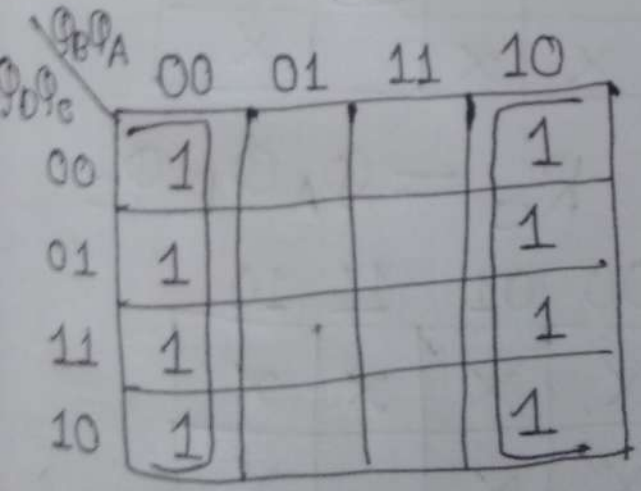


$$D_D = Q_D \bar{Q}_C + Q_D \bar{Q}_A + Q_D Q_C \bar{Q}_B + \bar{Q}_D Q_C Q_B Q_A$$

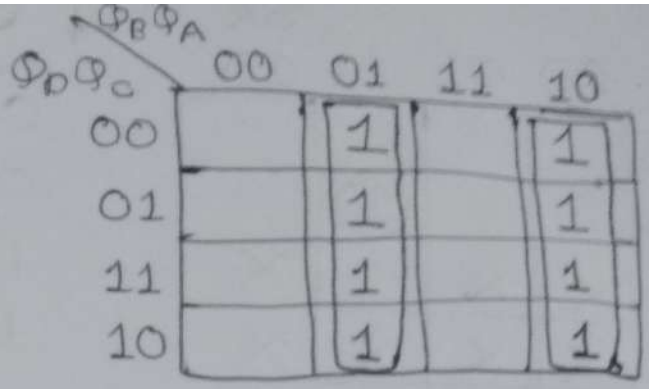
$$\Rightarrow Q_D (\bar{Q}_C + \bar{Q}_B + \bar{Q}_A) + \bar{Q}_D Q_C Q_B Q_A$$

$$\Rightarrow Q_D (Q_C Q_B Q_A)' + \bar{Q}_D (Q_C Q_B Q_A)$$

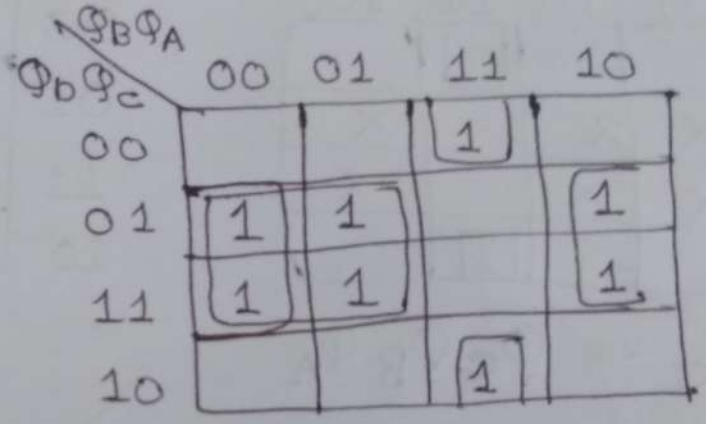
$$\Rightarrow Q_D \oplus (Q_A \cdot Q_B \cdot Q_C)$$



$$D_A = \bar{Q}_A$$



$$D_B = \bar{Q}_B Q_A + Q_A \bar{Q}_B = Q_B \oplus Q_A$$



$$D_C = Q_C \bar{Q}_B + Q_C \bar{Q}_A + \bar{Q}_C Q_A Q_B$$

$$= Q_C (\bar{Q}_B + \bar{Q}_A) + \bar{Q}_C Q_A Q_B$$

$$= Q_C (Q_A Q_B)' + \bar{Q}_C Q_A Q_B$$

$$= Q_C \oplus (Q_A Q_B)$$

Simplified Circuit of Synchron 4 Bit Counter using K Map Simplification for D Flip Flop

Q3) ALU Table

Selector lines					Output
S_4	S_3	S_2	S_1	S_0	
	0	0	0	0	Addition
	0	0	0	1	Subtraction
	0	0	1	0	Multiplication
	0	0	1	1	Division
	0	1	0	0	Bitwise AND
	0	1	0	1	Bitwise NAND
	0	1	1	0	Bitwise OR
	0	1	1	1	Bitwise NOR
	1	0	0	0	Bitwise XOR
	1	0	0	1	Bitwise XNOR
	1	0	1	0	Checking A<B (Comparator)

Rest Inputs are Invalid

When $S_2 = 0$ $S_3 = 0$ and $S_1 = 1$ Multiplexer 2×1 is Enabled to

S_0	Output
0	16 Bit Carry Over for Multiplication
1	16 Bit Remainder for Division