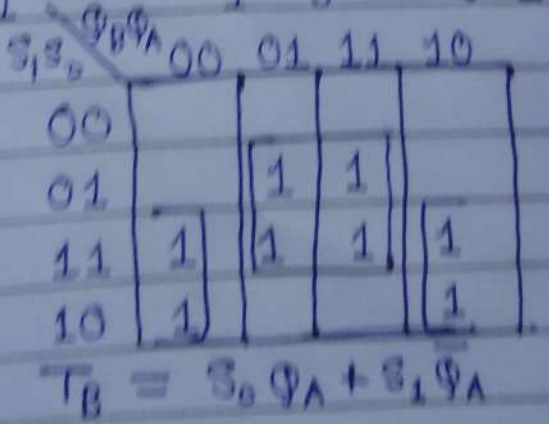
Lab 10

	S_1	S_0	Q_B	Q_A	Q_B^+	Q_A^+	T_B	T_A	D_B	D_A
No Counting – Memory State										
	0	0	0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	0	1
	0	0	1	0	1	0	0	0	1	0
	0	0	1	1	1	1	0	0	1	1
Count up by 1										
	0	1	0	0	0	1	0	1	0	1
	0	1	0	1	1	0	1	1	1	0
	0	1	1	0	1	1	0	1	1	1
	0	1	1	1	0	0	1	1	0	0
Count down by 1										
	1	0	0	0	1	1	1	1	1	1
	1	0	0	1	0	0	0	1	0	0
	1	0	1	0	0	1	1	1	0	1
	1	0	1	1	1	0	0	1	1	0
Count by 2										
	1	1	0	0	1	0	1	0	1	0
	1	1	0	1	1	1	1	0	1	1
	1	1	1	0	0	0	1	0	0	0
	1	1	1	1	0	1	1	0	0	1

$T_A = S_1 \oplus S_0$



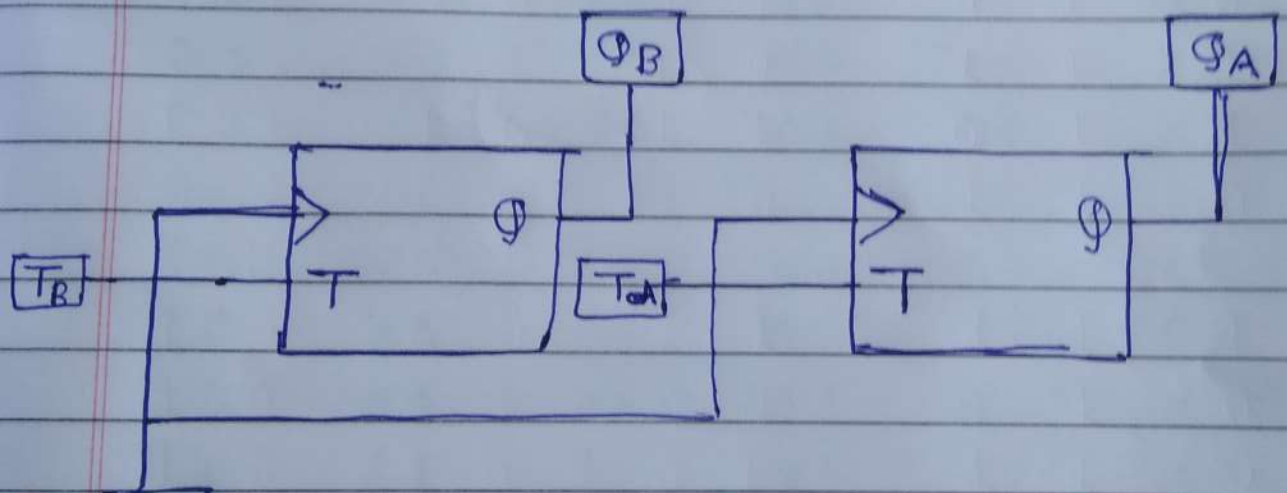
$T_B = S_0 Q_A + S_1 \bar{Q}_A$

S_1S_0 \ Q_BQ_A	00	01	11	10
00		1	1	
01	1			1
11		1	1	
10	1			1

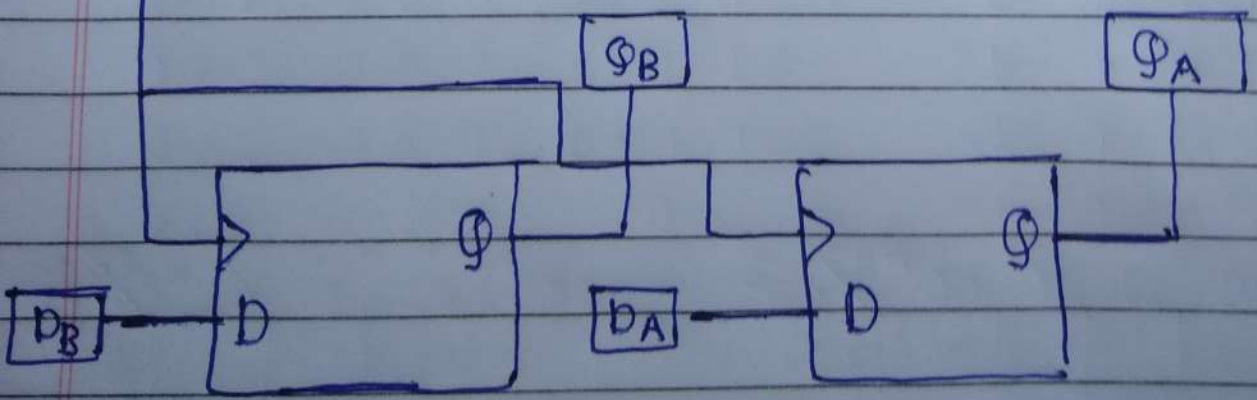
S_1S_0 \ Q_BQ_A	00	01	11	10
00			1	1
01		1		1
11	1	1		
10	1		1	

$$D_A = \bar{S}_1\bar{S}_0Q_A + \bar{S}_1S_0\bar{Q}_A + S_1S_0Q_A + S_1\bar{S}_0Q_A$$
$$= S_1 \oplus S_0 \oplus Q_A$$

$$D_B = \bar{S}_1Q_B\bar{Q}_A + S_1\bar{Q}_B\bar{Q}_A + \bar{S}_0Q_BQ_A + S_0\bar{Q}_BQ_A$$
$$= \bar{Q}_A(S_1 \oplus Q_B) + Q_A(S_0 \oplus Q_B)$$



2 bit Counter using T flip flop



2 bit Counter using D flip flop

2 bit Counter using JK and SR Flip Flop

S_1	S_0	Q_B	Q_A	Q_B^+	Q_A^+	$S_B R_B$	$S_A R_A$	$J_B K_B$	$J_A K_A$
0	0	0	0	0	0	0X	0X	0X	0X
0	0	0	1	0	1	0X	X0	0X	X0
0	0	1	0	1	0	X0	0X	X0	0X
0	0	1	1	1	1	X0	X0	X0	X0
0	1	0	0	0	1	0X	10	0X	1X
0	1	0	1	1	0	10	01	1X	X1
0	1	1	0	1	1	X0	10	X0	1X
0	1	1	1	0	0	01	01	X1	X1
1	0	0	0	1	1	10	10	1X	1X
1	0	0	1	0	0	0X	01	0X	X1
1	0	1	0	0	1	01	10	X1	1X
1	0	1	1	1	0	X0	01	X0	X1
1	1	0	0	1	0	10	0X	1X	0X
1	1	0	1	1	1	10	X0	1X	X0
1	1	1	0	0	0	01	0X	X1	0X
1	1	1	1	0	1	01	X0	X1	X0

S_1S_0 \ Q_BQ_A	00	01	11	10
00		X	X	
01	1			1
11		X	X	
10	1			1

$S_A = \overline{Q_A}(S_1 \oplus S_0)$

S_1S_0 \ Q_BQ_A	00	01	11	10
00	X			X
01		1	1	
11	X			X
10		1	1	

$R_A = Q_A(S_1 \oplus S_0)$

S_1S_0 \ Q_BQ_A	00	01	11	10
00			X	X
01		1		X
11	1	1		
10	1		X	

$$S_B = S_1\overline{Q_B}\,\overline{Q_A} + S_0\overline{Q_B}\,Q_A$$
$$= \overline{Q_B}\,(S_1\overline{Q_A} + S_0 Q_A)$$

S_1S_0 \ Q_BQ_A	00	01	11	10
00	X	X		
01	X		1	
11			1	1
10		X		1

$$R_B = S_0 Q_B Q_A + S_1 Q_B \overline{Q_A}$$
$$= Q_B (S_0 Q_A + S_1 \overline{Q_A})$$

S_1S_0 \ Q_BQ_A	00	01	11	10
00		X	X	
01	1	X	X	1
11		X	X	
10	1	X	X	1

S_1S_0 \ Q_BQ_A	00	01	11	10
00	X			X
01	X	1	1	X
11	X			X
10	X	1	1	X

$$J_A = S_1 \oplus S_0$$

S_1S_0 \ Q_BQ_A	00	01	11	10
00			X	X
01		1	X	X
11	1	1	X	X
10	1		X	X

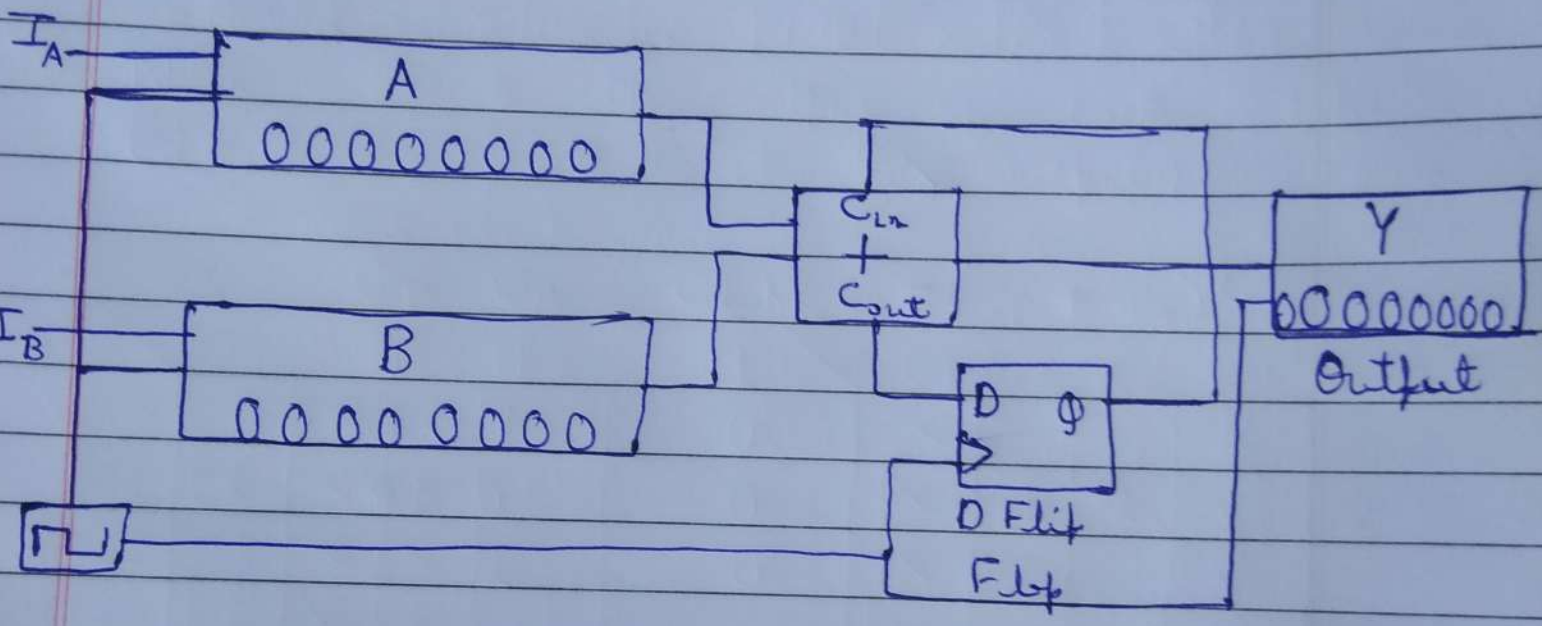
$$K_A = S_1 \oplus S_0$$

S_1S_0 \ Q_BQ_A	00	01	11	10
00	X	X		
01	X	X	1	
11	X	X	1	1
10	X	X		1

$$J_B = S_0 Q_A + S_1 \overline{Q_A}$$

$$K_B = S_0 Q_A + S_1 \overline{Q_A}$$

Q2. Deigning of 8 bit adder using 1 Full Adder and Shift Register



A, B and Y are Shift Register

It will require 8 clock pulses for complete addition of $Y = A + B$.

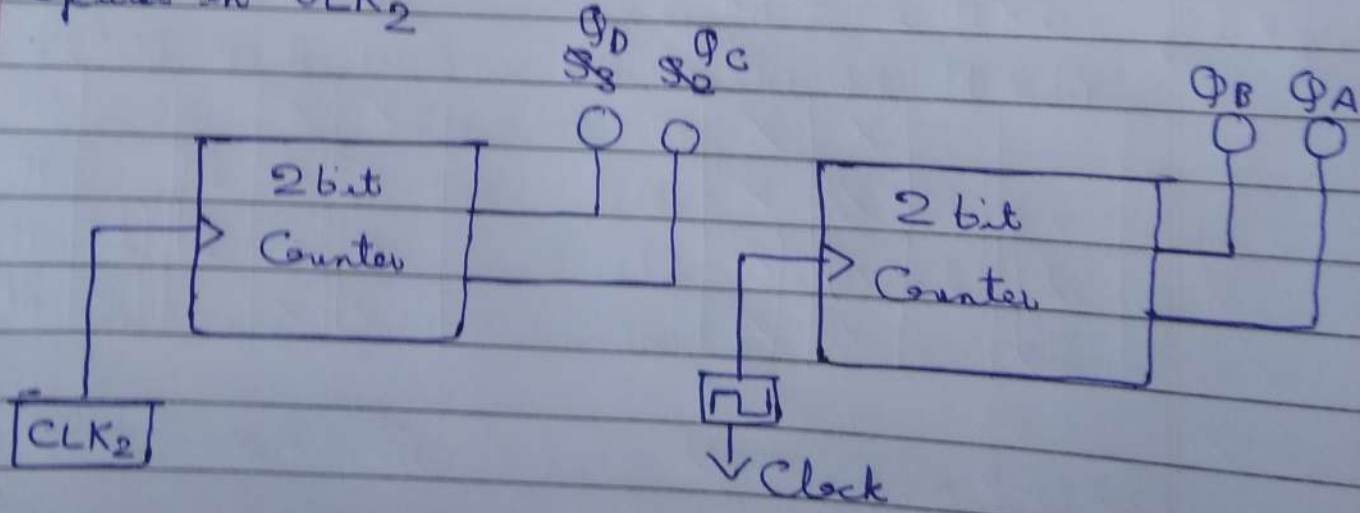
If we use a FA which is capable of adding more No. of bits, then consequently No. of clock required will reduce proportionately

Q3) 4 Bit Counter using 2 bit counter

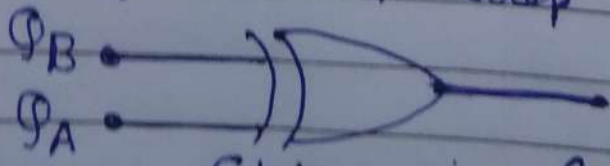
Since for every 4 pulses in Least Significant Bit we need a pulse in Most Significant 2 bit we use NOR gate to the output of last 2 bits (Least Significant Counter as Output)

Q_B	Q_A	CLK_2	$=(Q_B + Q_A)'$
0	0	1	
0	1	0	
1	0	0	
1	1	0	

As we can see that for every 4 pulse we get 1 pulse in CLK_2



2 bit using D Flip Flop



CLK_2 using $(Q_B + Q_A)'$