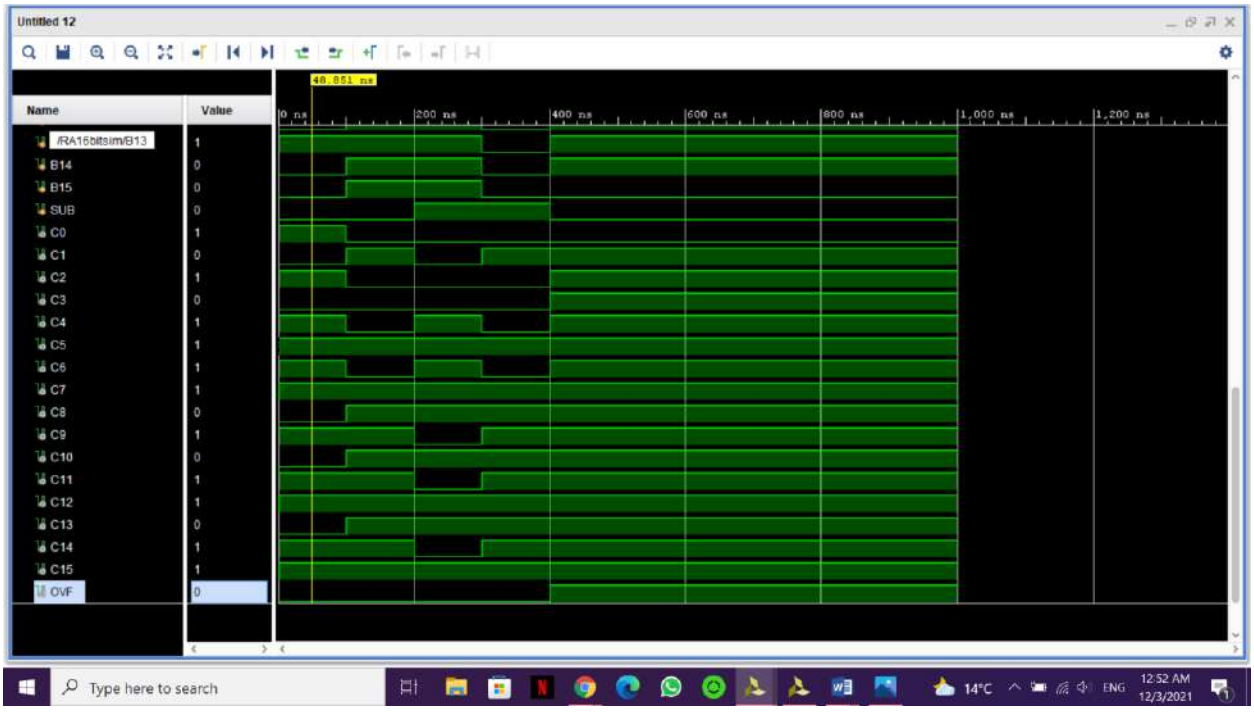
CS303-LOGIC & DIGITAL SYSTEM DESIGN

Lab 3 Report

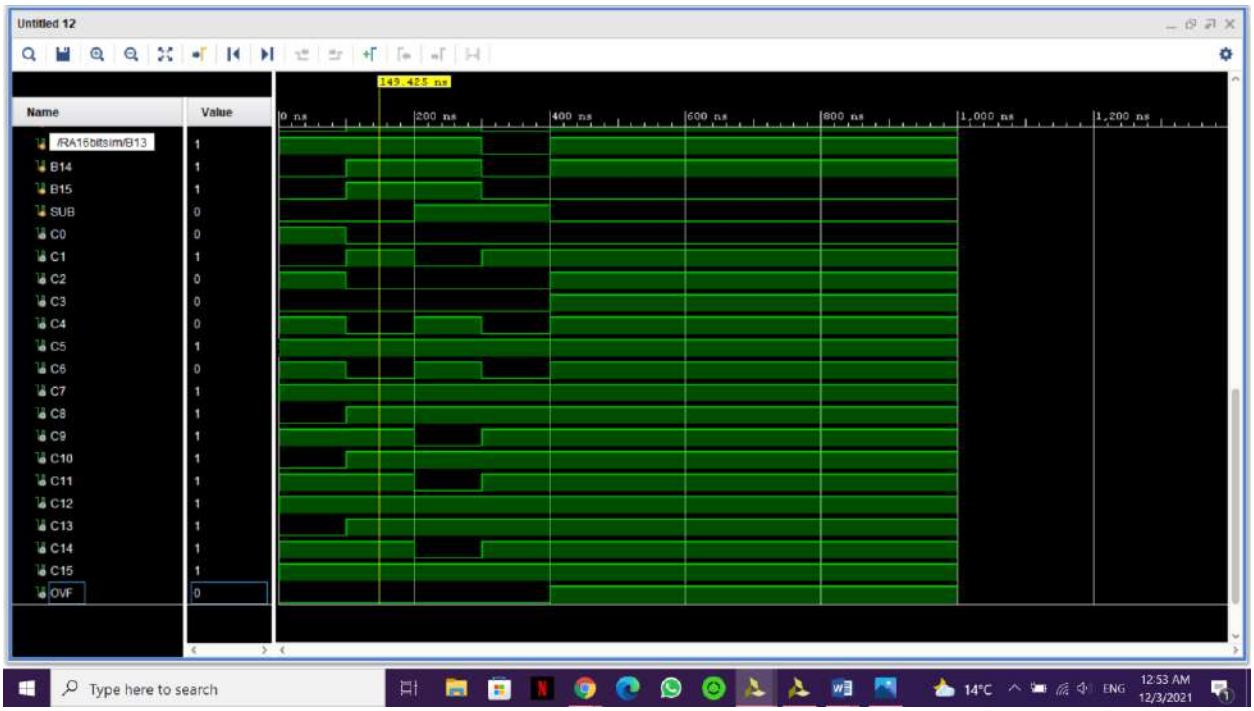
In this lab I designed two circuits that can both add and subtract two 16-bit integers with overflow detection. The first circuit which is a ripple carry adder-subtractor utilizes 16 full adders. The second design is a hybrid adder-subtractor uses 4, 4-bit carry look ahead adders.

1) 16-bit ripple-carry adder-subtractor using full adders

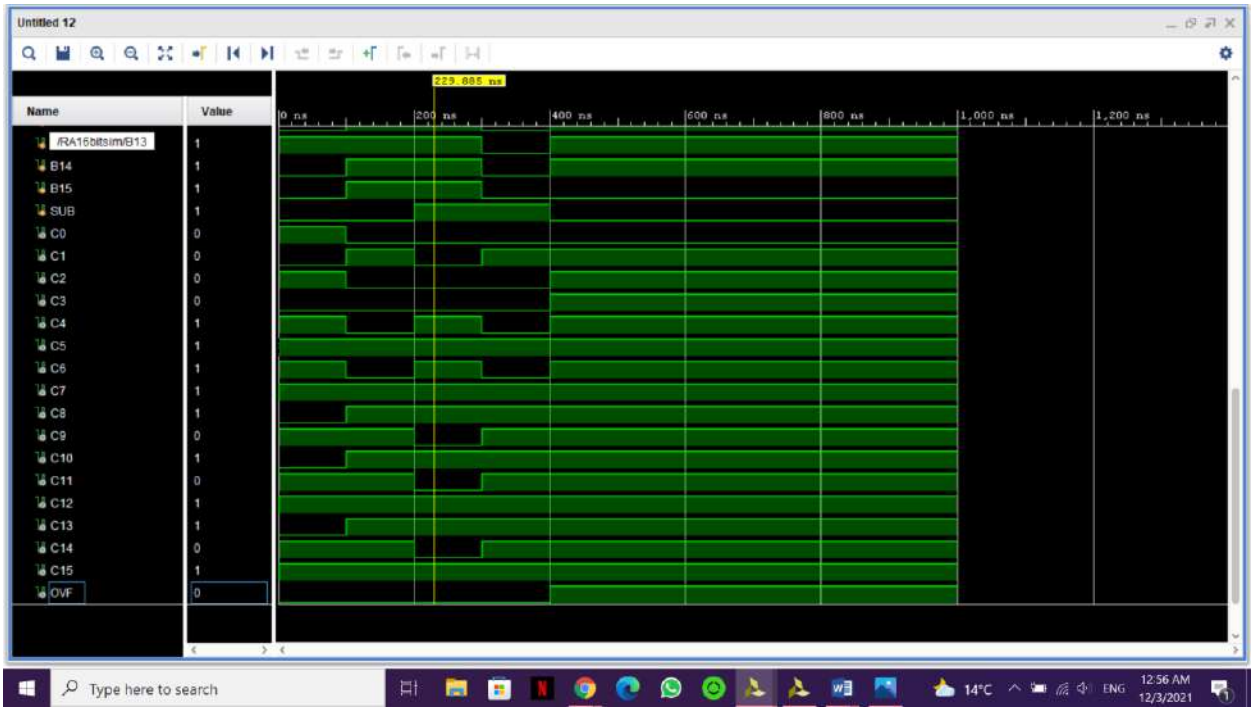
i. A = -18969
B = 9483
SUB = 0
C = 1101101011110101 = -9483
OVF = 0



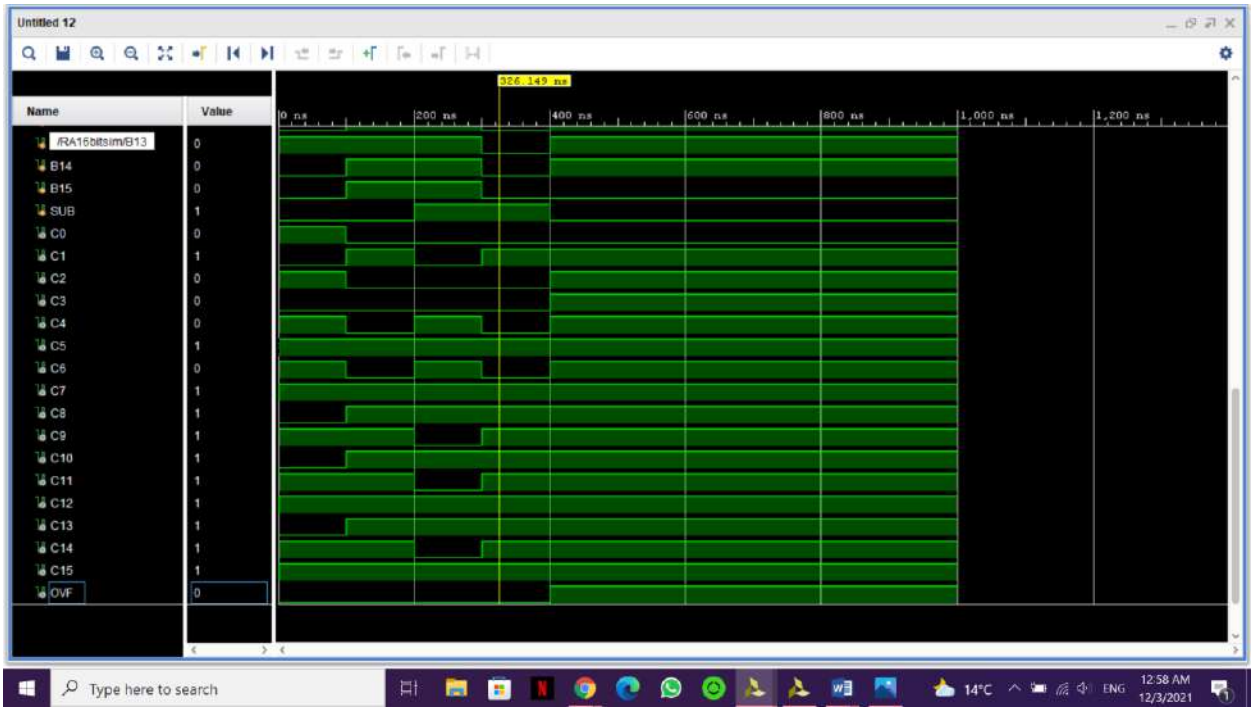
ii. A = 153
B = -247
SUB = 0
C = 1111111110100010 = -94
OVF = 0



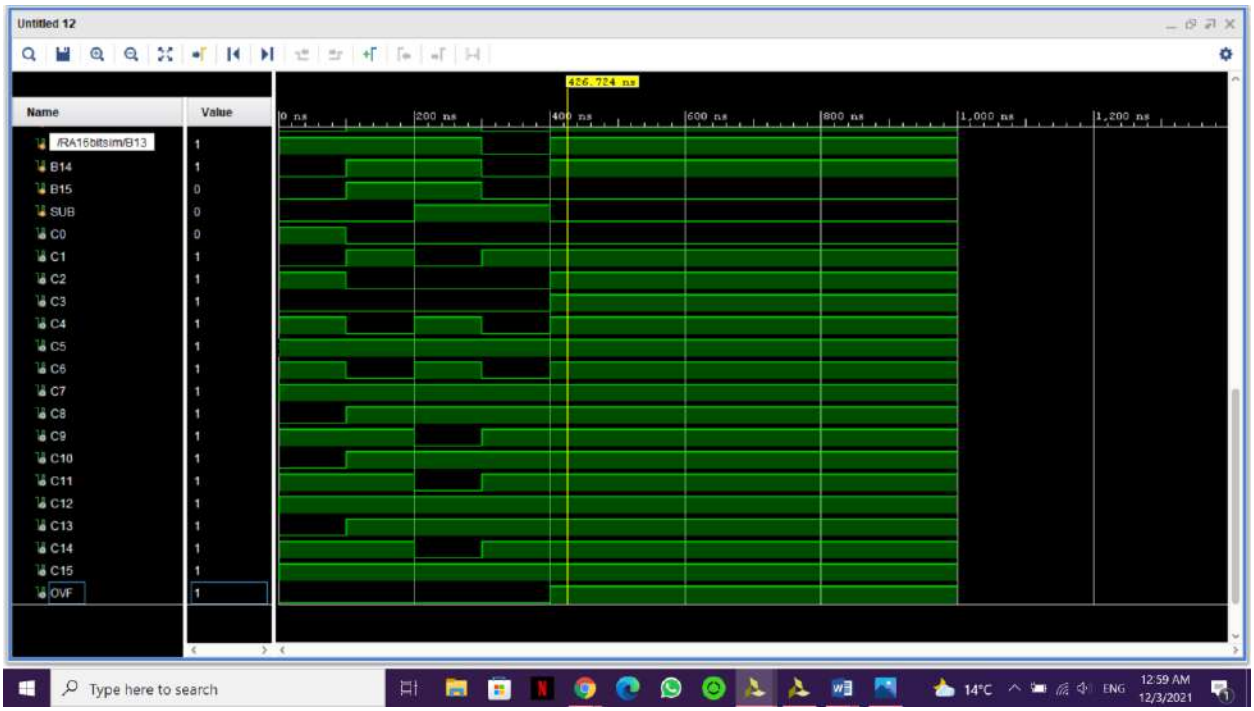
iii. A = -18966
B = -6
SUB = 1
C = 1011010111110000 = -18960
OVF = 0



iv. A = 256
B = 350
SUB = 1
C = 1111111110100010 = -94
OVF = 0

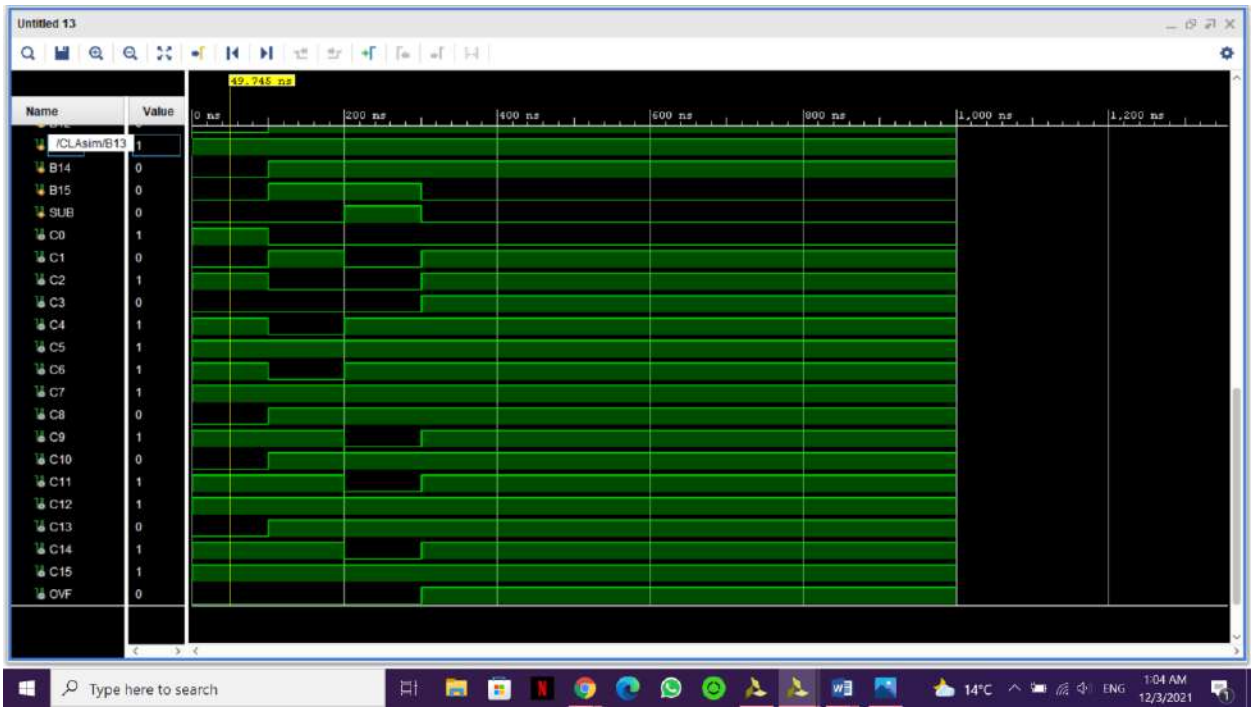


v. A = 327676
B = 32767
SUB = 1
OVF = 1

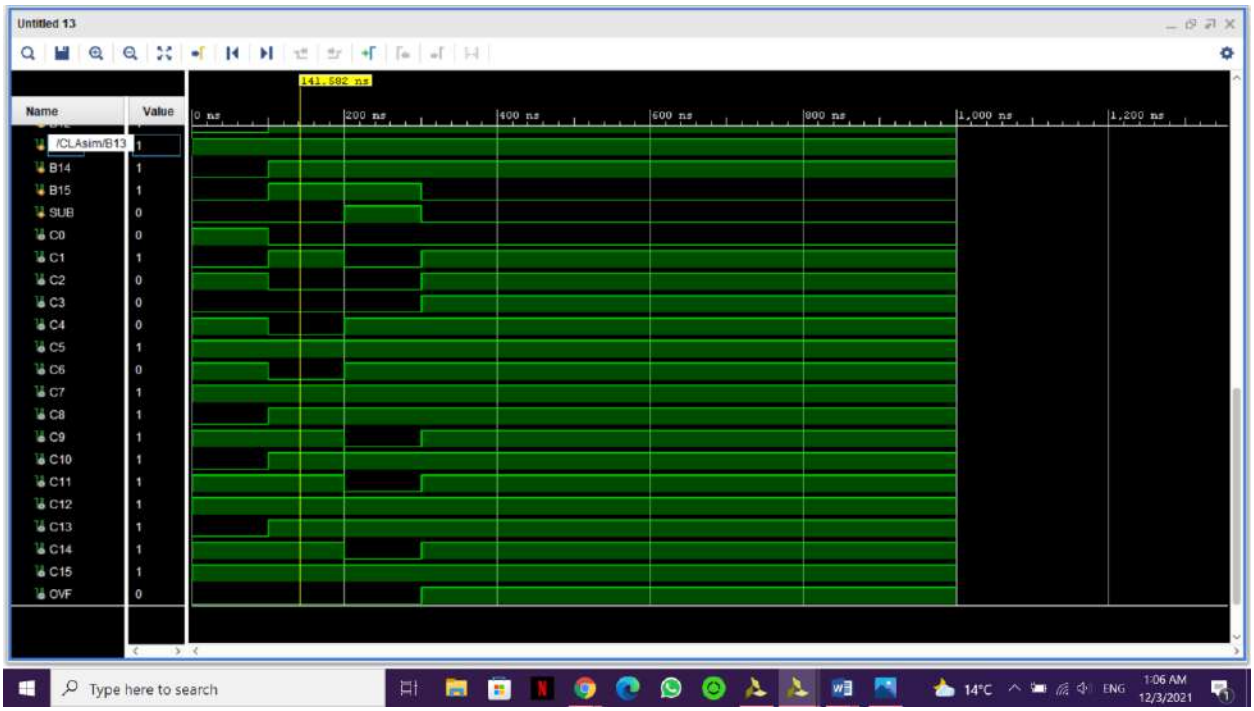


2) 16-bit hybrid adder-subtractor using four 4-bit carry lookahead adders (CLAs)

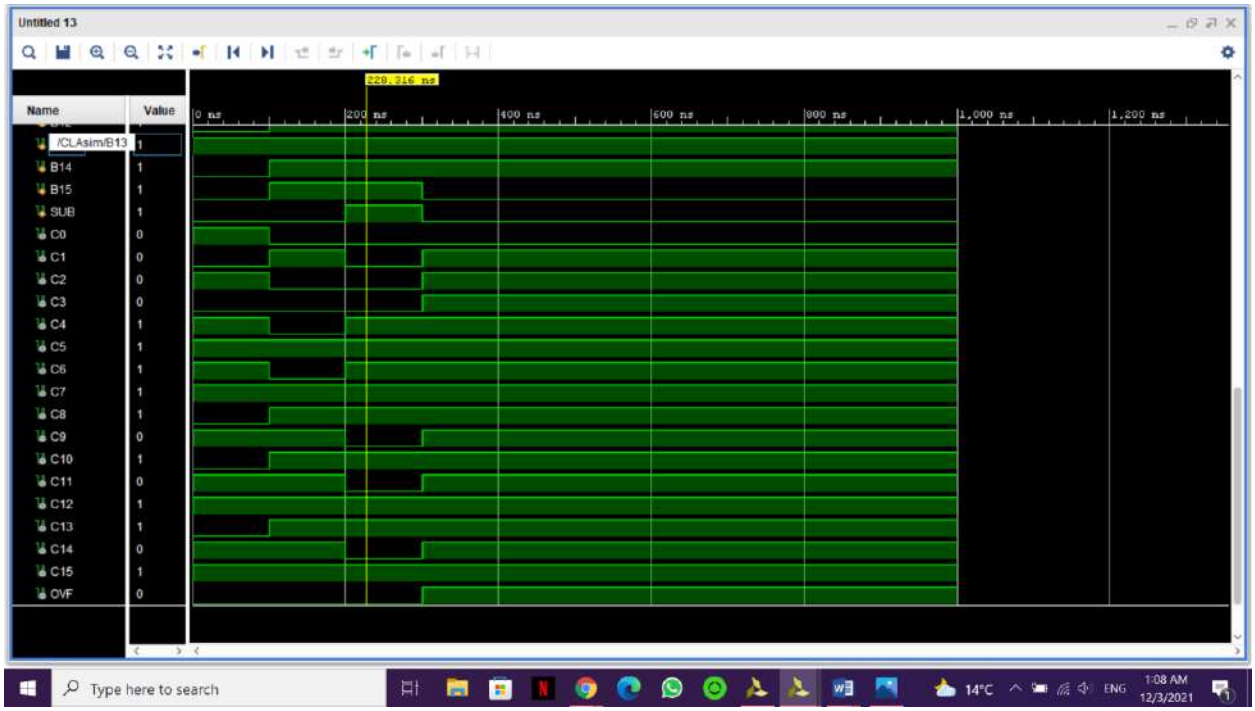
i. A = -18969
B = 9483
SUB = 0
C = 1101101011110101 = -9483
OVF = 0



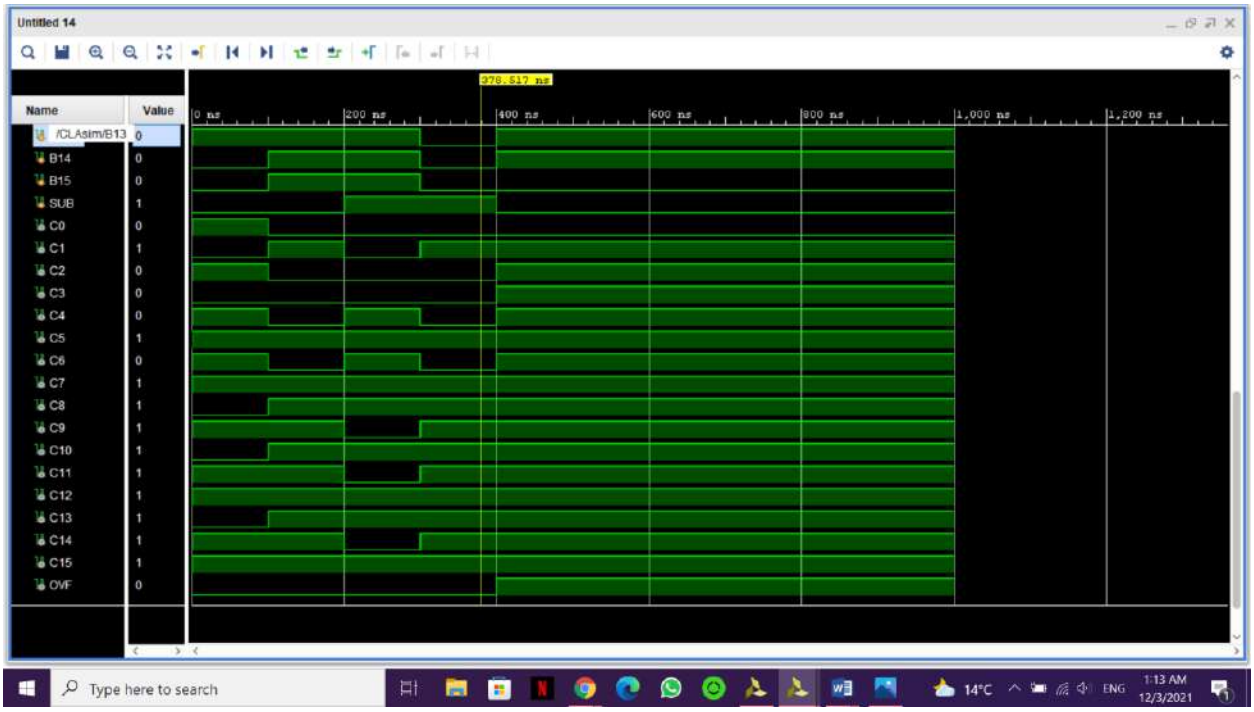
ii. A = 153
B = -247
SUB = 0
C = 1111111110100010 = -94
OVF = 0



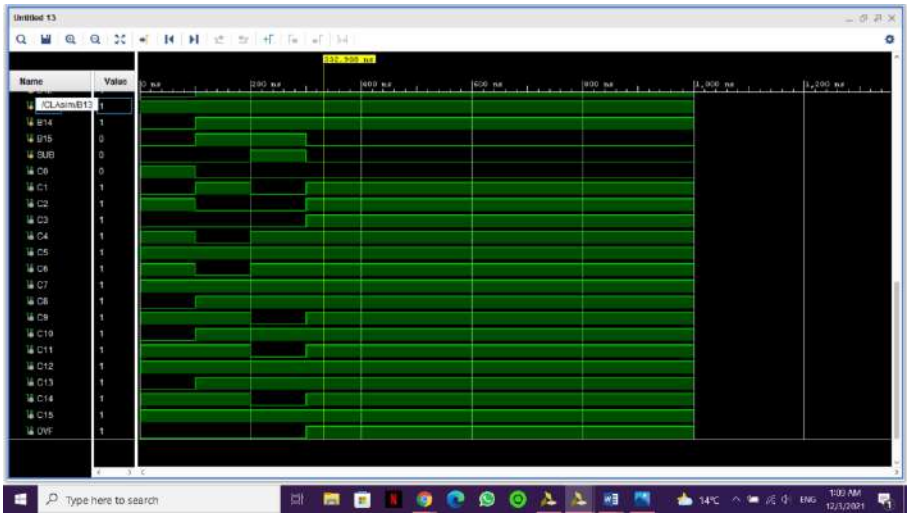
iii. A = -18966
B = -6
SUB = 1
C = 1011010111110000 = -18960
OVF = 0



iv. A = 256
B = 350
SUB = 1
C = 1111111110100010 = -94
OVF = 0



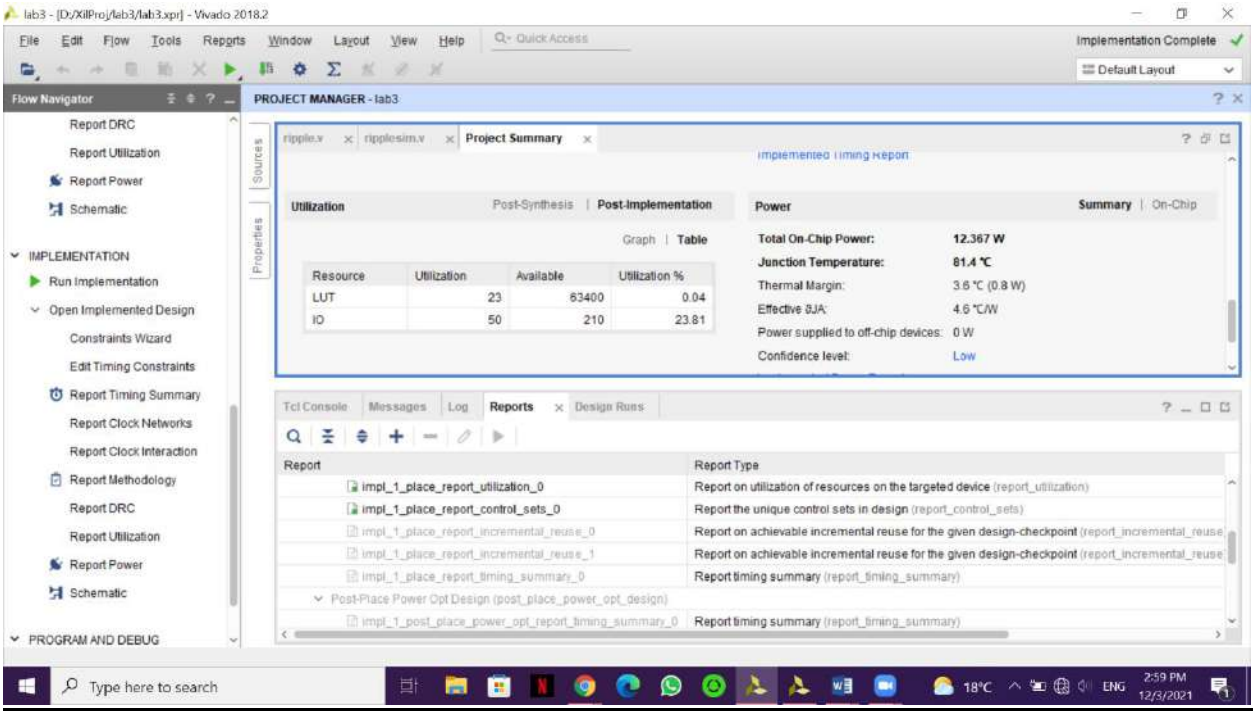
v. A = 327676
B = 32767
SUB = 1
OVF = 1



Implementation

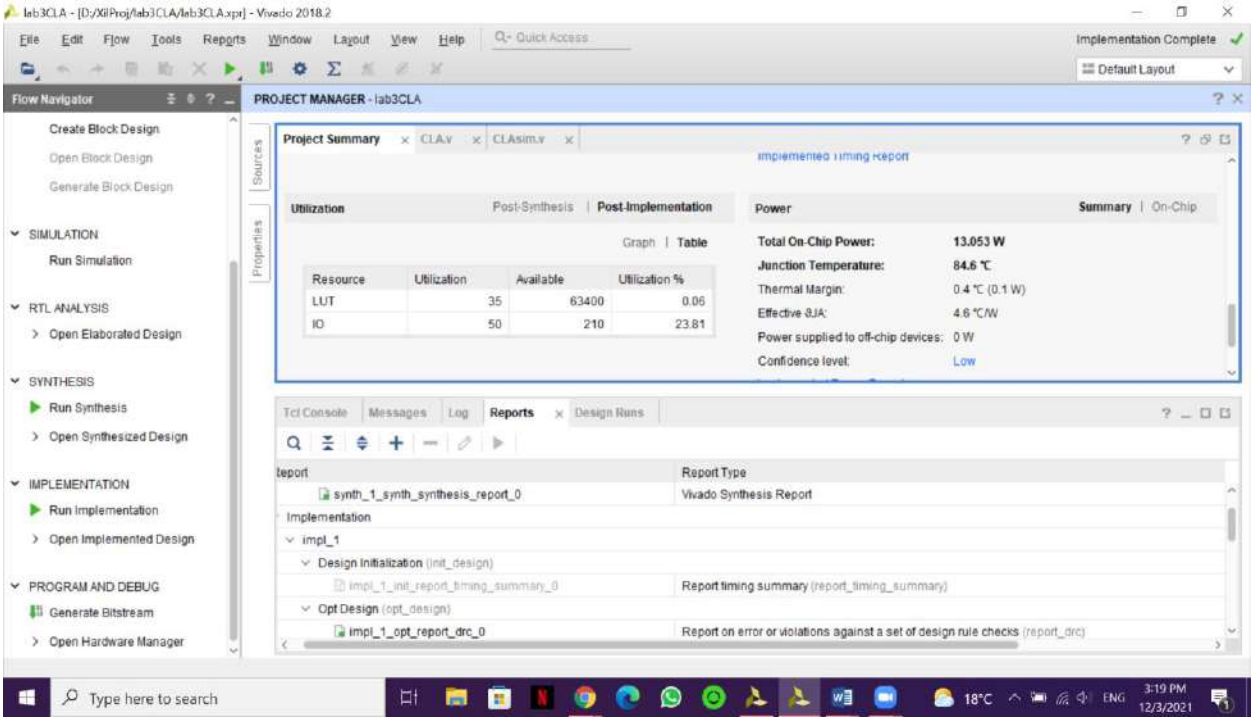
1) <u>16-bit ripple-carry adder-subtractor using full adders</u>

Number of LUTs = 23



2) 16-bit hybrid adder-subtractor using four 4-bit carry lookahead adders (CLAs)

Number of LUTs = 35



Results

Design 1 is better in terms of area as it utilizes 23LUTs and design 2 has 35LUTs therefore the shorter the area, the better and less complex the design. However, design 2 is better in terms of time delay as it uses Carry lookahead adders, therefore the propagation delay is reduced and it works faster than design 1. As a result, we will decide on which adder/subtractor to use after considering if time delay is the main priority or if area is the main priority.