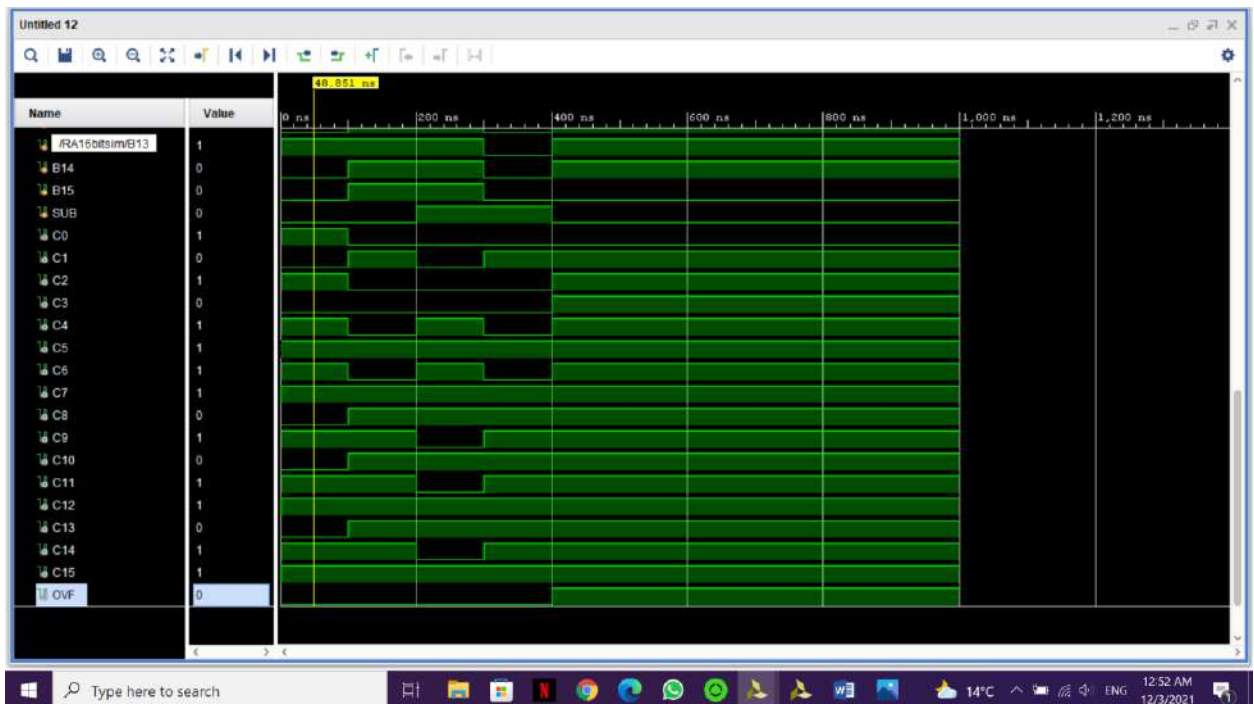


Lab 3 Report

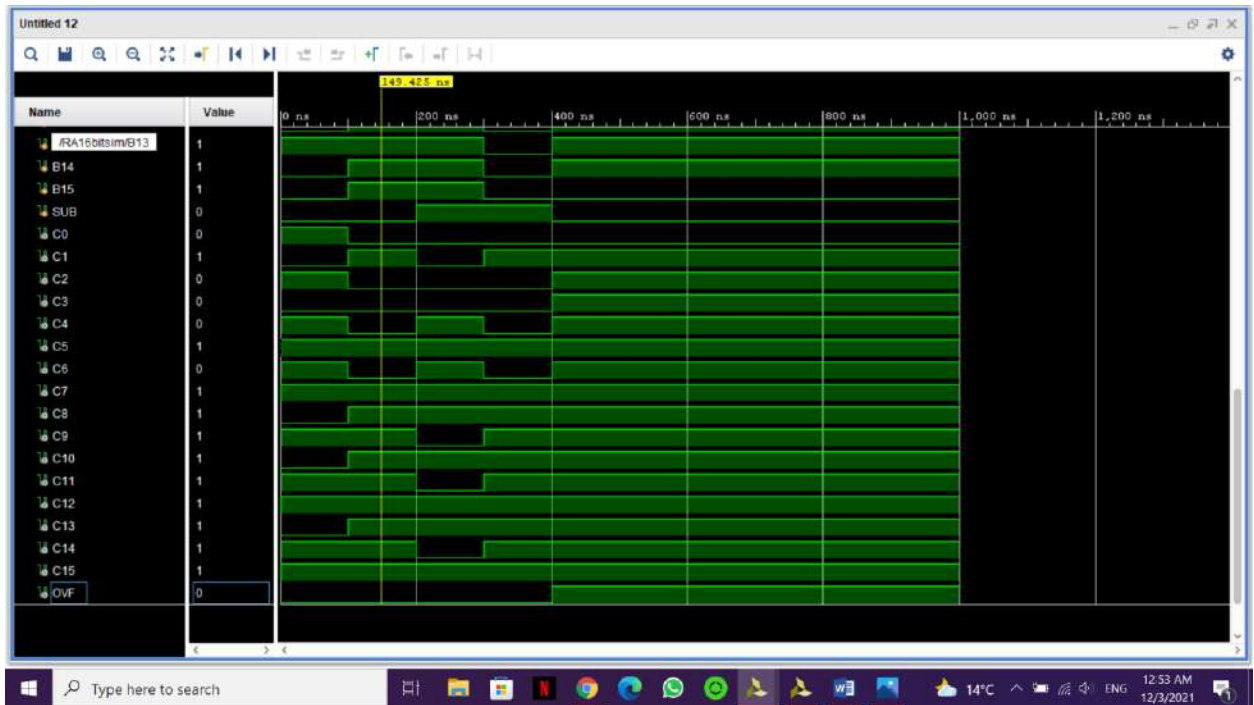
In this lab I designed two circuits that can both add and subtract two 16-bit integers with overflow detection. The first circuit which is a ripple carry adder-subtractor utilizes 16 full adders. The second design is a hybrid adder-subtractor uses 4, 4-bit carry look ahead adders.

1) 16-bit ripple-carry adder-subtractor using full adders

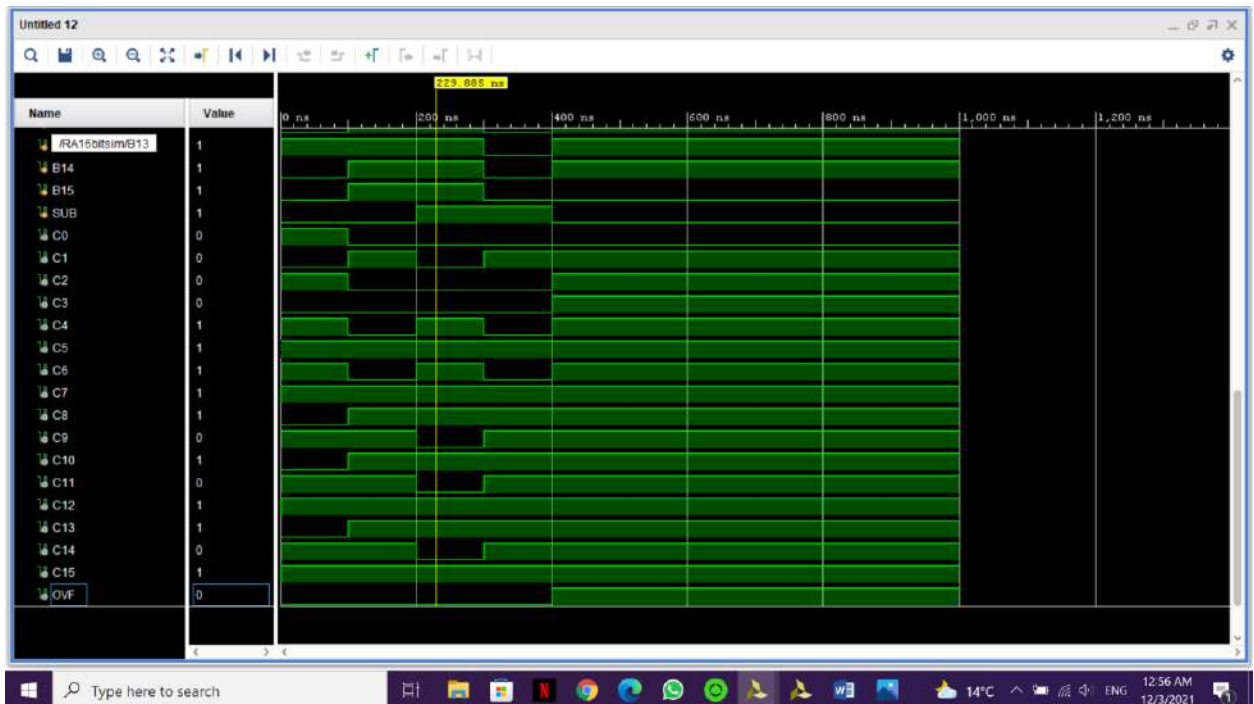
- i. A = -18969
 B = 9483
 SUB = 0
 C = 1101101011110101 = -9483
 OVF = 0



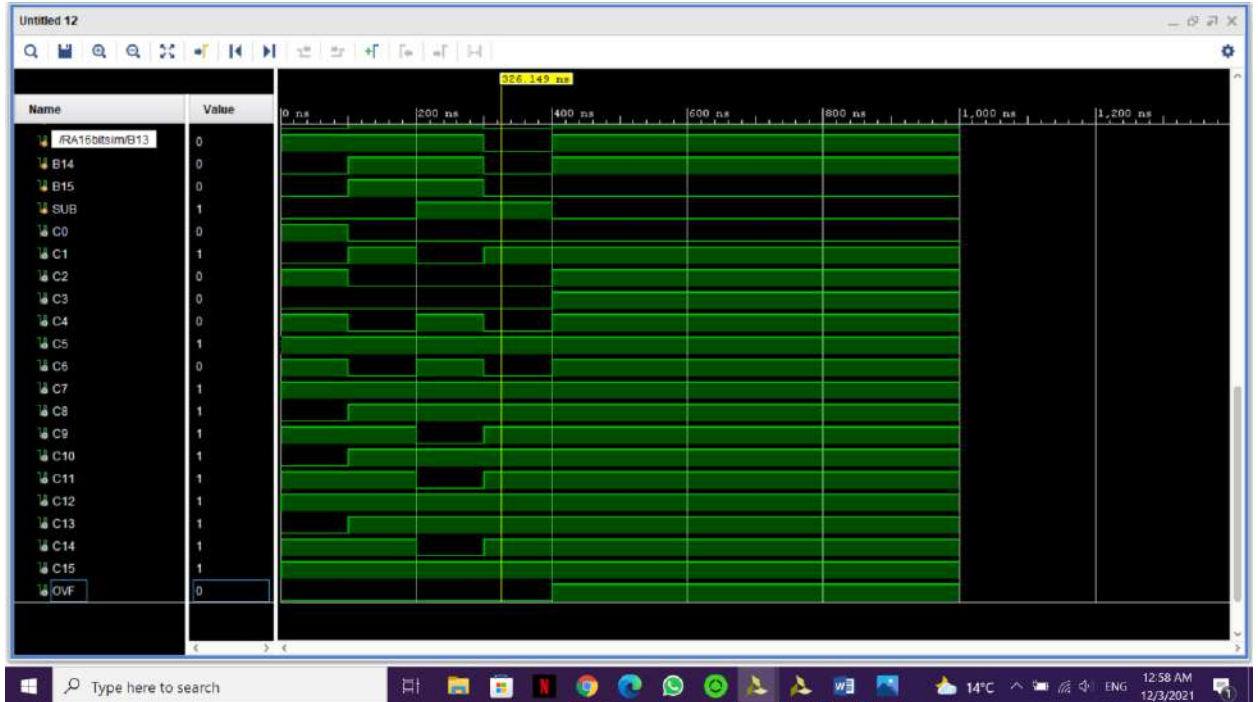
- ii. A = 153
 B = -247
 SUB = 0
 C = 11111111110100010 = -94
 OVF = 0



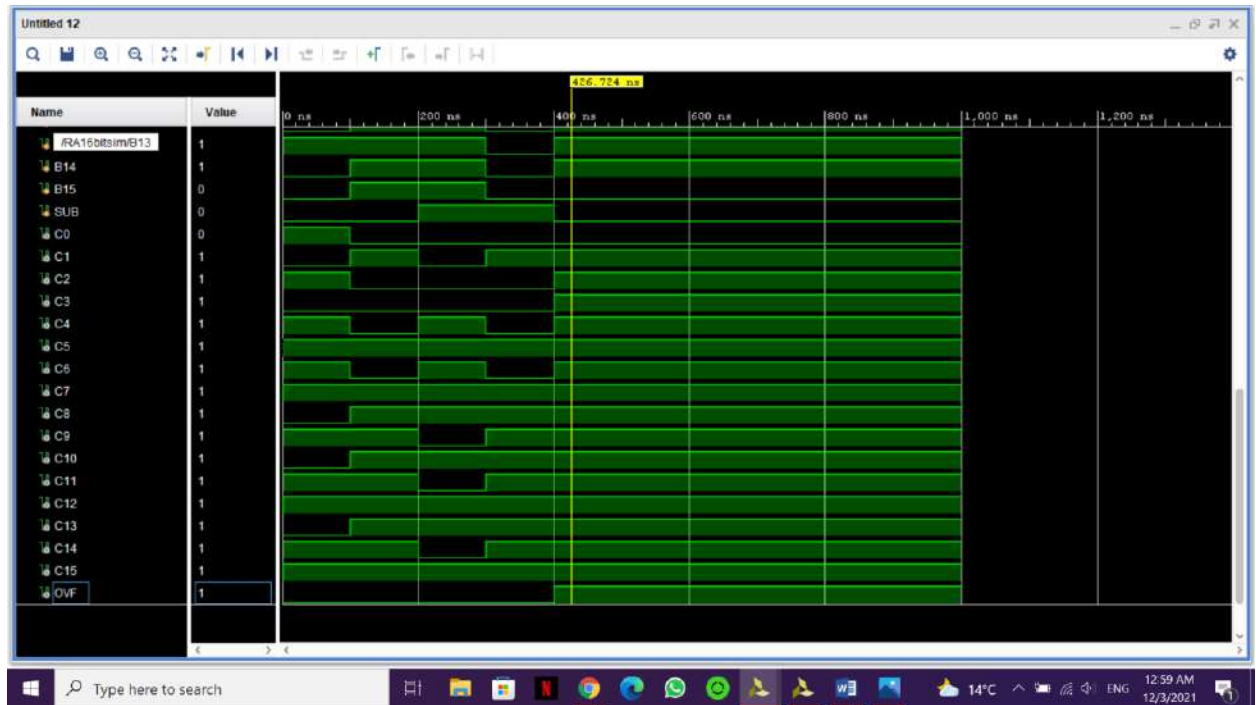
- iii. A = -18966
 B = -6
 SUB = 1
 C = 1011010111110000 = -18960
 OVF = 0



- iv. A = 256
 B = 350
 SUB = 1
 C = 1111111110100010 = -94
 OVF = 0

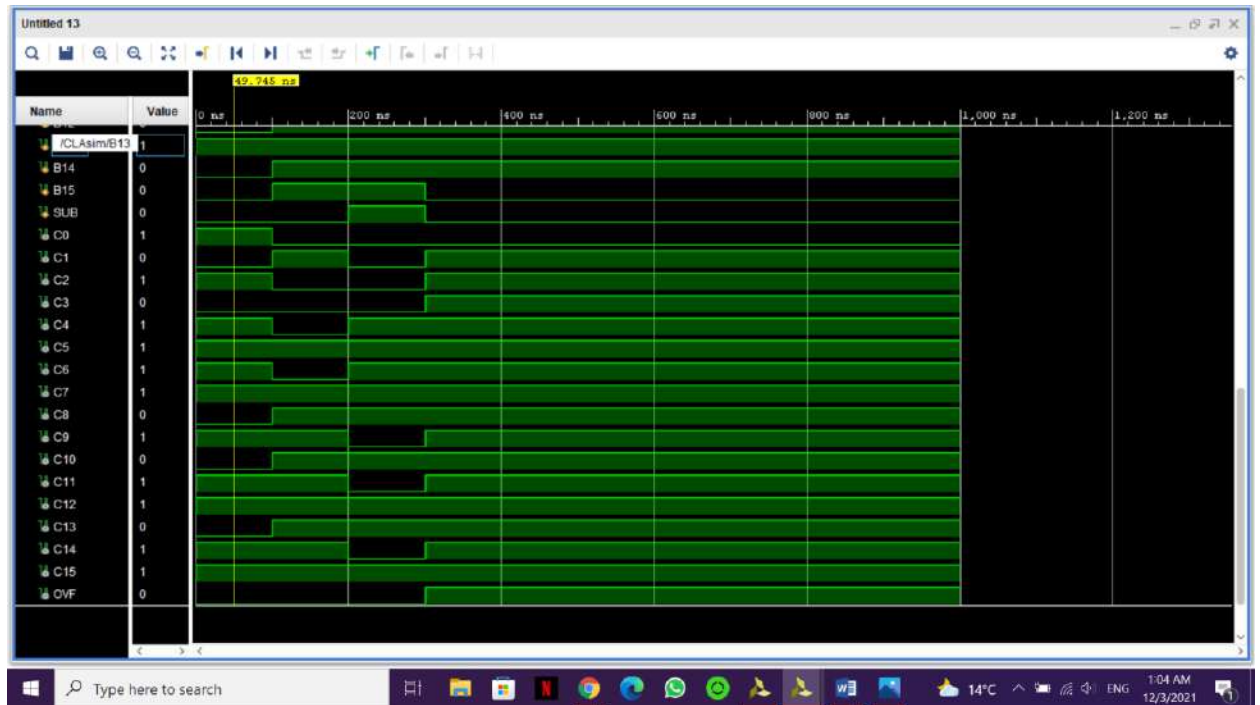


- v. A = 327676
 B = 32767
 SUB = 1
 OVF = 1

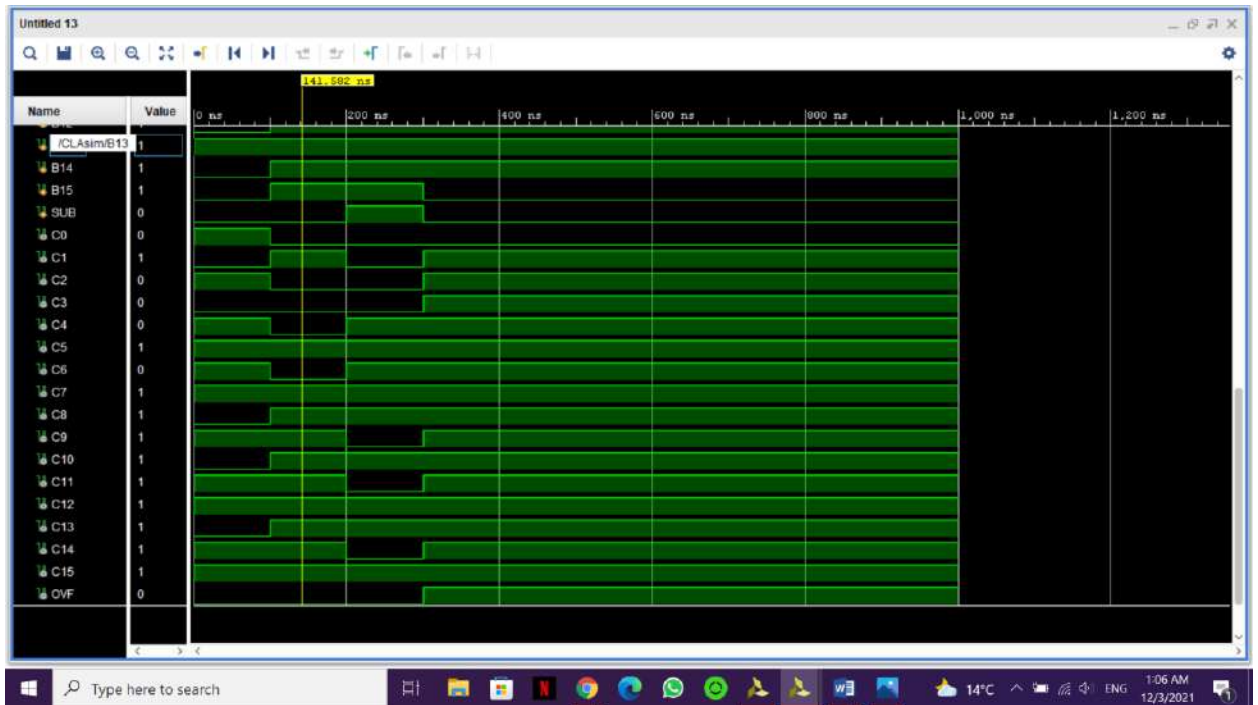


2) 16-bit hybrid adder-subtractor using four 4-bit carry lookahead adders (CLAs)

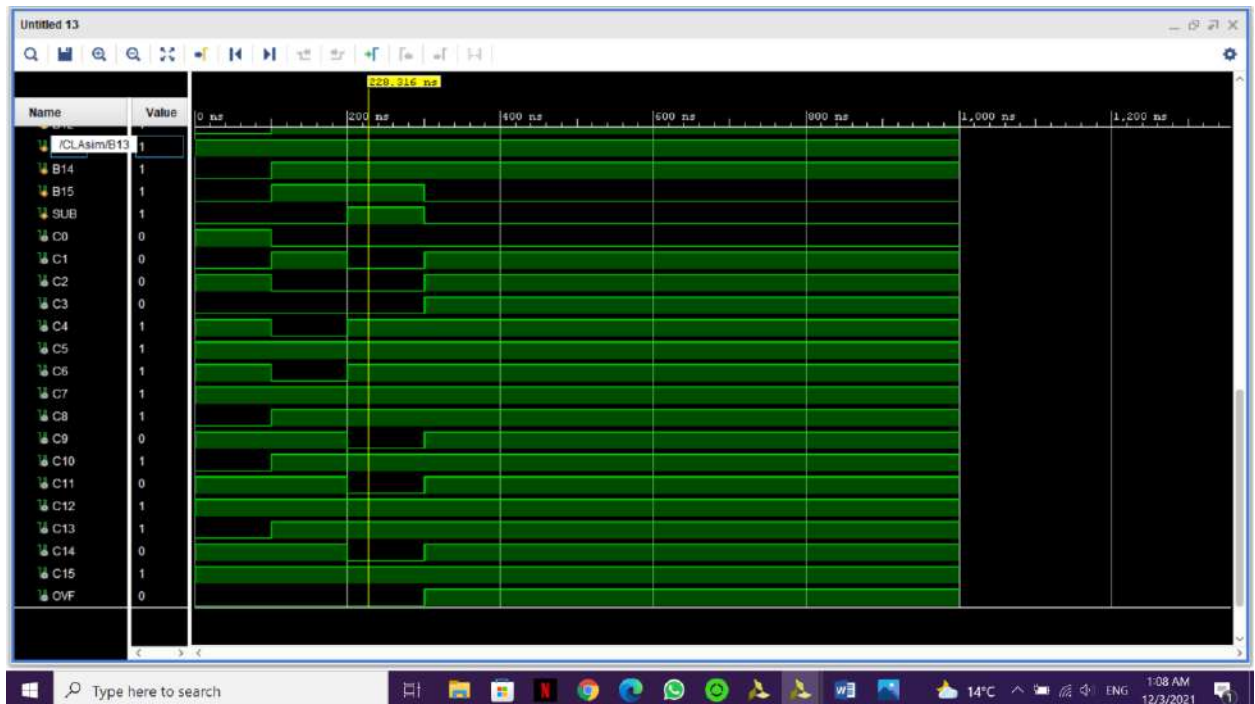
- i. A = -18969
 B = 9483
 SUB = 0
 C = 1101101011110101 = -9483
 OVF = 0



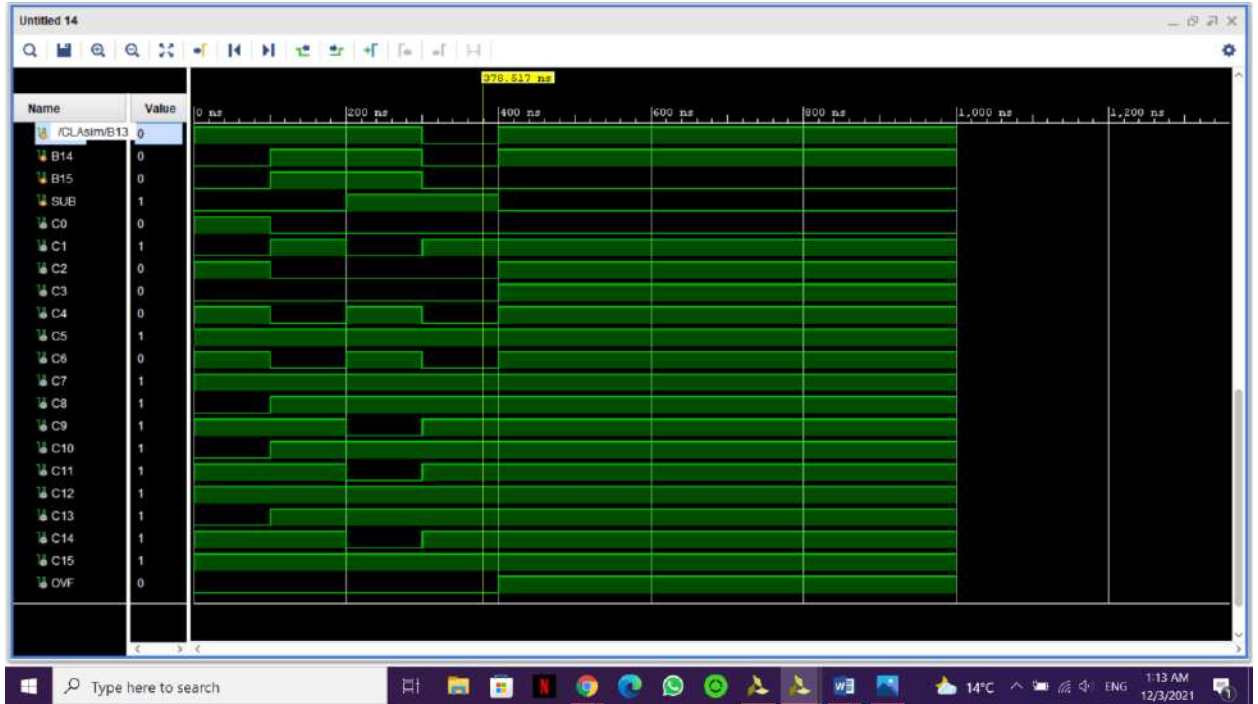
- ii. A = 153
 B = -247
 SUB = 0
 C = 1111111110100010 = -94
 OVF = 0



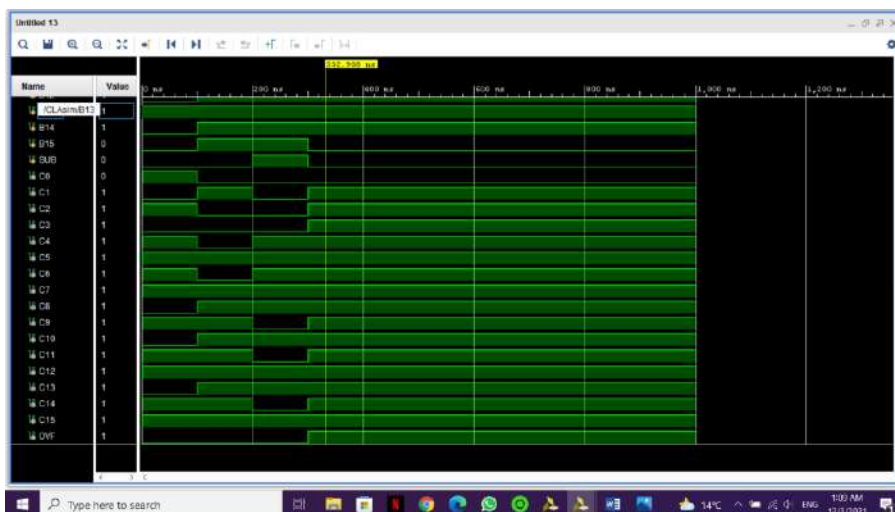
- iii. A = -18966
 B = -6
 SUB = 1
 C = 1011010111110000 = -18960
 OVF = 0



- iv. A = 256
B = 350
SUB = 1
C = 1111111110100010 = -94
OVF = 0



- v. A = 327676
B = 32767
SUB = 1
OVF = 1



Implementation

1) 16-bit ripple-carry adder-subtractor using full adders

Number of LUTs = 23

lab3 - [D:\XilProj\lab3\lab3.xpr] - Vivado 2018.2

Implementation Complete ✓

Flow Navigator

- Report DRC
- Report Utilization
- Report Power
- Schematic
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Utilization
 - Report Power
 - Schematic
- PROGRAM AND DEBUG

PROJECT MANAGER - lab3

Utilization Post-Synthesis | Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	23	63400	0.04
IO	50	210	23.81

Power Summary | On-Chip

Total On-Chip Power: 12.367 W

Junction Temperature: 81.4 °C

Thermal Margin: 3.6 °C (0.8 W)

Effective θ_{JA} : 4.6 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Tcl Console Messages Log Reports x Design Rules

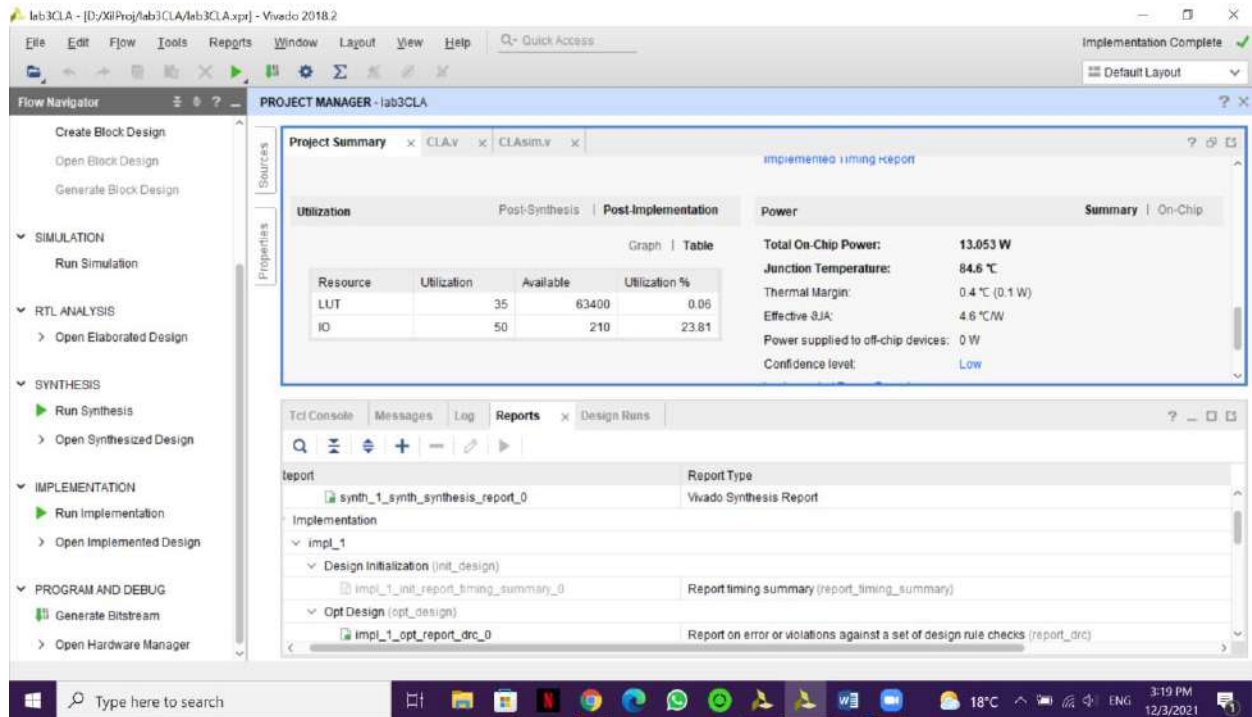
Report	Report Type
impl_1_place_report_utilization_0	Report on utilization of resources on the targeted device (report_utilization)
impl_1_place_report_control_sets_0	Report the unique control sets in design (report_control_sets)
impl_1_place_report_incremental_reuse_0	Report on achievable incremental reuse for the given design-checkpoint (report_incremental_reuse)
impl_1_place_report_incremental_reuse_1	Report on achievable incremental reuse for the given design-checkpoint (report_incremental_reuse)
impl_1_place_report_timing_summary_0	Report timing summary (report_timing_summary)
Post-Place Power Opt Design (post_place_power_opt_design)	
impl_1_post_place_power_opt_report_timing_summary_0	Report timing summary (report_timing_summary)

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2) 16-bit hybrid adder-subtractor using four 4-bit carry lookahead adders (CLAs)

Number of LUTs = 35



Results

Design 1 is better in terms of area as it utilizes 23LUTs and design 2 has 35LUTs therefore the shorter the area, the better and less complex the design. However, design 2 is better in terms of time delay as it uses Carry lookahead adders, therefore the propagation delay is reduced and it works faster than design 1. As a result, we will decide on which adder/subtractor to use after considering if time delay is the main priority or if area is the main priority.