**A picture containing logo

Description automatically generated**

**King Fahd University for Petroleum & Minerals**

**Mini Project:**

**Descent Timer**

Date:11/17/2020

**Prepared by:**

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**For:**

**COE203 - 201**

1.Objectives:

In this project we aim to design a descent timer based on Verilog and programmed on an FPGA board. Also, we will simulate the project based on computer-generated clock signals

2.Proceduer:

Task1: Designing mod10:

This module is used to count from 9-0 for the first second-digit.

1. Create new projects of HDL type.

Task2: Designing mod6:

This module is used to count from 5-0 for the second digit of the seconds.

1. Create new Verilog file named BCD\_3D.

Task2: Designing DownCounter:

This module is used to count from 9-0 for the two minute digits as well as loading the starting time inputs. If the inputs larger than 99 an LED error will turn on and set all digits zeros.

1. Create new Verilog file named BCD\_3D.

3.Problem Faced:

No problem faced

4.Work Distribution:

|  |  |  |
| --- | --- | --- |
|  | Sami | Ammar |
| Task1 | 0% | 100% |
| Task2 | 20% | 80% |
| Task3 | 100% | 0% |
| Report | 45% | 55% |
| Questions | 40% | 60% |

6.Conclusion:

We managed to design a response circuit that uses the previous circuit to measure a person response time. We learnt about the saturated counters; that when they reached the maximus do not recount again. Also, we learnt to combine to Xilinx projects and extend one project with the other.