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**King Fahd University for Petroleum & Minerals**

**Mini Project:**

**Descent Timer**

Date:11/17/2020

**Prepared by:**

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**For:**

**COE203 - 201**

1.Objectives:

In this project we aim to design a descent timer based on Verilog and programmed on an FPGA board. Also, we will simulate the project based on computer-generated clock signals

2.Proceduer:

Task1.1: Designing 1-Digit Saturating BCD Counter:

1. Create new projects of HDL type.
2. Create new source of Verilog module and named BCD\_1D.
3. Write the module's inputs as "clk", "reset" and "enable".
4. Write the outputs as "CEO" and reg[3:0]Q.
5. Assign "Q[3] & Q[0]" to "CEO".
6. Make a condition so that when "reset" is true then make Q equal to 0.
7. Make another condition so that when "enable" is true then make Q = 0 if "CEO" is true, otherwise increment Q by one.

Task1.2: Designing 3-Digit Saturating BCD Counter:

1. Create new Verilog file named BCD\_3D.
2. Make wire for each of CEO0, CEO1 and CEO2.
3. Assign "enable & ~CEO" to EN0.
4. Assign "CEO0 & EN0" to EN1.

3.Problem Faced:

No problem faced

4.Work Distribution:

|  |  |  |
| --- | --- | --- |
|  | Sami | Ammar |
| Task1 | 0% | 100% |
| Task2 | 20% | 80% |
| Task3 | 100% | 0% |
| Report | 45% | 55% |
| Questions | 40% | 60% |

6.Conclusion:

We managed to design a response circuit that uses the previous circuit to measure a person response time. We learnt about the saturated counters; that when they reached the maximus do not recount again. Also, we learnt to combine to Xilinx projects and extend one project with the other.