Lab 5

For the implementation of the RAM, we have an array of 128 32-bit logic vectors called i\_ram. We have two if statements that check for write enable and stores data in to i\_ram. The other one checks for output enable and stores the value at the address to dataout. We also have another if statement that resets all memory to 0 if the reset is 1. In the second part we made portmaps and with select statements to tell us which registers to use and how we want to use them. The address port is only 30 bits wide because we have to use OE and WE which are each 1 bit so we combine them with the address port to save space.



