Student ID: R12K41003

Student Name: 張柏彥

Computer-Aided VLSI System Design

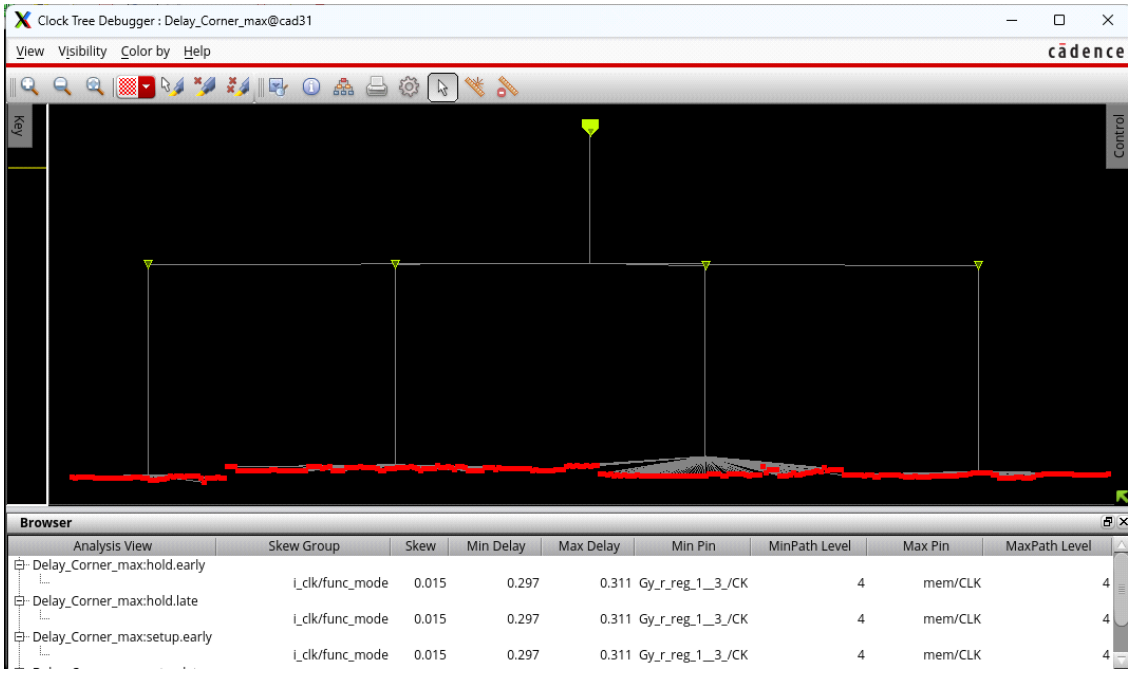
Homework 5 Report

APR Results

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	489062.43
	Core Area (um^2)	290445.51
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	5.2ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		From TA

Snapshots

CCOpt Clock Tree Debugger result:



DRC and LVS checking :

```
innovus 15> verify_drc
 *** Starting Verify DRC (MEM: 1800.4) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 176.800 176.800} 1 of 16
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 0.000 353.600 176.800} 2 of 16
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 0.000 530.400 176.800} 3 of 16
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 0.000 699.200 176.800} 4 of 16
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 176.800 176.800 353.600} 5 of 16
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 176.800 353.600 353.600} 6 of 16
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 176.800 530.400 353.600} 7 of 16
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 176.800 699.200 353.600} 8 of 16
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 353.600 176.800 530.400} 9 of 16
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 353.600 353.600 530.400} 10 of 16
  VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 353.600 530.400 530.400} 11 of 16
  VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 353.600 699.200 530.400} 12 of 16
  VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 530.400 176.800 699.460} 13 of 16
  VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 530.400 353.600 699.460} 14 of 16
  VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 530.400 530.400 699.460} 15 of 16
  VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 530.400 699.200 699.460} 16 of 16
  VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:04.0  ELAPSED TIME: 4.00  MEM: 1.7M) ***

innovus 16>
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Dec  2 20:14:18 2023

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (699.2000, 699.4600)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 20:14:18 **** Processed 5000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Dec  2 20:14:19 2023
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.9  MEM: 0.555M)

innovus 16>
```

Timing report(setup & hold):

```
End delay calculation (fullDC). (MEM=1797.32 CPU=0:00:01.1 REAL=0:00:01.0)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
2023-12-02 20:04   r2k41003   user   -rw-r--r--
+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.423  |  0.423  |  0.509  |  1.293  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 37.250%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 12.28 sec
Total Real time: 13.0 sec
Total Memory Usage: 1797.320312 Mbytes
Reset AAE Options
innovus 16>
ng to the professional edition here:  https://mobaxterm.mobatek.net
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.713  |  0.713  |  2.499  |  3.399  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 37.250%
       (100.000% with Fillers)
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 10.39 sec
Total Real time: 11.0 sec
Total Memory Usage: 1755.121094 Mbytes
Reset AAE Options
innovus 16>
```

Critical path:

```
End delay calculation. (MEM=1795.55 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1795.55 CPU=0:00:00.2 REAL=0:00:00.0)
Path 1: MET Setup Check with Pin psum_r_reg_13_/CK
Endpoint:   psum_r_reg_13_/D (^) checked with  leading edge of 'i_clk'
Beginpoint: mem/Q[3]         (v) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.303
- Setup                         0.207
+ Phase Shift                   5.000
+ CPPR Adjustment               0.000
= Required Time                 5.096
- Arrival Time                  4.673
= Slack Time                    0.423
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.002
     = Beginpoint Arrival Time           0.002
     +-------------------------------------------------------------------------------+
     |    Instance    |       Arc       |    Cell     | Delay | Arrival | Required |
     |                |                 |             |       |  Time   |   Time   |
     |----------------+-----------------+-------------+-------+---------+----------|
     | mem            | CLK ^           |             |       |   0.002 |    0.425 |
     | mem            | CLK ^ -> Q[3] v | sram_4096x8 | 2.696 |   2.699 |    3.121 |
     | U4247          | A v -> Y ^      | NAND2X4     | 0.166 |   2.865 |    3.287 |
     | U3551          | A ^ -> Y v      | INVX6       | 0.160 |   3.025 |    3.447 |
     | U3311          | B v -> Y ^      | NAND2BX1    | 0.135 |   3.160 |    3.583 |
     | U4295          | B0 ^ -> Y ^     | OA21X2      | 0.179 |   3.340 |    3.762 |
     | U1574          | A ^ -> Y v      | NAND2X1     | 0.069 |   3.408 |    3.831 |
     | U3789          | A1N v -> Y v    | AOI2BB1X1   | 0.257 |   3.665 |    4.088 |
     | U2993          | A v -> Y v      | OR2X4       | 0.159 |   3.825 |    4.247 |
     | U4672          | A1 v -> Y v     | OA21X4      | 0.201 |   4.026 |    4.448 |
     | U1742          | A v -> Y ^      | NAND4X2     | 0.081 |   4.107 |    4.529 |
     | U1739          | A ^ -> Y v      | INVX1       | 0.090 |   4.197 |    4.620 |
     | U3057          | A v -> Y v      | OR2X2       | 0.194 |   4.392 |    4.814 |
     | U3525          | A v -> Y ^      | NAND3X1     | 0.105 |   4.497 |    4.919 |
     | U4298          | B1 ^ -> Y ^     | OA22X4      | 0.176 |   4.673 |    5.096 |
     | psum_r_reg_13_ | D ^             | DFFRX1      | 0.000 |   4.673 |    5.096 |
     +-------------------------------------------------------------------------------+

innovus 17>
to the professional edition here:  https://mobaxterm.mobatek.net
```

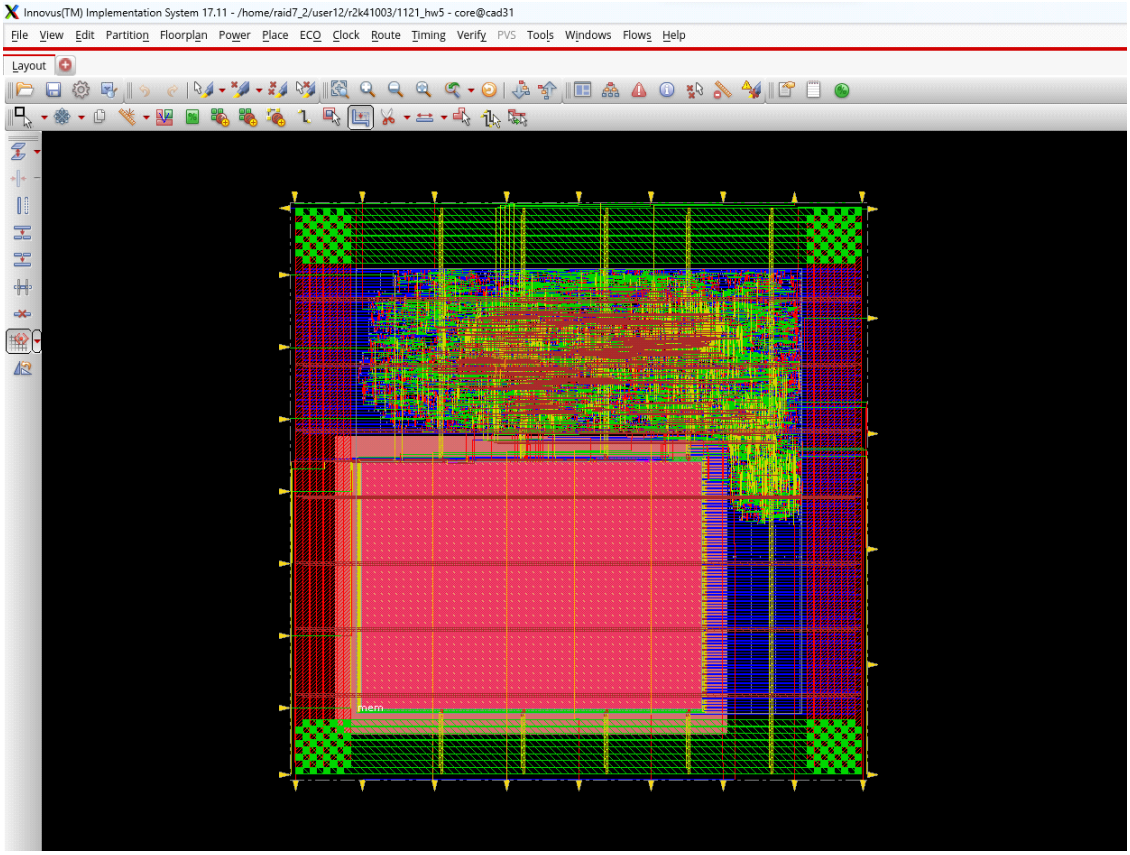
GDS stream out:

```
Custom Box                          0

Trim Metal                          0

Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/sram_4096x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/sram_4096x8.gds ......
        ****** Merge file: library/gds/sram_4096x8.gds has version number: 5.
        ****** Merge file: library/gds/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
innovus 18>
```

Final area report:

```
innovus 19> analyzeFloorplan
**WARN: (IMPAFPU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesign + tri
reate_ps_per_micron_model + timeDesign -proto + load_timing_debug_report -proto' to analyze congestion
 for the floorplan.
Start to collect the design information.
Build netlist information for Cell core.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 81320 sites (138033 um^2) / alloc_area 81320 sites (138033 um^2).
Pin Density = 0.09693.
            = total # of pins 16586 / total area 171112.
************************ Analyze Floorplan ************************
    Die Area(um^2)            : 489062.43
    Core Area(um^2)           : 290445.51
    Chip Density (Counting Std Cells and MACROs and IOs): 53.654%
    Core Density (Counting Std Cells and MACROs): 90.345%
    Average utilization       : 100.000%
    Number of instance(s)     : 13594
    Number of Macro(s)        : 1
    Number of IO Pin(s)       : 33
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
innovus 20>
```

Final layout:



Floorplanning strategy:

把 SRAM 擺在角落，或是擺放在 core 的四周，利於這些大型 Macro 的供電。